All-optical logic circuits based on polarization properties of nondegenerate four-wave mixing

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All-optical logic circuits based on the polarization properties of nondegenerate four-wave mixing are proposed. Schemes to perform multiple triple-product logic functions are discussed, and it is shown that higher-level Boolean operations that involve several bits can be implemented without resorting to the standard two-input gates. As a simple illustration of the idea, a circuit that performs error correction on a (3,1) Hamming code is demonstrated. Error-free performance (bit error rate of $<10^{-9}$) at 2.5 Gbit/s is achieved after single-error correction on the Hamming word with 50% errors. © 2001 Optical Society of America

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1. INTRODUCTION

Nonlinear optics has been of increased interest for all-optical signal processing in high-speed photonic networks.[1,2] Sample applications include all-optical switching as well as demultiplexing.[3–5] In addition, Boolean operations such as exclusive OR (EXOR) and two-bit addition have been demonstrated optically with a combination of such switching devices.[6,7] Devices have employed both fiber-based and semiconductor-based nonlinear elements. In the former case the physical nonlinearity is the Kerr nonlinearity of silica glass. In the latter case the nonlinearity results from a variety of ultrafast mechanisms in semiconductor gain media, including carrier heating and spectral hole burning.[8] Apart from long-haul data transmission, all-optical logic gates might someday find applications in local-area networks to provide certain limited all-optical functionality. Such functions will only make sense when equivalent electrical solutions are cumbersome or when a real advantage can be realized by maintaining signals in optical form. There has been interest in all-optical functionality for switching and routing in wavelength-division-multiplexed (WDM) systems, but so far there has been very limited implementation of these functions.[9,10] The likelihood of more sophisticated all-optical functions will be higher should time-division-multiplexed (TDM) or mixed TDM/WDM systems be implemented since this format lends itself better to a variety of well-established all-optical switching solutions.[1]

The fiber-transmission context for this paper is based neither on TDM or conventional WDM formats but instead takes an even-more forward-looking view of fiber communications based on the notion of a spectral data bus first introduced by Loeb *et al.*[11] at IBM. Sometimes called bytewide transmission, this format assigns each bit of a binary word to a different wavelength for copropagation along a fiber. The advantage of this format is clear in that enormous space savings are possible by compressing a normally large electrical bus onto a compact and lightweight optical fiber. Furthermore, the network ar-

chitecture is simplified since high-speed serializers/deserializers are not required. It is clear that the applications for this form of transmission would most likely be shared computer backplanes in large clusters or networks of supercomputers. A serious limitation associated with bytewide transmission is the problem of dispersion-induced bit skew. However, as noted by Jeong *et al.*,[12] modern techniques for dispersion management in fiber systems could be used to minimize bit skew in such a system.

There are interesting front-end signal-processing possibilities associated with spectral bus transmission including bytewide error correction and detection[13] and, possibly, improved security. We define front-end here to mean a device that is situated between the bus and whatever the bus is linked to (presumably a computer). In this very limited context we propose and study a form of optical logic designed to process data in a spectral form.

As background on the basic idea, we note that nondegenerate four-wave mixing (ND-FWM) provides a convenient means to multiply bits on a spectral bus. The fundamental process involving a third-order nonlinearity can, in fact, multiply up to three bits of information. So, in principle, a three-bit Boolean operation is possible. If the coupling to the nonlinear medium is strong enough, even higher-order products are possible so that higher-order *N*-input logic operations are feasible. A convenient way to identify a preferred logic state is suggested by observing that the four-wave mixing (FWM) output is sensitive to the states of polarization of the incident fields. Consequently, polarization-selection rules for the FWM process can be exploited to develop a logic operation. Use of polarization shift keying (PolSK) for information transmission is not new[14] and has been used in system demonstrations.[15]

We have earlier proposed a class of all-optical logic gates based on PolSK coding on a spectral bus.[16,17] In this paper we investigate the logic operations that can be performed by use of ND-FWM on PolSK-coded spectral data. We show that certain higher-order logic operations need not be constructed in terms of the standard two-
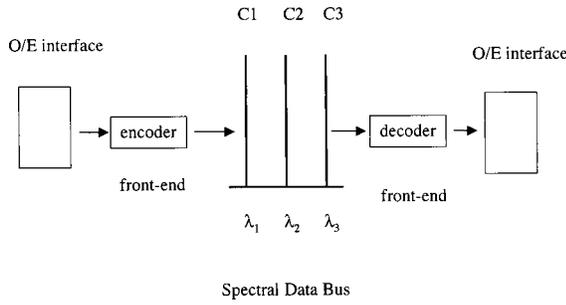
Fig. 1. All-optical logic circuits for on-the-fly signal processing on a spectral bus. C1, C2, C3, etc., represent encoded bits placed on separate wavelength channels.

input gates but can be realized more directly in the selection rules of multiphoton-scattering processes. As a simple example of this approach, we describe an all-optical front-end processor for error detection and correction (see Fig. 1) and then provide a simple experimental demonstration of this idea.

2. THEORY

A. (3,1) Hamming Code
We start by describing a logic circuit that performs on-the-fly error correction on a (3,1) Hamming code. Binary information is sent as a three-bit word that consists of the data bit accompanied by two check bits; i.e., binary information is sent as vectors (111) and (000). This added redundancy makes it possible to correct for a single error that can occur on any bit of the three-bit word.[18] The truth table for error correction by use of the (3,1) Hamming code is shown in Table 1. The binary word is PolSK modulated, where the binary states "1" and "0" are represented by orthogonal linear states of polarization along the fast and the slow axes of a polarization-maintaining fiber. This scheme enables implementation of the NOT function for binary data by the use of passive elements such as a half-wave plate.

Bytewide transmission is achieved by assigning each bit to a separate wavelength channel; thus the optical fiber acts as a parallel data bus. Also note that since the coding and decoding is accomplished in a bytewide fashion, the redundancy added by the code does not slow down the transmission rate. For the purpose of discussion the three-bit spectral word is assigned channels C1, C2, and C3. The logic operation realized in the error-correcting circuit is

$$EC = (C1 \cap C2) \cup (C2 \cap C3) \cup (C3 \cap C1), \qquad (1)$$

where "$\cap$" denotes the logical AND function, "$\cup$" denotes the logical OR function and EC is the error-corrected information. This operation corresponds to using the CARRY bit of a three-bit modulo-2 addition. This can also be written in terms of triple-product Boolean operations as

$$EC = (C1 \cap C2 \cap C3) \cup (\overline{C1} \cap C2 \cap C3)$$

$$\cup (C1 \cap \overline{C2} \cap C3) \cup (C1 \cap C2 \cap \overline{C3}). \qquad (2)$$

The FWM process as described below creates the EC channel, which is then filtered and detected.

The copropagating electric field E_k generated by the FWM process is given by

$$E_k(\omega_{EC} = \omega_{C1} + \omega_{C2} - \omega_{C3})$$

$$\propto \chi^{(3)}_{klmn} E_l(\omega_{C1}) E_m(\omega_{C2}) E_n^*(\omega_{C3}), \qquad (3)$$

where ω_i, i = EC, C1, C2, and C3, is the angular frequency of the optical wave and (*) denotes complex conjugation. $\chi^{(3)}_{klmn}$ is the third-order nonlinear susceptibility, which is a tensor of rank four and, as noted in the introduction, is dependent on the states of polarization of the electric fields of C1, C2, and C3. The geometry of the FWM process considered in this paper is such that the three input waves are launched into a single-transverse-mode waveguide (here a semiconductor optical amplifier, or SOA) along the same direction of propagation. The extracted product wave hence propagates along the direction of incidence.

In a bulk semiconductor medium the polarization dependence of the mixing product at ω_{EC} is given by

$$e_{EC} \propto [(e_{C1} \cdot e_{C3}^*) e_{C2} + (e_{C2} \cdot e_{C3}^*) e_{C1}], \qquad (4)$$

where e_i, i = EC, C1, C2, and C3, is the unit vector along the direction of the electric field. The terms in relation (4) can be physically interpreted as the FWM signal at EC being generated as follows: C3 forms dynamic gain and index gratings with C1 (or C2). Then, C2 (or C1) scatters off this grating to generate two FWM sidebands, one of them being at ω_{EC}.[19] These processes are diagramatically represented in Fig. 2. In a SOA, the unit vector e_i, representing each binary state, is aligned along the TE or TM direction of the waveguide structure to avoid polarization walk-off of the incident fields arising from birefringence of the waveguide.[20] The EC signal is generated in one of the following ways:

Table 1. Truth Table for Error Correction Using the (3,1) Hamming Code

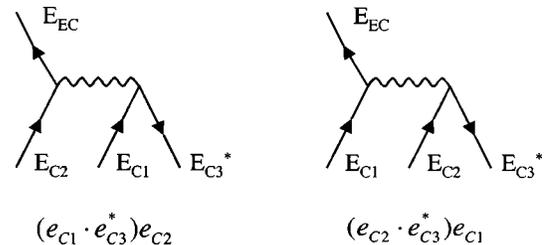| C1	C2	C3	EC
1	1	1	1
0	0	0	0
1	1	0	1
1	0	1	1
0	1	1	1
0	0	1	0
0	1	0	0
1	0	0	0

Fig. 2. Diagrammatic representation of the nondegenerate FWM process. The straight lines represent the photons involved, and the waves represent the dynamic gain and index gratings.
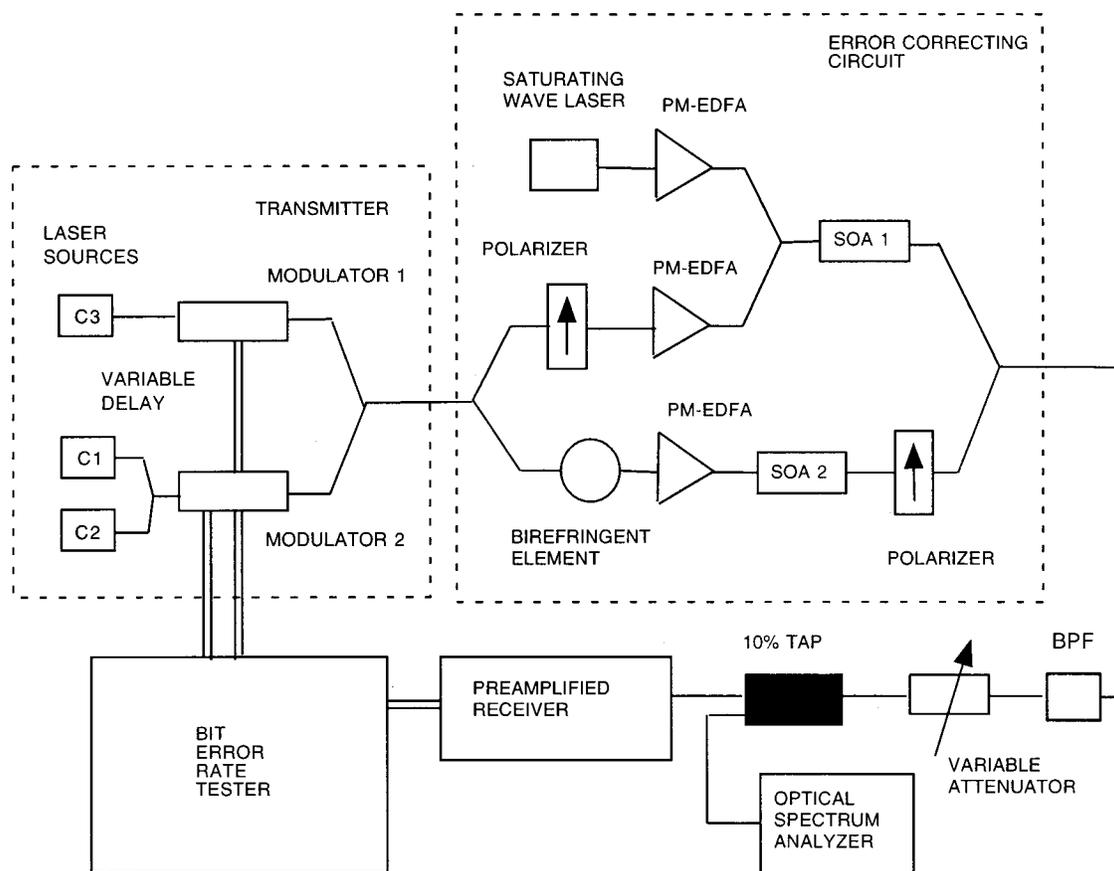
Fig. 3.   Schematic of the error-correcting circuit (BPF is an optical bandpass filter; PM-EDFA is a polarization-maintaining erbium-doped fiber amplifier).

• When all three input electric vectors are parallel (corresponding to identical bits on each channel, i.e., no errors are present), the electric field of the mixing signal at ω_{EC} is parallel to the three inputs. This is used, in turn, to generate an output when no error correction is necessary.

• When one of the electric fields is orthogonal to the other two (corresponding to an error on that bit), a product wave at ω_{EC} is generated only when C1 and C2 are orthogonal. In this case, C3 creates a grating with either C1 or C2 (the one whose polarization is parallel to C3), which scatters energy off the third wavelength to generate a FWM signal at ω_{EC} that is orthogonal to C3. This property is utilized to correct for errors.

The error-correcting circuit requires at least three SOA's (only two are required if retaining the PolSK format on the EC channel is not necessary) to generate the proper FWM signal in all possible cases. The circuit is designed in such a way that the FWM product at ω_{EC} occurs in only one SOA at a time. This is done in order to avoid interference of the desired FWM signal with additional spurious signals that would degrade the performance of the circuit. This is accomplished by adding a pre-processing element before each SOA as shown in Fig. 3. One of the preprocessing elements is a polarizer with its transmission axis aligned to either the fast or the slow axis of the polarization-maintaining fiber. The other element is a wavelength-selective half-wave plate, which

will be referred to as the birefringent element. It acts as a half-wave plate for C3 and a full-wave plate for C1 and C2. The result is that the state of polarization of C3 gets rotated by 90° (and thus inverts the binary state on C3) whereas that of C1 and C2 remain almost unchanged.

The output of the circuit for each possible case is as follows:

• In the absence of any errors, C1, C2, and C3 are parallel at the input, and mixing at ω_{EC} occurs in the SOA after the polarizer (SOA 1), whose axis coincides with C1, C2, and C3. The mixing signal is parallel to the input bits and has the same binary state as the input bits. Thus the output is generated without error correction, and it is for this reason that this arm is called the noncorrecting arm. (It should be noted that a polarizer changes PolSK modulation to amplitude-shift-keying modulation. Hence if PolSK modulation is to be preserved, two such noncorrecting arms are required, each with a polarizer as a preprocessing element aligned to the slow and the fast axes of the polarization-maintaining fiber, respectively.) Furthermore, when C1, C2, and C3 (all being parallel) pass through the birefringent element, which is the preprocessing element in the other arm, C3 becomes orthogonal to C1 and C2. In this case, no mixing at ω_{EC} takes place in the SOA after the birefringent element (SOA 2); in accordance with relation (4).

• In the presence of an error, C1, C2, and C3 will not all be parallel, and thus one or more of them will not pass

through the polarizer. Hence no mixing will occur in SOA 1. There are two possible cases. When the error is on C3, it is orthogonal to both C1 and C2. After passing through the birefringent element, C3 will become parallel to C1 and C2, and the mixing signal in SOA 2 will have the same binary state as C1 and C2. Thus an error on C3 will be corrected. When the error is on either C1 or C2, C3 will align with the incorrect bit (since it gets inverted by the birefringent element) and will form a grating that scatters off the correct bit to give a mixing signal parallel to the correct bit. Thus an error-corrected signal is generated, and hence the arm with the birefringent element as the preprocessing element is called the correcting arm.

The Boolean operation implemented in the noncorrecting arm is $(C1 \cap C2 \cap C3)$, and that implemented in the correcting arm is $(\overline{C1} \cap C2 \cap C3) \cup (C1 \cap \overline{C2} \cap C3) \cap (C1 \cap C2 \cap \overline{C3})$. Thus each triple-product Boolean function can be associated with the terms in relation (4) contributing to the ND-FWM process.

As illustrated in Fig. 4, the same circuit can be used to implement the SUM bit of a three-bit modulo-2 addition, as given by

$$\text{SUM} = C1 \oplus C2 \oplus C3, \tag{5}$$

where "$\oplus$" denotes the logic function exclusive OR (EXOR). This expression can be rewritten in terms of triple-product functions as

$$\text{SUM} = (C1 \cap C2 \cap C3) \cup (\overline{C1} \cap \overline{C2} \cap C3)$$

$$\cup (C1 \cap \overline{C2} \cap \overline{C3}) \cup (\overline{C1} \cap C2 \cap \overline{C3}). \tag{6}$$

The generation of this operation in Fig. 4 is possible by taking the output of the correcting arm of the error-correcting circuit and inverting its output by a fiber cross splice before combining it at the output of the circuit.

B.   Encoding and Decoding Other Hamming Codes
The SUM bit, $C1 \oplus C2 \oplus C3$, also corresponds to the parity of the three bits C1, C2, and C3 and can be used to generate parity bits for encoding of other Hamming codes. For example, the encoder for the (7,4) Hamming code takes four input data bits [D1, D2, D3, D4] and creates three additional parity bits, given by

$$\text{P-}(412) = D4 \oplus D1 \oplus D2, \tag{7a}$$

$$\text{P-}(423) = D4 \oplus D2 \oplus D3, \tag{7b}$$

$$\text{P-}(413) = D4 \oplus D1 \oplus D3, \tag{7c}$$

i.e., the parity bits are SUM bits of the three-bit additions of D4 with two additional bits $[D_i, D_k]$ $(i, k = 1, 2, 3)$
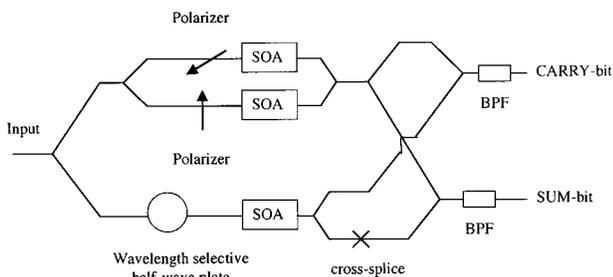
Fig. 4.   Schematic of a three-bit modulo-2 adder (BPF is an optical bandpass filter).
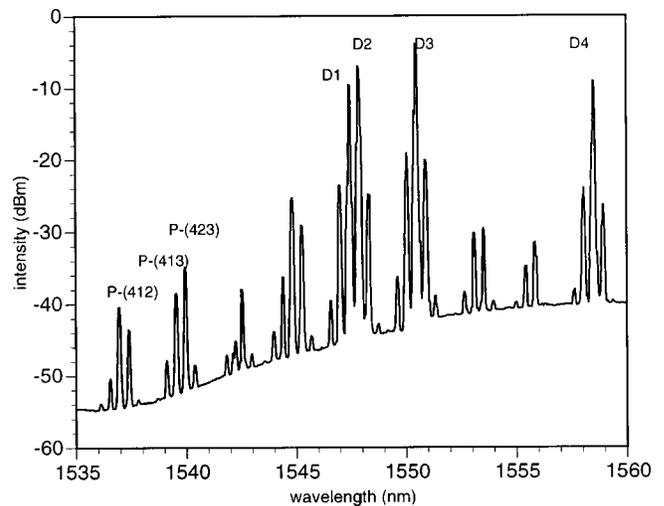
Fig. 5.   Optical spectrum at the output of the SOA showing the wavelengths for the data bits [D1–D4] and the parity bits [P-(412), P-(423), P-(413)] for encoding the (7,4) Hamming code.
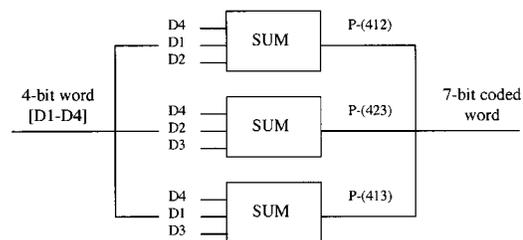
Fig. 6.   Schematic of the (7,4) coding when the three parity bits are generated simultaneously in the same circuit.

from the remaining three bits (there is nothing special about D4; it is just taken for this example). For spectrally placed channels [D1–D4], each ND-FWM of D4 with $[D_i, D_k]$ will occur at a different wavelength channel, as shown experimentally in Fig. 5 and given by

$$E_k(\omega_{\text{P-}(412)}) = \omega_{\text{D1}} + \omega_{\text{D2}} - \omega_{\text{D4}})$$

$$\propto \chi^{(3)}_{klmn} E_l(\omega_{\text{D1}}) E_m(\omega_{\text{D2}}) E_n^*(\omega_{\text{D4}}), \tag{8a}$$

$$E_k(\omega_{\text{P-}(423)}) = \omega_{\text{D2}} + \omega_{\text{D3}} - \omega_{\text{D4}})$$

$$\propto \chi^{(3)}_{klmn} E_l(\omega_{\text{D2}}) E_m(\omega_{\text{D3}}) E_n^*(\omega_{\text{D4}}), \tag{8b}$$

$$E_k(\omega_{\text{P-}(413)}) = \omega_{\text{D1}} + \omega_{\text{D3}} - \omega_{\text{D4}})$$

$$\propto \chi^{(3)}_{klmn} E_l(\omega_{\text{D1}}) E_m(\omega_{\text{D3}}) E_n^*(\omega_{\text{D4}}). \tag{8c}$$

In this case the three-bit adder circuit described above can be used as an encoder for the (7,4) Hamming code, which simultaneously generates the three parity bits using different ND-FWM processes. Since D4 is common to all the additions, the preprocessing element in one of the arms should act as a half-wave plate for D1, D2, and D3 and a full-wave plate for D4. The seven-bit word at the output of the encoder will be in a bytewide format with the data and the parity bits on separate wavelength channels. Figure 5 shows the different FWM signals that arise from to the presence of four wavelength channels [D1–D4], and the ND-FWM signals that generate the parity bits are marked. Thus three independent logic functions can in principle be implemented in parallel in one circuit. This is schematically shown in Fig. 6.

In a similar fashion, one way to realize a decoder circuit for the (7,4) Hamming code is by using the three-bit adder circuits as building blocks and cascading them. The transmitted code word contains the original four bits [D1–D4] and three parity bits [P-(412), P-(423), P-(413)]. To make a distinction between transmitted and received data, the transmitted bits are denoted by upper case and the received bits are denoted by lower case. Thus the transmitted word is [D1, D2, D3, D4, P-(412), P-(423), P-(413)], whereas the received word is [d1, d2, d3, d4, p-(412), p-(423), p-(413)]. For the sake of brevity, SUM[A1, A2, A3] and CARRY[A1, A2, A3] are used to denote the SUM and the CARRY bits resulting from the modulo-2 addition of the three bits A1, A2, and A3. Thus P-(412) = SUM[D4, D1, D2].

Since D4 is present in all three parity bits, it is the first bit that is checked for errors. The following additions are performed on the received bits:

$$d4\text{-}(12) = \text{SUM}[\,p\text{-}(412),\ d1,\ d2\,], \tag{9a}$$

$$d4\text{-}(23) = \text{SUM}[\,p\text{-}(423),\ d2,\ d3\,], \tag{9b}$$

$$d4\text{-}(13) = \text{SUM}[\,p\text{-}(413),\ d1,\ d3\,]. \tag{9c}$$

In the absence of any errors (received bit equals transmitted bit), each of the above additions would equal D4. For example, if d4-(12) is computed in the absence of any errors, it equals

$$d4\text{-}(12) = \text{SUM}[\,p\text{-}(412),\ d1,\ d2\,]$$
$$= \text{SUM}[\,P\text{-}(412),\ D1,\ D2\,]$$
$$= (D4 \oplus D1 \oplus D2 \oplus D1 \oplus D2) = D4. \tag{10}$$

Since CARRY[A1, A2, A3] equals the bit that occurs the largest number of times among [A1–A3]. This can be used to find the correct transmitted bit D4 from the four bits [d4, d4-(12), d4-(23), d4-(13)] by use of the following operations:

$$D4 = \text{CARRY}[\,\text{CARRY}[d4,\ d4\text{-}(12),\ d4\text{-}(23)],$$
$$\text{CARRY}[d4,\ d4\text{-}(23),\ d4\text{-}(13)],$$
$$\text{CARRY}[d4,\ d4\text{-}(12),\ d4\text{-}(13)]]. \tag{11}$$

This ensures that D4 is correctly generated for all possible cases of the received code word, including those with a single error on any bit. For example, if the error is on d2, i.e., $d2 = \overline{D2} = D2 \oplus 1$, we obtain

$$d4\text{-}(12) = \text{SUM}[\,P\text{-}(412),\ D1,\ d2\,]$$
$$= (D4 \oplus D1 \oplus D2 \oplus D1 \oplus D2 \oplus 1)$$
$$= D4 \oplus 1 = \overline{D4}, \tag{12a}$$

$$d4\text{-}(23) = \text{SUM}[\,P\text{-}(423),\ D2,\ D3\,]$$
$$= (D4 \oplus D2 \oplus D3 \oplus D2 \oplus D3 \oplus 1)$$
$$= D4 \oplus 1 = \overline{D4}, \tag{12b}$$

$$d4\text{-}(13) = \text{SUM}[\,P\text{-}(413),\ D1,\ D3\,]$$
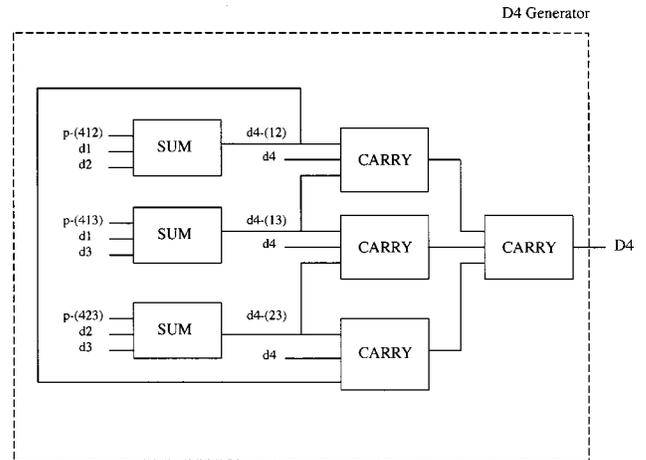$$= (D4 \oplus D1 \oplus D3 \oplus D1 \oplus D3) = D4. \tag{12c}$$

Fig. 7. Block diagram of the circuit that generates the correct bit D4 from the received seven-bit Hamming word.

In this case the right-hand side of Eq. (11) equals

$$\text{CARRY}[\,\text{CARRY}[D4,\ \overline{D4},\ \overline{D4}],\ \ \text{CARRY}[D4,\ \overline{D4},\ D4],$$

$$\text{CARRY}[D4,\ \overline{D4},\ D4]] = \text{CARRY}[\overline{D4},\ D4,\ D4] = D4. \tag{13}$$

Similarly, if the error is on d4, i.e., $d4 = \overline{D4} = D4 \oplus 1$, the right-hand side of Eq. (11) equals

$$\text{CARRY}[\,\text{CARRY}[\overline{D4},\ D4,\ D4], \text{CARRY}[\overline{D4},\ D4,\ D4]$$

$$\text{CARRY}[\overline{D4},\ D4,\ D4]] = \text{CARRY}[D4,\ D4,\ D4] = D4, \tag{14}$$

and if the error is on any one of the parity bits, say, p-(412), i.e., p-(412) = P-(412) ⊕ 1, the right-hand side of Eq. (11) equals

$$\text{CARRY}[\,\text{CARRY}[D4,\ \overline{D4},\ D4], \text{CARRY}[D4,\ D4,\ D4],$$

$$\text{CARRY}[D4,\ \overline{D4},\ D4]] = \text{CARRY}[D4,\ D4,\ D4] = D4. \tag{15}$$

Figure 7 shows the block diagram of a circuit that generates D4. The other bits [D1–D3] occur symmetrically in the seven-bit word and can be found by use of the following additions:

$$d1\text{-}(42) = \text{SUM}[\,p\text{-}(412),\ d2,\ D4\,], \tag{16a}$$

$$d1\text{-}(43) = \text{SUM}[\,p\text{-}(413),\ d3,\ D4\,], \tag{16b}$$

$$D1 = \text{CARRY}[d1,\ d1\text{-}(42),\ d1\text{-}(43)], \tag{16c}$$

$$d2\text{-}(41) = \text{SUM}[\,p\text{-}(412),\ d1,\ D4\,], \tag{17a}$$

$$d2\text{-}(43) = \text{SUM}[\,p\text{-}(423),\ d3,\ D4\,], \tag{17b}$$

$$D2 = \text{CARRY}[d2,\ d2\text{-}(41),\ d2\text{-}(43)], \tag{17c}$$

$$d3\text{-}(41) = \text{SUM}[\,p\text{-}(413),\ d1,\ D4\,], \tag{18a}$$

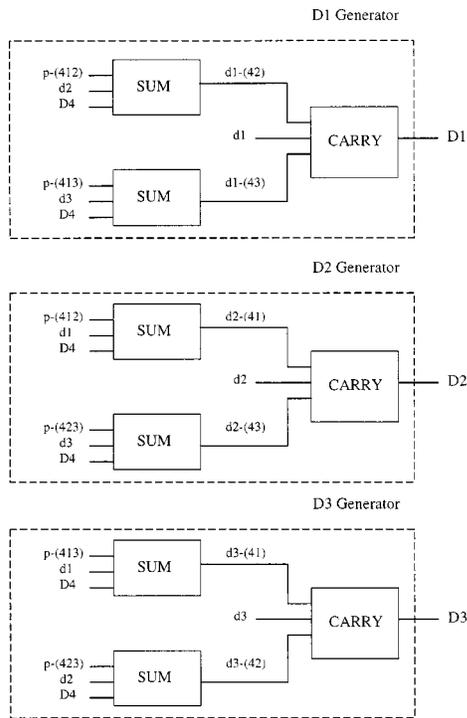$$d3\text{-}(42) = \text{SUM}[\,p\text{-}(423),\ d2,\ D4\,], \tag{18b}$$

Fig. 8. Block diagrams of the circuits that generate the correct bits [D1–D3] from the received seven-bit Hamming word.

$$D3 = \text{CARRY}[d3, d3\text{-}(41), d3\text{-}(42)]. \qquad (18c)$$

It is easy to verify that the bits [D1–D3] are also generated correctly for all possible cases in which the received seven-bit word has at the most one erroneous bit. Figure 8 shows the block diagrams of the circuits that generate the bits [D1–D3] once D4 has been generated.

C. Comments on Generalization

The above examples serve to demonstrate how logic circuits can be designed by use of the polarization properties of ND-FWM. We have also shown that different ND-FWM processes can be used to implement different logic functions simultaneously. Thus it is possible to physically realize useful Boolean operations in terms of triple-product functions by use of nonlinear multiscattering processes, and it is unnecessary to think of generating these operations in terms of two-input gates. It is also possible to build other types of *N*-input building blocks by use of different preprocessing elements and different configurations. A comprehensive study on this issue is beyond the scope of the present paper and will be the subject of a future publication.

3. EXPERIMENT

In this section the dynamic operation of the error-correcting circuit for the (3,1) Hamming code described in Section 2 is tested. Figure 9 shows the optical spectrum at the output of SOA 1 when the three-bit word is (111). The wavelength channels C1, C2, and C3 along with the desired FWM process at ω_{EC} are marked in the spectrum.

A schematic of the experimental setup is given in Fig. 3. Three New Focus external-cavity tunable diode lasers are used to generate the wavelength channels for the three-bit Hamming word. PolSK modulation is achieved by coupling the DATA and $\overline{\text{DATA}}$ outputs of a dual-output Mach–Zehnder electro-optic modulator along the fast and the slow axes of a polarization-maintaining fiber, using an in-fiber polarization beam combiner. To introduce errors, one of the laser sources is connected to modulator 1, and the remaining two sources are connected to modulator 2. Nonreturn-to-zero data streams of 2.5 Gbit/s are generated with a dual-output pattern generator. A variable-delay line is further introduced between the pattern-generator output and modulator 1 to shift the data streams temporally with respect to each other. This enables the addition of random errors on one of the bits of the three-bit word. The entire circuit is built of polarization-maintaining components to preserve PolSK modulation and to add robustness to the setup.

Since the error-correcting circuit is a front-end device operating immediately before detection, it is not necessary to retain PolSK format. This simplifies the optical circuit since only one correcting and one noncorrecting arm are required; i.e., a noncorrecting arm for the case when all the bits are identically "0" is not necessary. A polarizer is introduced after SOA 2 in the correcting arm to convert PolSK modulation to amplitude-shift-keying modulation. The lengths of the two arms in the circuit are synchronized to within 20 ps, which is ~1/20th of a bit period at 2.5 Gbit/s. This reduces undesired overlap between two temporally adjacent three-bit words.

High FWM conversion efficiency is achieved by use of 1.5-mm-long bulk SOA's from Optospeed biased at 650 mA. A high optical signal-to-noise ratio is achieved by fully saturating the SOA's after preamplifying the input channels[21] with high-gain polarization-maintaining erbium-doped fiber amplifiers. The birefringent element is prepared by splicing the principal axes of a polarization-maintaining bow-tie fiber at an angle of 45° on both sides with respect to the principal axes of polarization-maintaining Panda fiber used in the rest of the setup. The length of the bow-tie fiber is 75 cm. The birefringent element is temperature controlled to enable tunability and increased stability. The wavelengths for C1 and C2 are 1547.43 nm and 1547.85 nm (the birefrin-
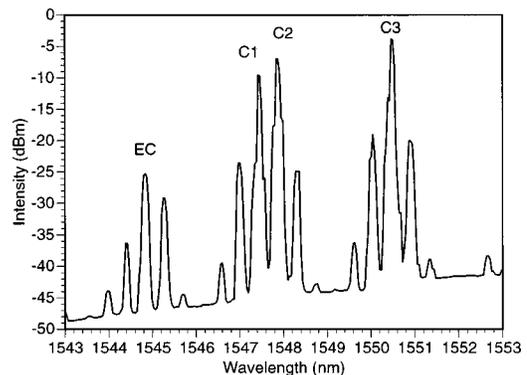

Fig. 9. Optical spectrum at the output of the SOA showing wavelength channels [C1–C3] and EC (in 0.1-nm resolution bandwidth).
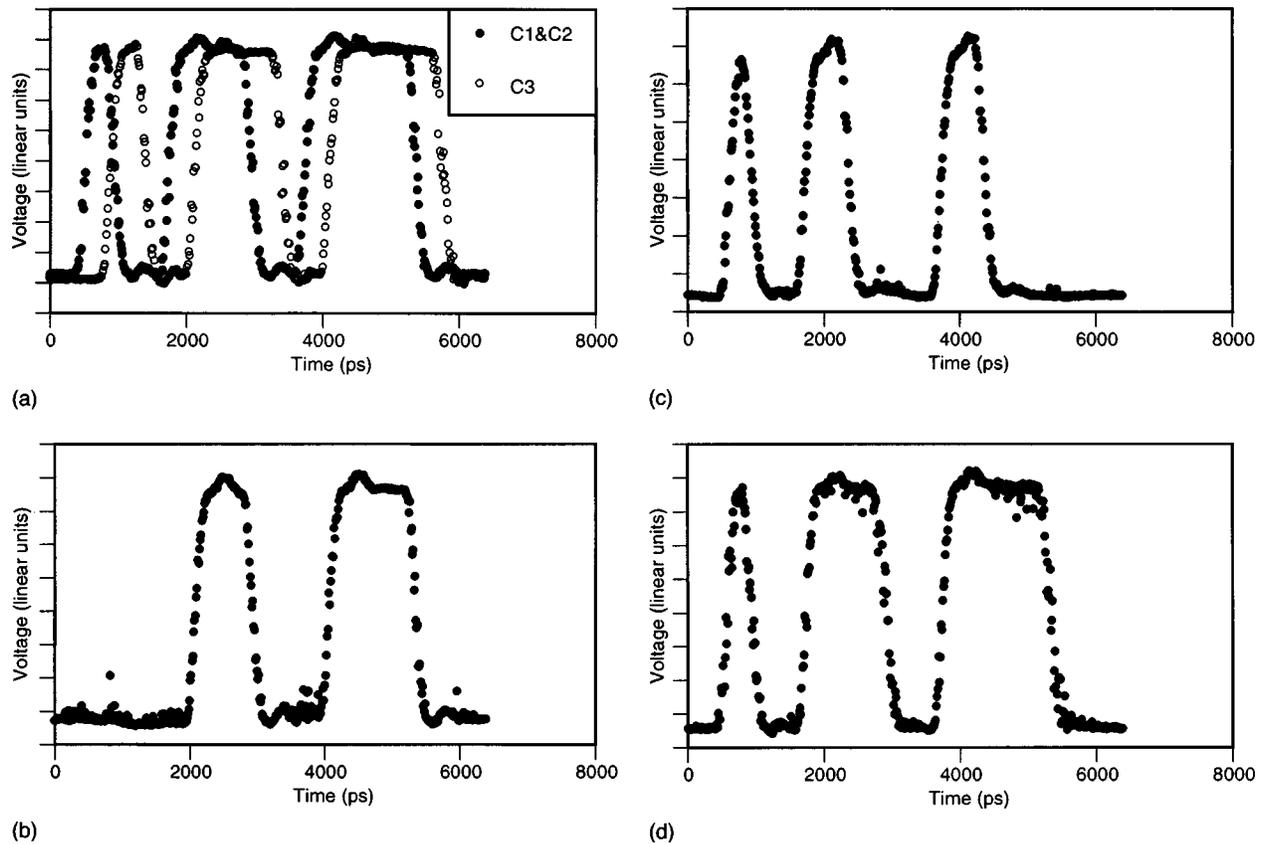
Fig. 10.   Oscilloscope traces of (a) 16-bit patterns on channels C1, C2, and C3 at 2.5 Gbit/s, (b) EC output from the noncorrecting arm, (c) EC output from the correcting arm, and (d) EC output from both arms combined.

gent element is almost a full-wave plate), and that of C3 is 1550.47 nm (the birefringent element is a half-wave plate).   Note that the SOA in the correcting arm is always saturated since there is always power incident upon it.   However, the SOA in the noncorrecting arm is not saturated when all the bits are identically "0," as the polarizer before it does not allow any channel to pass through and be amplified.   This leads to a modulation of amplified spontaneous emission from SOA 1 because its gain recovery time is comparable with the bit rate.   Thus an additional cw laser is coupled into SOA 1, which is called the saturating-wave laser (see Fig. 3).   Its power is adjusted such that it is low compared with the power in the other channels but high enough to ensure saturation of SOA 1.   The laser's wavelength is carefully selected at 1558.5 nm so that the additional FWM sidebands that it generates do not interfere with the EC channel.

The SOA's are further tested for mode-conversion effects,[22] which would lead to a degradation of the extinction ratio of the PolSK signals.   TE-polarized light is launched into the SOA's operating under conditions identical to those used in the experiment.   With another polarizer at the output of the SOA's, the TM component is found to be at least 30 dB lower than the TE component, which is of the same order as the extinction ratio of the polarizes used in the measurement.   For TM-polarized light launched into the SOA's the TE component at the output is also found to be at least 30 dB lower than the

TM component.   Hence we conclude that mode conversion is not significant in the devices used in this experiment.

The output from each arm is combined by use of a polarization-maintaining coupler.   Spurious interference can occur between the two arms owing to the presence of power in the EC channel originating in the arm where the FWM is not supposed to occur.   This is because the state of polarization on each channel is not perfectly linear along the fast or the slow axis of the polarization-maintaining fiber, leading to a residual power in the orthogonal direction.   This interference is minimized by coupling the EC channel in each arm to the orthogonal axes of the polarization-maintaining fiber.   The error-corrected channel is filtered optically with a 1-nm-wide tunable bandpass filter and is detected with a preamplified receiver.

4.   RESULTS AND DISCUSSIONS

Figure 10(a) shows a 16-bit pattern [1001110011110000] at 2.5 Gbit/s on each channel.   The variable time delay is adjusted so that there is a one-bit delay on C3 relative to C1 and C2.   Thus C3 is the channel that has occasional errors.   The resultant patterns on ω_{EC}, which are obtained from the noncorrecting and the correcting arms separately, are shown in Figs. 10(b) and 10(c), respec-

tively. Figure 10(d) shows the pattern on ω_{EC} after both arms have been combined and is identical to the pattern on C1 and C2. This shows that the data stream with errors was corrected.

We further demonstrate the dynamic operation of this circuit by modulating C1, C2, and C3 with a pseudo-random-bit stream ($2^7 - 1$), with a one-bit delay on C3 relative to C1 and C2. In this case the binary state on C3 is complementary to the state on C1 and C2 approximately 50% of the time. Figure 11(a) shows the bit error rate (BER) versus received power (in 0.5-nm resolution bandwidth) of the EC channel for this case. This is compared with the case when there are no errors on C3 relative to C1 and C2. Detection with a low bit error rate, $<10^{-9}$; is demonstrated despite a 50% error rate on the
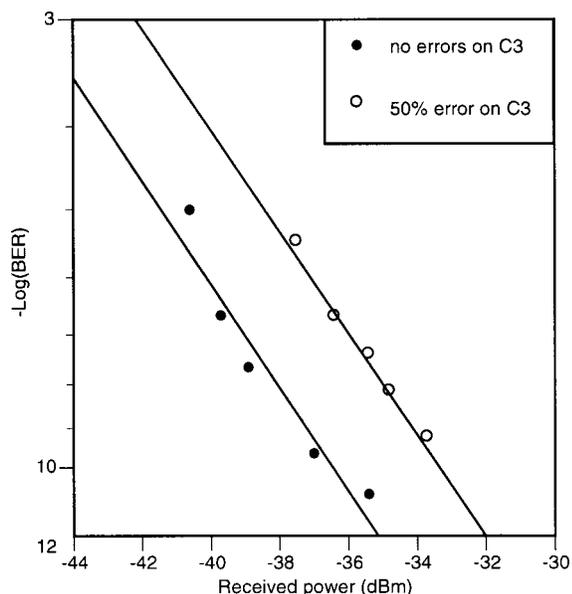
(a)
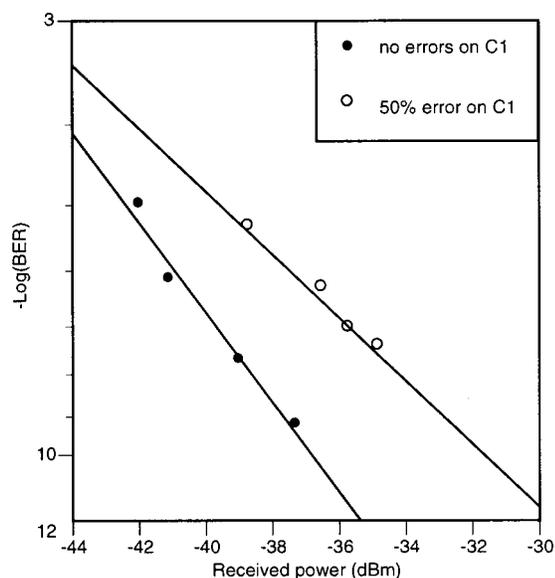
(b)

Fig. 11. Bit error rate versus received power (in 0.5-nm resolution bandwidth) at 2.5 Gbit/s for (a) random errors on C3 and (b) random errors on C1.
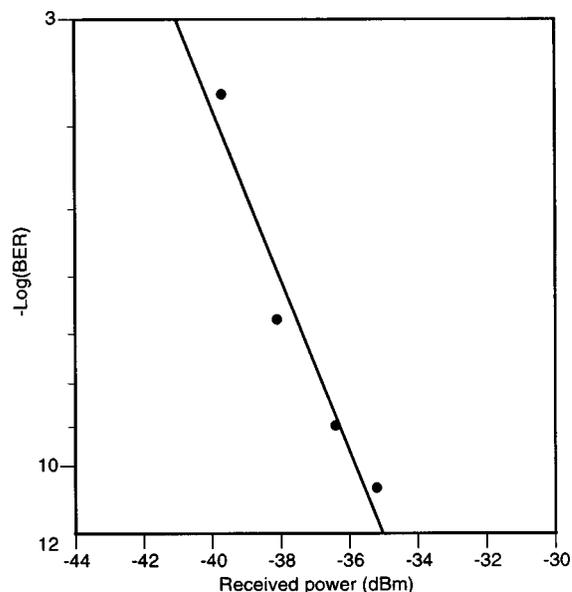

Fig. 12. Bit error rate versus received power (in 0.5-nm resolution bandwidth) at 2.5 Gbit/s for error correction on ill-defined states with 30% errors on C3.

received word. Similar results are obtained by modulating C1, C2, and C3 with pseudo-random-bit streams with a one-bit delay on C1 relative to C3 and C2, in which case the binary state on C1 is complementary to that on C2 and C3 approximately 50% of the time. The bit error rate for this is shown in Fig. 11(b). The slight degradation after error correction in Fig. 11(b) compared with Fig. 11(a) can be explained by the lowering of FWM efficiency in the correcting arm when C1 and C2 are orthogonal compared with when C1 and C2 are parallel, as determined by relation (4).

The operation of the logic circuit is further tested when the information on C3 is severely distorted, so that a bit error rate no better than 30% could be achieved on C3. This is achieved by changing the dc bias of the Mach–Zehnder modulator. Thus the information on C3 is ambiguous in that there are no clearly defined binary states on it. Pseudo-random-bit streams on C1 and C2 were detected to be error free upon transmission through the circuit. Figure 12 shows the bit error rate versus received power on the EC signal for this case. Once again a low bit error rate of $<10^{-9}$ on the mixing signal for ambiguous data on C3 and error-free data on C1 and C2 is demonstrated. This shows that error correction on certain ill-defined states is also possible.

The experimental feasibility of cascading such circuits remains to be investigated. Issues such as the strength of the nonlinearity present in the devices used will determine the conversion efficiencies and optical signal-to-noise ratios of the FWM signals involved. The degradation of the extinction ratio of the PolSK signals owing to mode-conversion effects in these elements will affect the performance of these circuits and should be minimized. The results will be especially important in the design and implementation of more-complex logic gates involving several Boolean operations, e.g., the decoding circuit for higher-level linear codes, such as the (7,4) Hamming code.

5. CONCLUSIONS

We have shown that FWM on PolSK-coded bits can be used to construct certain higher-level logic elements without resorting to the standard two-input gates. Taking the simple example of the (3,1) Hamming code, we have demonstrated on-the-fly error correction on severely distorted data. The data are recovered with a bit error rate of $<10^{-9}$. To the best of our knowledge, this is the first demonstration of a fiber-optic logic circuit that performs signal processing on more than two input channels simultaneously. The bit rate of the experiment was limited to 2.5 Gbit/s by the bandwidth of the modulators. Since FWM is an ultrafast nonlinearity, the error-correcting circuit can be made to perform at much-higher bit rates. We have also shown that several ND-FWM processes can be used to perform different triple-product logic operations simultaneously, and this can simplify the design of the encoder circuit for the (7,4) Hamming code. Finally, we would like to point out that the error detection and correction schemes have been taken merely as examples to demonstrate the potential offered by use of the polarization-selection rules of ND-FWM processes to implement optical logic.

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