Macroscopic and microscopic studies of electrical properties of very thin silicon dioxide subject to electrical stress

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The electrical characteristics of various size tunnel switch diode devices, composed of Al/SiO_2/n-Si/p^+-Si layers, which operate with a range of parameters (such as current densities in excess of 10^4 A/cm^2) that stress the oxide layer far beyond the levels used in typical thin oxide metal-oxide semiconductor research have been examined. It is found that the first time a large current and electric field are applied to the device, a ''forming'' process enhances transport through the oxide in the vicinity of the edges of the gate electrode, but the oxide still retains its integrity as a tunnel barrier. The device operation is relatively stable to stresses of greater than 10^7 C/cm^2 areally averaged, time-integrated charge injection. Duplication and characterization of these modified oxide tunneling properties was attempted using scanning tunneling microscopy (STM) to stress and probe the oxide. Electrical stressing with the STM tip creates regions of reduced conductivity, possibly resulting from trapped charge in the oxide. Lateral variations in the conductivity of the unstressed oxide over regions roughly 20–50 nm across were also found. © *1997 American Vacuum Society.* [S0734-211X(97)06904-7]

I. INTRODUCTION

The continuing drive to decrease the characteristic dimensions of metal-oxide semiconductor-field effect transistors (MOSFETs) in modern integrated circuits has fueled basic research of metal-oxide semiconductor (MOS) structures with very thin (<3.5 nm) silicon dioxide layers. Studies of current-voltage (I-V) and capacitance voltage (C-V) characteristics,[1–7] as well as more basic surface studies using x-ray photoemission spectroscopy (XPS)[4,8,9] and ballistic electron emission microscopy (BEEM),[10–12] have greatly enhanced our understanding of current transport through these oxides, the chemical nature of the Si–SiO_2 interface, and the effects of electrical stressing. However, as the bulk of this work has been aimed at studying the future of the MOSFET, few studies have attempted to stress thin oxides (<3.5 nm) with very high current densities ($>4\times10^3$ A/cm^2). While an oxide that has been degraded with electrical stress is no longer usable in a MOSFET, it has not become an electrical short,[2,4] and may be useful in other devices. Studies of such devices may prove useful in understanding the intrinsic properties of the oxide and its role in the operation of any device.

Consider the tunnel switch diode (TSD) device discovered by Yamamoto *et al.*[13] [Fig. 1(a)], which has been proposed as a candidate for power switching, logic, and memory applications.[14–16] The device consists of a p-n junction in series with a MOS junction, yielding a thyristorlike I-V characteristic shown in Fig. 1(b), consisting of two stable current states for a range of voltages. It has been demonstrated theoretically[15] and experimentally[17,18] that this device relies critically on the oxide as a tunnel barrier. If the oxide is either too thin or too thick, the peak in the I-V curve disappears, and there are no bistable current states for any range in voltage. A comparison (Table I) of typical operating parameters of TSD devices produced in our laboratory with thin oxide MOS research parameters[3] indicates that the TSD clearly operates in a parameter space far removed from that of the MOSFET, stressing the oxide far beyond the point at which the MOSFET fails.

In this article we present electrical studies of the TSD device, focusing on the role of the oxide and its ability to perform a critical role under heavy stress. By measuring the I-V characteristics of various size devices both before and after stress has been applied to the device, we find that initial stress causes a ''forming'' process, leading to nonuniform current transport through the device, but that further stress produces little or no change. This suggests a local modification of the oxide tunneling properties. In an attempt to create and characterize similar locally stressed regions in a somewhat simpler system, we examine a simple SiO_2–Si interface using atomic force microscopy (AFM) and scanning tunneling microscopy (STM).

II. TSD STUDIES

A. Basic device operation

While the behavior of the TSD device is not completely understood, the generally accepted basic mechanisms leading to the thyristorlike I-V curve are described in detail elsewhere.[14,15,18,19] Here we will only give a brief description of the device operation and the role of the thin oxide barrier.

The device is most easily described as a p-n junction and an MOS junction in series. If positive bias is applied to the gate electrode, the I-V curve is dominated by the reverse biased p-n junction and contains no unusual features. As negative bias is applied to the gate electrode, the MOS junction depletion layer begins to extend into the n-Si layer [Fig.

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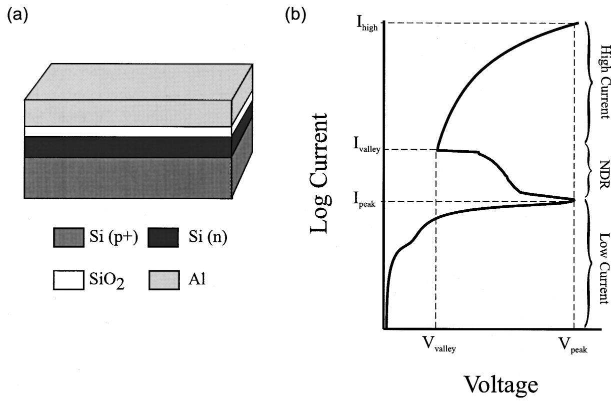

FIG. 1. Tunnel switch diode (TSD). (a) The TSD device consists of a $p+$ silicon substrate with an n silicon epilayer, typically a few microns thick, a tunnel oxide (10–40 Å), and a conductive (e.g., Al) gate on top. (b) A typical measured I-V curve for a 150×150 μm^2 device. For this particular device, I_{high}=100 mA, I_{valley}=0.1 mA, I_{peak}=0.009 mA, V_{valley}=1 V, and V_{peak}=4 V.

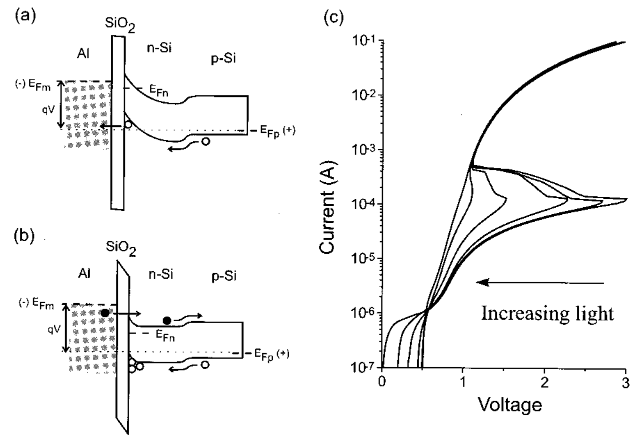

FIG. 2. (a) A band diagram of the TSD in the low current state just below the peak voltage. Further bias will extend the MOS junction depletion layer, forward biasing the p-n junction. E_{Fm}, E_{Fn}, E_{Fp} and V are the metal Fermi level, electron quasi-Fermi level at the SiO_2/n-Si interface, the Fermi level in the flat band region of the p-Si substrate, and the applied bias, respectively. (b) A band diagram of the TSD in the high current state. The hole inversion layer maintains the majority of the applied bias across the oxide, while electrons tunneling through the oxide and holes injected from the p-Si layer keep the n-Si layer highly populated, but nearly charge neutral. (c) Measured I-V curves of a 150×150 μm^2 device for different intensities of injected light.

2(a)]. In this state, the current is low, limited by the reverse-biased depletion layer, and the bulk of the bias is dropped across this layer. Once the depletion layer reaches the p-n junction depletion region, however, further bias causes the p-n junction to be turned on, flooding the n-Si layer with holes. If the oxide layer is not too thin, the holes will accumulate in the n region, creating an inversion layer. This shifts the bulk of the bias from the depletion layer to the oxide [Fig. 2(b)], causing a large increase in tunnel current, provided the oxide layer is not too thick. This, in turn, causes the Fermi level in the n-Si layer to be pulled up, forward biasing the p-n junction even more. This positive feedback mechanism switches the device into the high current state, in which the n-Si layer is nearly charge neutral, highly populated by both holes and electrons, with a hole inversion layer at the surface providing the large field across the oxide. This state can only be supported as long as the oxide is thin enough to allow large tunnel currents, but thick enough to support the hole inversion layer.

Other mechanisms can be employed to switch the device from the low to high current states. For example, light injection into the n-Si layer causes electron-hole pairs to be produced, setting up the necessary carrier distribution in the n-Si layer at a much lower bias.[13] In Fig. 2(c), we see that increased light injection intensity results in a decrease in the peak voltage of the TSD, until eventually the peak disappears completely. Charge injection via a third terminal, connected to the n-Si layer, results in a similar modification of the I-V characteristic.[14,19]

TABLE I. A comparison of maximum stress operating parameters of the TSD devices produced in our labs with those of current thin oxide MOS research structures (see Refs. 2 and 5). For the purposes of a rough comparison, we define "Q_{max}" as the areally-averaged maximum fluence of charge that results in a nonfunctioning device, and we compare this with Q_{bd} in MOS devices. As our time-tested TSD devices did not expire in the course of our testing (Fig. 3), we can only give a lower bound on this number.

	t_{oxide} (Å)	Q_{max}, Q_{bd} (C/cm^2)	J_{oxide} (A/cm^2)	Electric field (MV/cm)
TSD	<35	>10^7	>10^4	10–20
MOS	30–60	<10^5	<10	<15

B. Experimental procedures

The details of the device fabrication and measurement are described elsewhere[17], so we will only reproduce a summary here. Chips approximately 1×1.5 cm^2 were cleaved from commercially obtained wafers consisting of a p-type (3 $\times 10^{18}$/cm^3) silicon (100) substrate and an n-type (2 $\times 10^{15}$/cm^3) epilayer approximately 1.5 μm thick. After cleaning, thin sacrificial oxide layers were grown on the chips in a rapid thermal processing (RTP) oven in O_2 for 60 s at 900 °C. During ramp-up and anneal in the oven, the chips were held in an Ar ambient. The sacrificial layers were stripped off in a buffered oxide etch (BOE), and another oxide was grown, again at 900 °C in O_2. The thickness of this oxide was controlled by varying the O_2 flow time. Samples with a flow time of 15, 30, 45, and 60 s were produced. The oxide thicknesses of these samples were estimated to be 1.5, 1.8, 2.1, and 2.5 nm, respectively, by measuring the thickness of the 60 s sample using standard C-V techniques and extrapolating along published calibration curves[20,21] to the smaller thicknesses. As these values are only estimated and not measured, we will refer to the samples by the controlled O_2 flow time rather than the thickness. We note that the thickness estimation[17] is calibrated using C-V measurements which have been reported to yield values roughly 0.9 nm less that those given by optical techniques such as ellipsometry when metal gates are used.[22] Aluminum contacts were deposited on both the front and

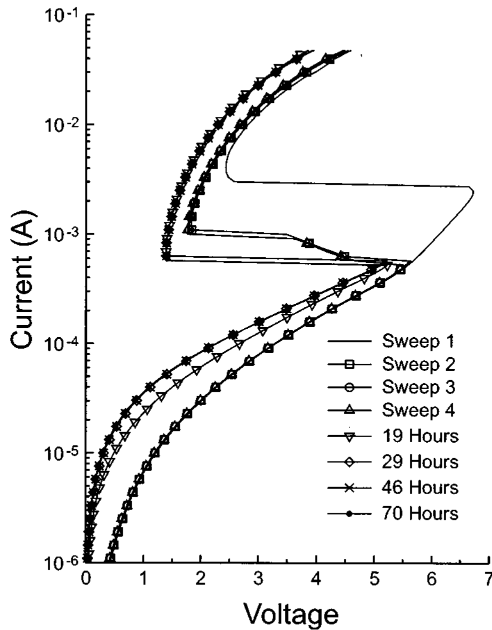

FIG. 3. Effect of stress on TSD I-V curve over time. The first four sweeps represent the ''virgin'' scan, taken the first time bias was ever applied to the device, and the three subsequent scans. The remaining curves were taken after the indicated number of hours of stress.

back of the chip. Discrete devices were defined by lithographically etching the top Al surface into squares of various sizes.

The device I-V curves were measured at room temperature by placing the chips on a conductive chuck of a probe station, contacting the top Al pads with a tungsten probe tip, sourcing current to the device over an exponential range, and measuring voltage. Light from a lamp directed through a microscope connected to the probe station could be injected in the device with varying intensity in order to modify the I-V curve as shown in Fig. 2(b) and described above.

C. Results and discussion

In this section we discuss properties of the TSD I-V curves that may be related to the transport properties through the oxide layer. In particular, we explore two general characteristics of the devices: an initial ''forming'' behavior, and the scaling of the current with device size.

We have observed, as have others,[18] that the first time a large enough bias is applied to force the device into the high current state, the I-V curve appears to change noticeably, but subsequent stressing of the device results in very little change. In Fig. 3, we show several scans taken on a single 150×150 μm device: a ''virgin'' scan taken before any bias had been applied to the device, three additional scans taken immediately thereafter, and four subsequent scans taken after the device had been continuously ramped from negative to positive bias at 60 Hz for the indicated total number of hours. The ac stress was designed to continuously cycle the device back and forth from the high current state to the low current state in order to determine whether switching between states would cause further degradation. We would expect that degradation of the oxide would be similar for unipolar stressing as the p-n junction limits the current in the reverse bias, and therefore little voltage is dropped across the oxide. Note that the ''virgin'' scan exhibits a much higher peak voltage than all subsequent scans, but that no other sudden changes in the I-V curve are apparent. We suggest that the initial stress could be causing a modification of the oxide. We will return to this point shortly.

We have also observed that the I-V characteristics of different size devices have not scaled with area as would be expected if the current density were uniform. Typical I-V

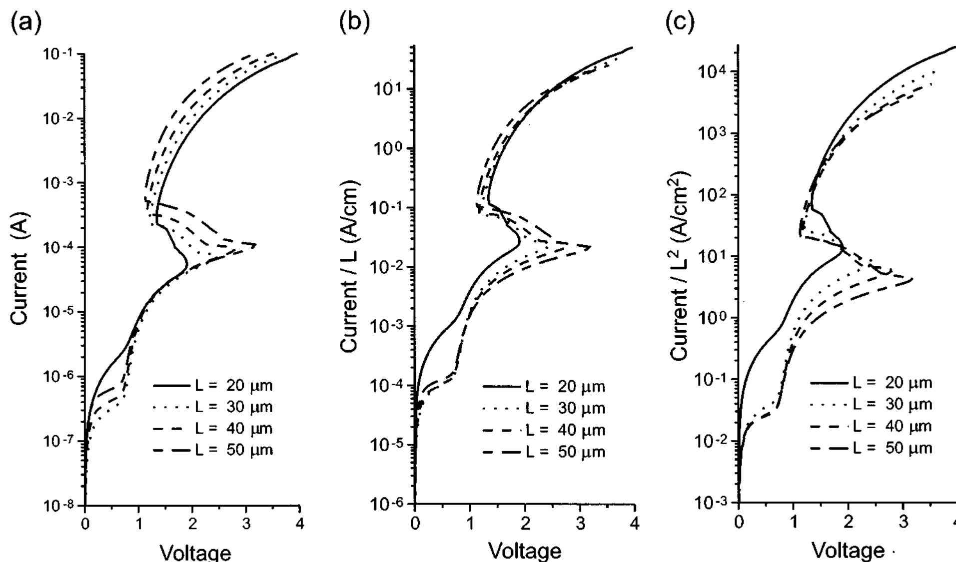

FIG. 4. Scaling behavior of the TSD device. Typical I-V curves for square devices ranging in size from 20×20 μm^2 to 50×50 μm^2 plotted as (a) current/L^0, (b) current/L^1, and (c) current/L^2, where L is the length of the side of the device (i.e., 20, 30, 40, and 50 μm).

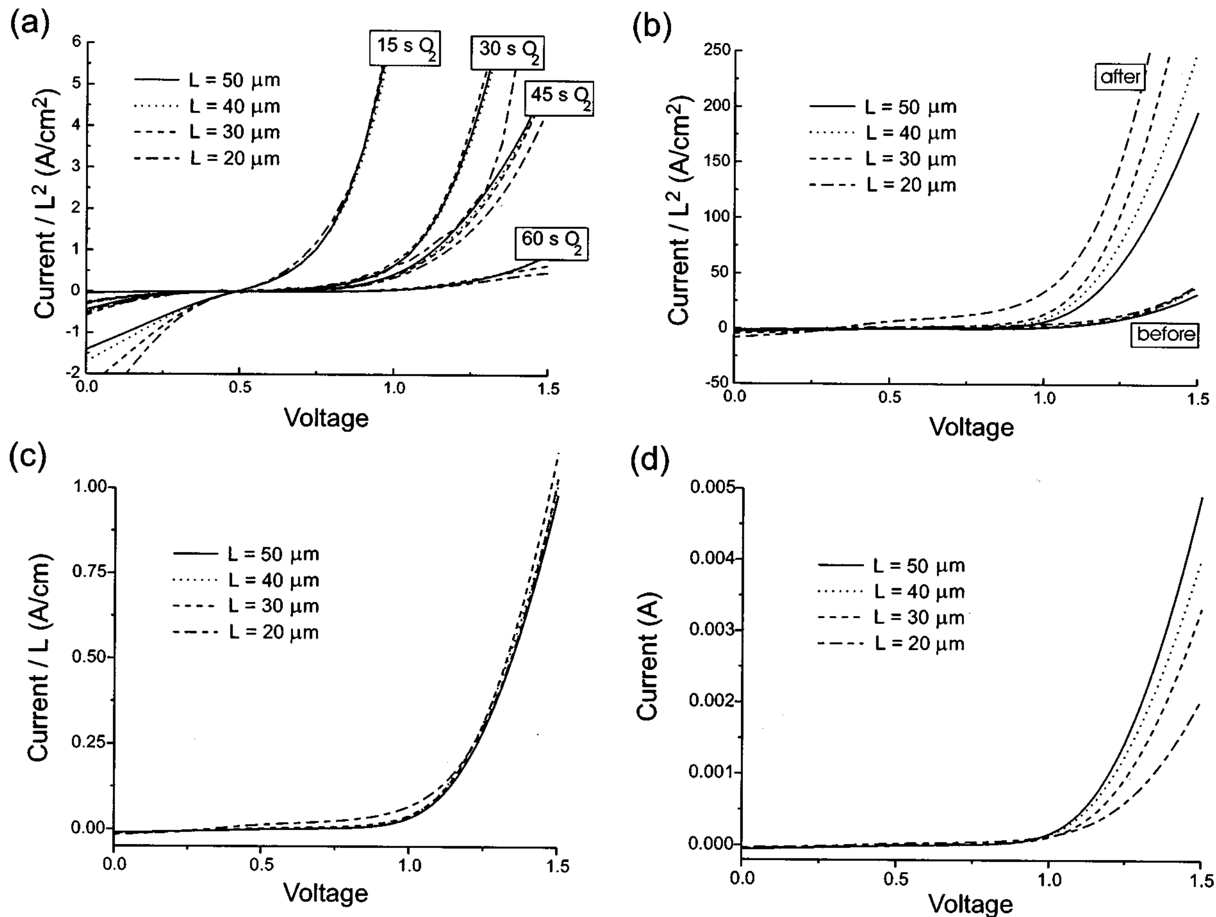

FIG. 5. Low voltage scaling behavior of the TSD with light injection. (a) ''Virgin'' J-V curves taken before the devices had ever been subjected to high field stress. Devices of four different sizes are shown in groups corresponding to samples with different oxide thicknesses. Each group collapses to nearly the same current density, suggesting a uniform current density. (b) J-V curves for a group of different size devices on the 30 s O_2 sample taken both before and after high field stress. The ''after'' curves are also plotted as (c) current/L^1 and (d) current/L^0 in order to illustrate the modified scaling behavior.

curves for devices of a range of sizes on the 30 s O_2 sample are shown in Fig. 4, scaled by the length (L) of the edge of the square Al contact that defines the active area of the device, raised to the powers 0, 1, and 2. If the current density through the device were uniform, the current/L^2 curves shown in Fig. 4(c) would collapse to a single curve, but we see that different parts of the I-V curve appear to scale with different powers of L. For example, the low current region just below the peak seems to be independent of area, while the high current region above the peak seems to scale more nearly linearly with L than as any other integral power, suggesting an edge effect. It is possible that parasitic resistances could play a role in the high current region, but this would typically result in a current independent of area.

In order to determine whether the oxide plays a role in this scaling behavior, we would like to isolate its contribution to the I-V curve. As described above and illustrated in Fig. 2(c), light injection causes the peak voltage to be reduced and, if intense enough, can eliminate the peak altogether, effectively forcing the device into the high current state at any bias. In this state, the current through the device is primarily controlled by oxide tunneling as the majority of the bias falls across the oxide. Therefore, with high enough light injection, we can effectively examine the I-V characteristic of the MOS junction even at low bias.

Using this light injection technique, we examined the MOS part of the device under low bias both before and after the device had been subjected to the stress of the high bias, high current regime that forces the ''forming'' process. The light level was set to completely eliminate the peak in the I-V curve. In Fig. 5(a), we plot pre-stress current density voltage (J-V) curves for four different size devices on each of four chips with different O_2 flow times during oxidation, and hence different oxide thicknesses. We see that the curves very nearly collapse into four groups corresponding to the four different thicknesses, suggesting nearly uniform current density through each of the oxides. While the curve corresponding to the 20 μm device on the 30 s O_2 sample does not quite coincide with the other curves for this sample, it is possible that the probe tip scraped off part of the Al pad, resulting in a smaller effective area.

In Fig. 5(b), we plot similar J-V curves of a set of different size devices on the 30 s O_2 chip under illumination both before and after the devices had been stressed. This stress

was achieved by connecting the devices to a curve tracer and, for a few seconds, switching from negative to positive bias at 60 Hz to a maximum positive bias current of 100 mA. We see, first of all, that the (average) current density through the devices increased by over an order of magnitude after stressing. We also note that the currents no longer scale with L^2. In fact, we see by comparing Figs. 5(b), 5(c), and 5(d), that the current most closely scales linearly with L. We suggest that the oxide may be forming locally near the edges of the device where the electric field is somewhat higher. Similar behavior was observed for the 15, 45, and 60 s O_2 samples.

It is not surprising that our device geometry would produce edge effects, and it is probable that such effects could be minimized with a different device geometry, for example by extending the gate electrode across a thicker field oxide surrounding the device, or by using a guard ring. The interesting result, however, is that in the presence of the locally enhanced field around the edge of the device, the ''formed'' oxide is relatively stable under continued stress. As can be seen in Fig. 3, after the ''forming'' process, the device can be operated for long times with little modification of the peak or valley voltages at stresses far exceeding acceptable MOS values (Table I). Others have observed similar long lifetimes in these devices after an initial ''forming.''[13,18] Even though this forming process greatly enhances carrier transport through the oxide locally, the oxide layer must still be functioning as an effective barrier, or the peak region of the I-V curve would disappear as described earlier.

While these results reflect a local modification of the device oxide, it is difficult to extract the oxide properties from the functions of the TSD, which is not completely well understood, in a geometry which clearly produces nonuniform transport. It would be interesting to study a simpler system with many of the same properties to see if it exhibited similar local modifications of the oxide. For these reasons, we attempted to mimic the high field local stress produced by the edge of our TSD devices with tunnel current injected from an STM tip through a thin oxide on a simple silicon substrate as described in Sec. III.

III. LOCAL PROBE STUDIES

A. Introduction

Scanning tunneling microscopy (STM) allows one to take spatially resolved measurements of the tunnel current flowing from a sharp tip to a sample surface.[23,24] On conductive samples made of a single material, the tip may be brought to within angstroms of the surface and held at a constant voltage while the tip is raster scanned over the surface and its height modulated to maintain a constant tunnel current, effectively yielding a physical contour plot of the surface down to atomic dimensions. Similarly, on flat surfaces comprised of materials differing in conductivity, the STM may be used to generate a conductivity contour plot of the surface.[25,26] The atomic spatial resolution of the STM makes it an attractive tool for the study of conducting and semiconducting samples. Insulating samples, on the other hand, do not generally allow a sufficient tunneling current to flow for adequate tip response resulting in frequent tip crashing, and therefore do not lend themselves as readily for STM study.

Thick layers of silicon dioxide would normally fall into the category of materials for which STM is not a useful tool. However ultrathin (<3.5 nm) layers of silicon dioxide, such as those used in the TSD, allow sufficient tunneling current to make STM a viable tool for examining local conductivity. Others have been able to study ultrathin oxides in experiments with beam assisted scanning tunneling microscopy (BASTM),[27] with BEEM,[10,12,28] and with STM of thinner oxides.[25,29] We have found that by operating at high tip voltages (1–5 V) and lower than usual tunneling currents (1–5 pA), the tip may be rastered over the silicon dioxide surface, yielding an image without crashing. The image obtained in this fashion represents some convolution of the silicon surface contour, the silicon dioxide surface contour, and any variations in the local conductivity of the silicon dioxide layer. We have attempted to characterize the local conductivity of our thin oxide layer with these STM images, comparing them with topological AFM images of our sample before and after oxidation. Furthermore, since the nature of STM is to inject large local current densities, we have also attempted to look at the effects of localized electrical stressing on the thin oxide layer.

B. Experimental details

Samples were produced using boron doped p-type (100) silicon wafers (00.00425–0.00575 Ω cm) cleaved into square chips $\sim$1 cm on a side. These chips were subject to a standard acetone, isopropyl alcohol, de-ionized water degrease in ultrasound. The chips were then etched in 10:1 HF solution to remove any oxide, and a grid of circles 2 μm in diameter, 5 μm apart, was patterned onto the chips. Chemically assisted ion beam etching (CAIBE) was employed whereby 50 sccm of chlorine gas was used to react with the bare silicon surface while a beam of xenon ions was used to sputter the chlorine-reacted silicon for 15 s. After another degrease, the bare patterned silicon surface was then examined on a Digital Instruments Nanoscope III MultiMode AFM. The chips were then degreased once again and dipped in 10:1 HF acid to remove any residual oxide. An AG Associates Mini-pulse rapid thermal Processor (RTP) was used to bring the chips up to 900 °C in ultrapure argon. Device quality oxide was then grown by exposing the chips to ultrapure oxygen at 900 °C for 15–30 s followed by an anneal in ultrapure argon for 30 s at 900 °C. Immediately following oxidation, the chips were mounted with conductive silver paint onto magnetic pucks for use with the AFM/STM and allowed to dry for 20 min.

After drying, the thickness of the oxide layer was measured on a J. A. Woollam variable angle spectroscopic ellipsometer (VASE). Data was taken at 70°, 75°, and 80° angles of incidence across wavelengths from 205 to 365 nm. The thickness was computed using bulk SiO_2 optical constants to be 34–35 Å thick for the grown RTP oxides. AFM surface images of the samples were taken in ambient both to image

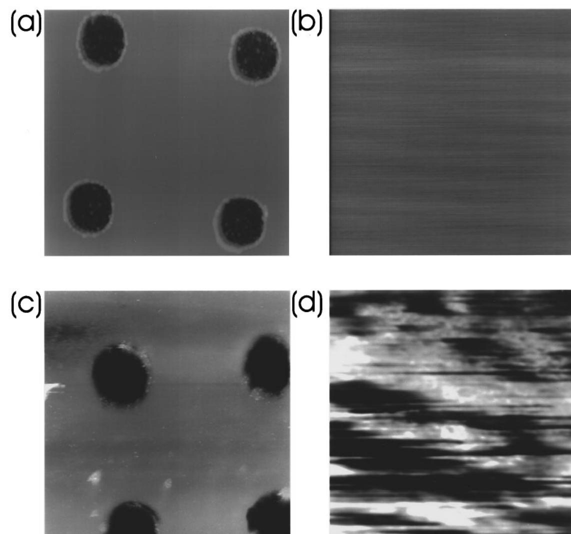

FIG. 6. Comparison of AFM and STM scans of p-type Si with a 34 Å RTP grown oxide. Large scale scans (10 μm, 50 nm light to dark) show the patterning of the chips in (a) an AFM scan and (c) an STM scan (4.3 V, 3.3 pA). Small scale scans (100 nm, 5 nm light to dark) taken in unpatterned areas show (b) the surface roughness in the AFM scan, and (d) the lateral variance in conductivity in the 1.0 V, 2.0 pA STM scan.

the large scale patterning (10 μm square) and the oxide surface in the unpatterned regions (100 nm square). The samples were then moved to a similar STM setup in ambient with a picoamp boost stage for use at low currents, and a variety of STM scans were taken over a period of several hours. Following study with the STM, the surface was again examined with the AFM and the oxide thickness was again measured on the ellipsometer.

We attempted to quantify the effects of atmospheric exposure on the RTP grown oxide due to native oxide growth and accumulation of atmospheric moisture or other contaminants. Unpatterned samples were degreased, etched, and oxide layers were grown in the RTP in a similar fashion to the patterned samples. Timed thickness measurements taken over periods of 10–15 h in ambient exhibited linearized growth rates on the order of 0.2 Å/h. This correlates well with the ellipsometric observed change in thickness of several angstroms over the time of the STM scanning.

C. Results and discussion

The AFM was used to examine the topological contour of chips both before and after oxidation. Before oxidation, the bare silicon surface was examined both to verify that the patterning was successful and to quantify the silicon surface roughness. Section linescans of the plots showed the silicon surface to have local roughness on the order of 1 nm. Post-oxidation Si–SiO_2 interface roughness has been found to be less than 1 nm by others.[30] After RTP oxidation, the AFM was again used to image the patterning and surface roughness. Figure 6 shows typical AFM scans of both the large scale patterning and small scale roughness of the RTP thin oxide layer. Figure 6(a) shows the large scale patterning image, found to have patterned hole depths of 18 nm. Figure 6(b) shows a 100 nm scan of the RTP oxide surface roughness. Line scans of the 100 nm image show small scale roughness to be less than 1 nm in the unpatterned areas of the chip.

The STM was then used to look at the electrical contour of the RTP thin oxide layer. An initial attempt was made to image the surface in a constant-height mode, looking only at local changes in tunneling currents without allowing the tip to respond to the surface. However, the very dramatic changes in current across our oxide resulted in extreme noise, frequent tip crashes, and an irreproducible image. In constant-current mode, we are assured that if the sample is uniformly conductive, the surface image will reproduce that of the AFM. By comparing our image with the AFM, we are able to distinguish differences in conductivity in the oxide layer from topological features. The STM images were taken at relatively high voltages (1–5 V) and low currents (1–5 pA) to keep the tip sufficiently far away from the surface to avoid crashing and also to drive sufficient tunnel current through the oxide for adequate feedback. This high voltage low current imaging was done at the expense of lateral resolution, but was necessary to generate repeatable scans. Similar setpoint voltages with nanoamp currents have been used by others in STM experiments with thinner oxides,[25,29] as well as BASTM,[27] and BEEM[10,12,28] experiments.

Initially the chips were scanned over 10 μm to image the patterned circles to verify that our scan parameters were producing a reliable image. Figure 6(c) shows a typical large scale STM image (4.3 V, 3.3 pA) of the patterned surface on the same scale as the corresponding AFM image in Fig. 6(a). The images of the patterned circles show depths of 18.5 nm in excellent agreement with the AFM scan, well within expected variation in etch depth across the sample. Having established that the STM is producing a reliable image of the oxidized chip, the scan size was reduced to look at local variations in the oxide. Figure 6(d) shows a 100 nm STM image (1.0 V, 2.0 pA) of the oxide layer on the same scale as the corresponding AFM image in Fig. 6(b). Line scans show apparent height variations on the order of 5 nm across areas 20–50 nm in size. The dramatic difference in the images taken with AFM and STM, coupled with the AFM verified flat topology, suggest that there are significant lateral variations in conductivity across the oxide. In order to verify that these images represented true surface features, we attempted to reproduce them with a variety of scan parameters. Surface features were relatively reproducible under changes in scan rate, direction, and area. Figure 7 shows a representative series of STM images (1.5 V, 3.0 pA) ranging in size from 1 μm to 100 nm on the same unpatterned section of RTP oxide. Apparent height variations in all four images are on the order of 5 nm with feature size on the order of 20–50 nm laterally in all images. Lateral variations in conductivity similar in size and magnitude were seen across a number of different scans and chips.

Note that in the interpretation of these variations as conductive rather than topological features, we require a tip-sample separation of at least 5 nm. This is considerably

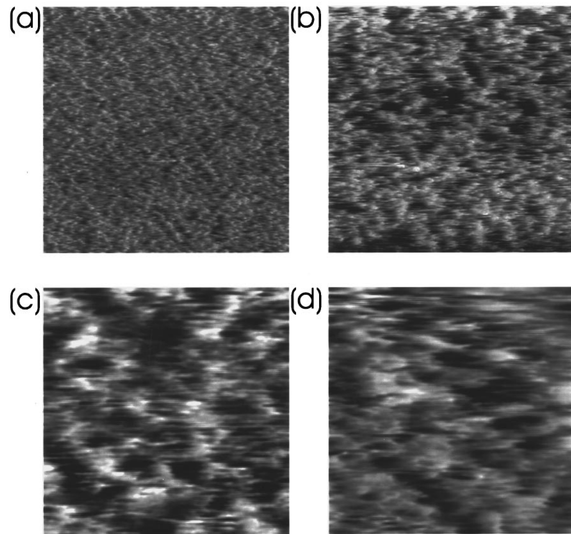

FIG. 7. Zoom in sequence of STM scans (1.5 V, 3.0 pA) over an unpatterned area of 34 Å RTP oxide on *p*-type Si. Lateral variations in conductivity can be seen over the sequence of scans: (a) 1 μm, (b) 500 nm, (c) 250 nm, and (d) 100 nm scans. Light to dark variation in the scans is 5 nm.

larger than the distances typically assumed in vacuum STM setups, and would suggest that the tip current in our experimental setup is considerably less sensitive to tip-sample distance. This is a reasonable assumption for ambient STM; accumulation of moisture and atmospheric contaminants on the tip and sample due to the high fields present can serve to reduce the sensitivity of current to tip-sample distance.[31] Similar larger than expected tip-sample distances have been previously reported in other STM experiments in ambient.[25]

The STM was also used to look at the effect of large currents on localized areas of the chip. Two different methods of stressing were employed. In one stress mode, the tip was held at one spatially localized area, and an *I-V* curve was taken, causing the voltage to be ramped repeatedly from positive to negative bias. After scanning a 10 μm area, an *I-V* curve was taken over a bias range of ± 5 V or more. Upon returning to the imaging mode (1.5 V, 1–2 pA), a large dark area hundreds of nanometers in size and more than 30 nm deep was present. A similar effect was noted in another stress mode, whereby scans were kept at imaging voltages and currents but concentrated in lateral dimension. Figure 8 illustrates the appearance of a modified surface feature after a series of scans similar to those in Fig. 7. Figure 8(a) shows an initial scan of a 1 μm area, and Fig. 8(b) a rescan of the same 1 μm area after 500, 250, and 100 nm scans had been performed within it. The scan of the modified surface contains a large dark area 10 nm deep where the smaller, more concentrated, scans had occurred, similar to that which was present after the *I-V* scans. These features are likely due to the creation and charging of trap states which reduce the conductivity of the sample, as seen by others.[12,28]

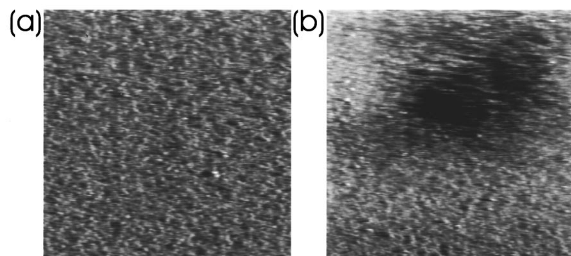

FIG. 8. (a) Before and (b) after 1.5/1.0 V, 3.0 pA STM scans of a 1 μm, 20 nm light to dark, area subjected to a zoom in sequence of scans. The 10 nm deep ''hole'' visible in (b) after zoom in represents an area of reduced conductivity.

IV. DISCUSSION

It is difficult to conclusively compare the results of these two sets of experiments. It is unclear whether the small scale lateral variations seen in the STM images on the unstressed oxides could play a role in the ''forming'' behavior of the devices or the ability of the formed oxide to continue to act as an effective barrier. It is possible that stress modification of the different conductivity regions could be related to the observed ''forming'' behavior, but unfortunately, due to the large drift in the lateral tip position, we have as yet been unable to selectively stress the different conductivity regions with the STM in order to test this hypothesis.

While we observed an increase in the oxide conductivity in the stressed regions of the TSD device, we observed a decrease in the oxide conductivity with stress in the STM experiments. Others[11] have observed an initial decrease in conductivity followed by an increase in conductivity with continued charge injection in BEEM stressing experiments. Assuming a similar behavior in our system, is possible that we were unable to inject a high enough charge density to stress the oxide to the point of increasing conductivity due to tip drift or current spreading.

V. CONCLUSIONS

Observations of the scaling behavior of the TSD device indicate that under initial heavy electrical stress, the silicon dioxide layer appears to become more conductive in the vicinity of the edges of the gate electrode where the electric field is expected to be highest. It does not break down in the conventional sense, however, as it still acts as enough of a tunnel barrier that the device supports multistable current states. AFM and STM measurements on similarly grown oxides indicate that, while the silicon and oxide surfaces are quite flat topologically, there are significant lateral electrical variations, even before significant stress has been applied. Stressing the oxide by injecting large currents with large voltages, or by concentrating a raster scan over a small area, results in an area of lower conductivity in the STM image, likely the result of negative charge trapping in the oxide.

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