Spectral logic gates for byte-wide WDM signal processing

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In light of the current trend towards the use of WDM technologies in optical networks, it is interesting to investigate new forms of all-optical signal processing, specifically designed to take advantage of multiwavelength transmission. In particular, here we consider byte-wide WDM, i.e., the parallel transmission and processing of entire bytes of information on a single fiber, with each bit assigned to a different WDM channel. This transmission format was first theoretically studied in a paper published in 1988 [1], in which a case was made for the use of byte-wide WDM in local-area computer links (in particular to eliminate the need for high-speed serializer/deserializer nodes and protocol handling circuitry). For a practical implementation (aside from techniques to actively manage fiber dispersion, which are well established nowadays) it is necessary to develop a set of logic gates capable of processing multiwavelength input signals (spectral logic) [2].

In this work we demonstrate one such gate (XOR), based on four-wave mixing (FWM) in semiconductor optical amplifiers (SOAs). This nonlinear process, which has been recently used for wavelength conversion of high data-rate signals [3]-[4], is particularly suited to this purpose because it automatically tests for the simultaneous presence of two input bits at different wavelengths (and same polarization). Notice however that FWM alone cannot be used to perform logical inversion (i.e., the NOT operation) of intensity modulated signals in any simple way. Instead, here we will use the polarization state of each wavelength channel to define its logical state (i.e., we select two orthogonal polarization states, say TE and TM, and interpret one as the logical "1" and the other as the logical "0"). The NOT gate is then immediately provided by a half-wave polarization element.

Conceptually, the construction of a FWM spectral logic gate can be divided into three main steps [2], as illustrated schematically in Fig. 1 (where we use the notation λ_C^P, with P = 1, 0 (TM, TE) denoting the polarization state of wavelength channel number C). The first step consists of resolving the optical input to the gate according to both wavelength and polarization (not shown in the figure). In the second step, some of the resulting wavelength and polarization products are inverted (i.e., their polarization is rotated by 90° with a half-wave polarization element, indicated by a solid circle in Fig. 1), in a way that depends upon the desired truth table (XOR in the case shown in the figure). Finally, these waves are coupled in two SOAs (the smallest number required to avoid spurious outcomes in this case), where the FWM conditional test function (third step) occurs. The output of the logic gate is then given by the combined output of these two SOAs, with the input wavelengths filtered out.

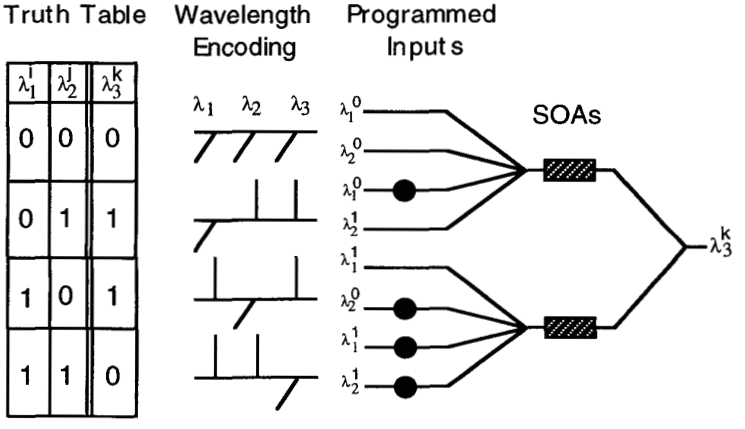

Fig.1: Schematics of the XOR gate (the solid circles denote polarization rotators)

The experimental setup is shown in Fig. 2, including the signal generators (upper box) and the XOR gate (lower box, shaded). The photonic programming chip is an integrated circuit based on silica planar waveguide technology, in which the first two steps described above are carried out. In Fig. 3 we show experimental results at 2.5 Gbit/sec: the two upper traces are the two input signals, spaced by 3 nm in wavelength, the bottom one is the gate output (the TM component of each signal is shown). The implementation of the XOR function is clearly seen in this figure. We also performed BER measurements with one of the inputs held constant and found a power penalty of less than 2 dB. Possible applications of this set of logic gates include all-optical encryption and error detection/correction, as will be discussed.

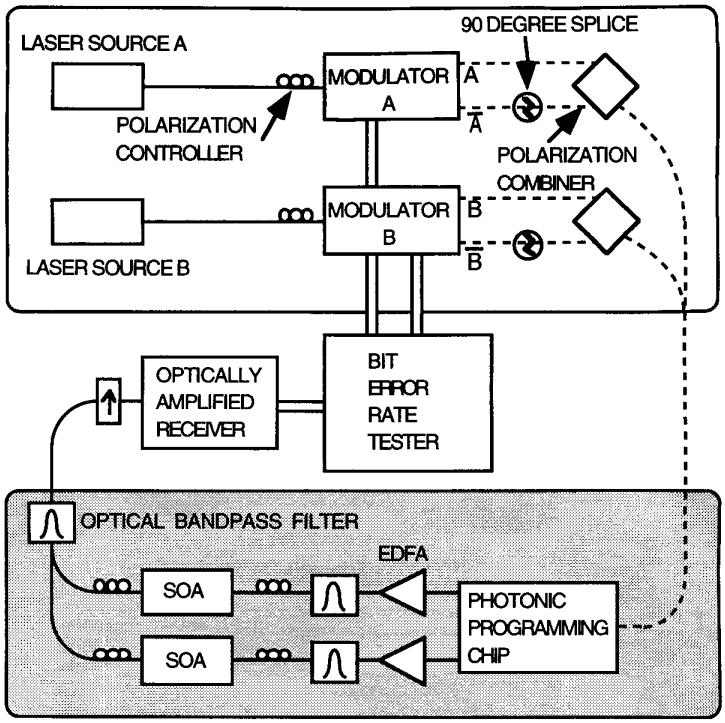

Fig. 2: Experimental setup (the dashed lines denote polarization maintaing fibers)

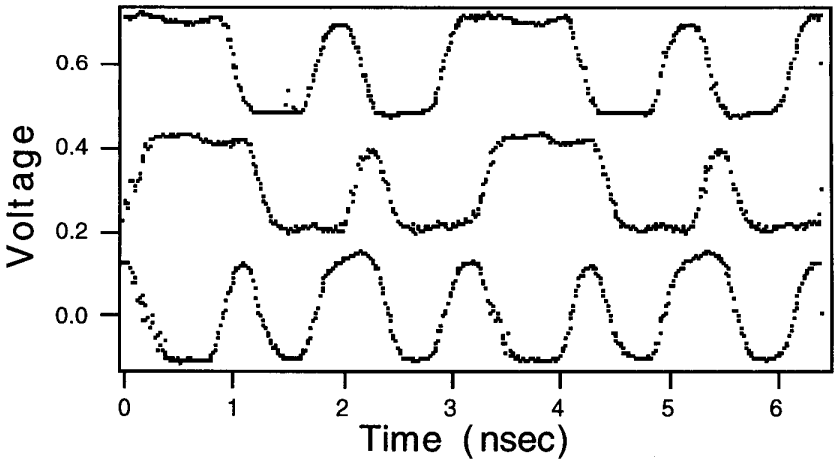

Fig. 3: Experimental results: input signals (upper traces) and output (bottom trace) of the XOR gate at 2.5 Gbit/sec

References

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