DESIGN ISSUES IN CROSS-COUPLED INVERTER SENSE AMPLIFIER

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ABSTRACT

This paper presents an analytical approach to the design of CMOS cross-coupled inverter sense amplifiers. The effects of the equilibrating transistors and the tail current source on the speed of the sense amplifier are analyzed. An analysis of the offset due to mismatch in various parameters is performed, showing that a complete offset analysis has to account for the cell and bitline structure. A new figure of merit for the offset in the sense amplifier and several new design insights are introduced.

1. INTRODUCTION

The CMOS cross-coupled inverter pair is frequently used as a fast and reliable sense amplifier. The positive feedback is exploited to achieve a fast sensing operation. Several analyses have been done on the offset of the cross-coupled pair being used as a sense amplifier [1],[2],[3]. The approach taken in [1],[2] is based on an empirical analysis while [3] presents an analysis of the system which results in series of involved analytical formulas for the mismatch.

While cross-coupled pairs have been studied extensively, the additional devices used in practice can alter the basic analysis significantly. In particular, the equilibrating device connected between the two differential nodes and the tail current source can significantly degrade the performance of the cross-coupled inverters as a sense amplifier. Several design insights on how to mitigate their effects on the sense amplifier performance can be achieved by performing an analysis which takes these devices into account.

Section 2 reviews the basic analysis of the CMOS cross-coupled regenerative response. Section 3 discusses the effect of the gradual turning off of the equilibrating device. In section 4 the gradual turning on of the tail current source at sensing time is discussed. The mismatch effect from various sources is considered in section 5.

2. BASIC CROSS-COUPLED PAIR ANALYSIS

We start with the classic analysis of the cross-coupled inverter pair. The operation of the cross-coupled pair sense amplifier shown in Fig. 1a is based on regeneration in the circuit due to positive feedback. It can be modeled by its small signal equivalent circuit shown in Fig. 1b. The equivalent model is based on two simplifying assumptions: 1) the current has been flowing in the transistors for a long enough time. 2) the equilibrating device can be modeled as an ideal switch. Both of these assumptions will be challenged in the subsequent sections. The simplified analysis of the Fig. 1 results in the following differential equation pair, for the v_1 and v_2

$$\frac{dv_1}{dt} + \frac{G_0}{C} \cdot v_1 + \frac{G_m}{C} \cdot v_2 = 0$$

$$\frac{dv_2}{dt} + \frac{G_0}{C} \cdot v_2 + \frac{G_m}{C} \cdot v_1 = 0$$

where C represents the total parasitic capacitance on regenerative nodes and

$$G_m = g_{mn} + g_{mp}$$

$$G_o = g_{on} + g_{op}$$

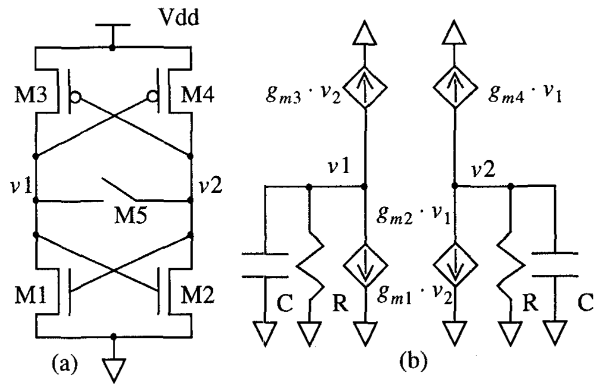

Figure 1. The simplified model for the sense amplifier.

where $g_{mn} = g_{m1} = g_{m2}$ and $g_{mp} = g_{m3} = g_{m4}$ represent the transconductance of the NMOS and PMOS devices at the beginning of the operation, respectively; g_{on} and g_{op} are the output conductances of the NMOS and PMOS devices. This pair of equations can be decoupled, defining the following variables:

$$V_{diff} = v_1 - v_2$$

$$V_{cm} = \frac{v_1 + v_2}{2}$$

During the sensing period, our major interest is toward the differential voltage which is governed by

$$\frac{dV_{diff}}{dt} + \frac{G_0 - G_m}{C} \cdot V_{diff} = 0$$

This equation has the following solution

$$V_{diff}(t) = V(0) \cdot e^{t/\tau 1}$$

where

$$\tau_1 = \frac{C}{G_m - G_o} \cong \frac{C}{G_m}$$

The time required for the output to reach a minimum acceptable voltage difference, V_{min} is given by

$$t = \tau_1 \cdot ln\left(\frac{V_{min}}{V_{init}}\right)$$

Note that this sensing time decreases linearly with τ while it changes only logarithmically with V_{init}. Therefore once a large enough differential voltage to override the offset is established on regenerative nodes it is more effective to design for the minimum time constant instead of maximizing the initial voltage difference.

3. GRADUAL TURNING OFF OF THE EQUILIBRATING DEVICE

In this section we will take into account the effect of the finite switching time of the equilibrating device. The gradual turning off of this device affects the dynamics of the sense amplifier output voltage. Fig. 2 represents a more realistic model for the sense amplifier in the presence of a equilibrating device. The voltage at the gate of the M5 can be approximately obtained from the simpli-

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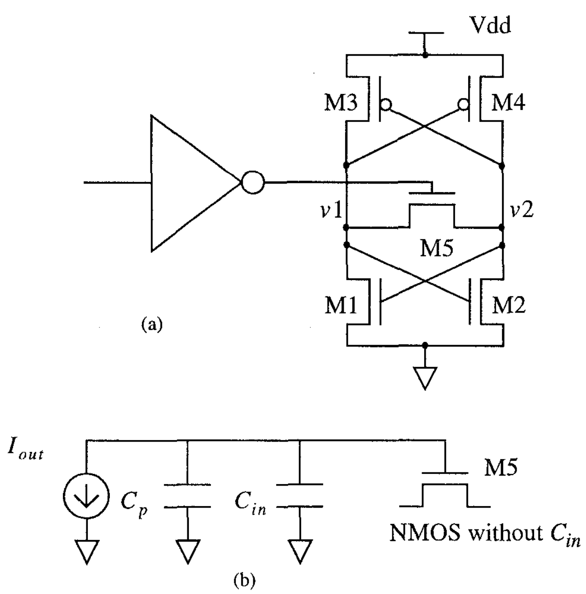


Figure 2. Equivalent circuit for the equilibrating device.

fied model shown in Fig. 2b. Note that the total gate capacitance of the M5 is shown as C_{in}. In Fig. 2 terms C_p and I_{out} represent the parasitic capacitances on the control line and equivalent average output current of the driver, respectively. Using the approximate model shown in Fig. 2b the following expression for the gate voltage of M5 is obtained

$$V_G = V_{dd} - r \cdot t$$

where $r = I_{out}/(C_{in} + C_p)$ is the slope of the voltage transition. The above expression can be used to find the conductance of the equilibrating device as a function of time. Since this expression is going to be used during the firing period of the sense amplifier (*i.e.* M5 turning off) the common mode voltage of the nodes can be approximated as being $V_{dd}/2$. Note that the following analysis is valid irrespective of this particular choice of the initial common-mode voltage. Using these approximations G_{on} can be written as

$$G_{on}(t) \cong \mu_n C_{ox} \cdot \frac{W}{L} \cdot \left[\frac{V_{dd}}{2} - V_T - r \cdot t\right]$$

This results in the following differential equation for the output differential voltage of the sense amplifier

$$\frac{dV_{diff}}{dt} + \left[\frac{2G_{on}(t) - G_m}{C}\right] \cdot V_{diff} = 0$$

The above equation can be solved to give the following solution

$$V(t) = \begin{cases} V_{init} \cdot e^{t/\tau_1} \cdot e^{t^2/\tau_2^2} & t \le t_{off} \\ V_{init} \cdot e^{t_{off}/\tau_1} \cdot e^{t_{off}^2/\tau_2^2} \cdot e^{t/\tau_3} & t > t_{off} \end{cases}$$

where

$$\tau_1 = \frac{C}{G_m - 2G_{on0}}$$

$$\tau_2 = \sqrt{\frac{2C}{\mu_n C_{ox} \cdot \frac{W}{L} \cdot r}}$$

and

$$\tau_3 = \frac{C}{G_m}$$

in which G_{on0} represents the on conductance of M5, *i.e.*

$$G_{on0} = \mu_n C_{ox} \cdot \frac{W}{L} \cdot \left(\frac{V_{dd}}{2} - V_T\right)$$

and t_{off} is the time M5 turns off, *i.e.* $V_G = V_{dd}/2 - V_T$.

As can be seen from the above equation for the $V(t)$, making the W/L ratio of the equilibrating device smaller makes the retention operation faster. This can be seen intuitively too. Since a large device shows a large positive conductance at the regenerative nodes, which makers the term G_o larger and as a result makes τ larger. So every effort should be made to minimize the size of the equilibrating device as long as it can equalize the residual voltage from last sensing cycle.

4. GRADUAL CURRENT SOURCE TURNING ON

The cross-coupled pair sense amplifier usually incorporates a tail MOS current source which operates to limit the power dissipation and facilitates the equilibrating device operation as shown in Fig. 3. The exact time at which this device is turned on is arbitrary to some extent. It can be turned on at the same time as the equilibrating device is turned off, or it can be turned on earlier or later. The earlier this device is turned on the larger the power dissipation and the faster the sensing time. It also affects the offset mismatch in device parameters and the charge injection.

To gain more intuition into the circuit, an analytical approximation for this circuit is attempted on the circuit model of Fig. 3. The same analysis as the simple cross-coupled pair can be applied assuming a time dependent transconductance, $g_m(t)$, for the MOS devices. The transconductance depends on the tail current in the following form

$$g_{m(n,p)} = \sqrt{\mu_{(n,p)} C_{ox} \frac{W_{(n,p)}}{L_{(n,p)}} I_D}$$

While M6 is in the pinch-off region, the following expression for the total $G_m = g_{mn} + g_{mp}$ can be obtained

$$G_m(t) = \alpha \cdot (V_{dd} - V_{CS} - V_T)$$

where

$$\alpha = \frac{C_{ox}}{2} \cdot \sqrt{\mu_n \frac{W_c}{L_c}} \cdot \left(\sqrt{\mu_n \frac{W_n}{L_n}} + \sqrt{\mu_p \frac{W_p}{L_p}}\right)$$

W_c/L_c, W_n/L_c, W_p/L_p stand for the W/L ratio of the tail current source device, NMOS, and PMOS, respectively, and V_{cs} is the voltage on the gate of M6.

The differential equation governing the differential voltage across the sensing nodes is

$$\frac{dV_{diff}}{dt} - \frac{G_m(t)}{C} \cdot V_{diff} = 0$$

Assuming a slope of r for the gate voltage of M6 the following solution for the differential equation is obtained

$$V_{diff}(t) = \begin{cases} V_{init} \cdot e^{\frac{G_{mf}}{C} \cdot \frac{t^2}{2t_f}} & 0 < t < t_f \\ V_{init} \cdot e^{\frac{G_{mf}}{C} \cdot \frac{t_f}{2}} \cdot e^{\frac{G_m}{C} \cdot t} & t_f < t \end{cases}$$

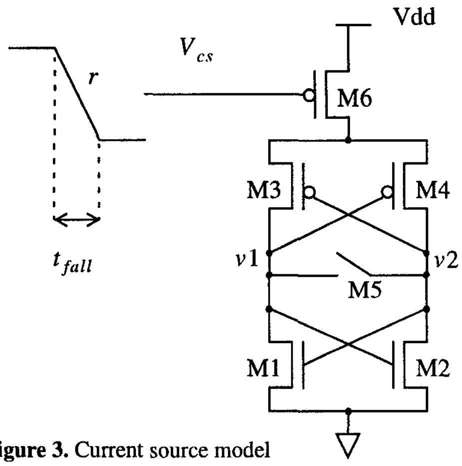


Figure 3. Current source model

where t_f is the fall time of V_{cs}. From the above equation for $t = t_f$

$$V_{diff}(t_f) = V_{init} \cdot e^{\left(\frac{G_m}{C} \cdot \frac{t_f}{2}\right)}$$

The argument of the exponential function is half the value it would have if the devices were turned on early. This shows that further speed improvements are possible by turning on these devices earlier, or faster. The maximum delay penalty is $t_f/2$.

It can be seen that there is a trade-off between the speed advantage obtained by turning M6 on earlier and the corresponding increase in the power dissipation. It should also be noted that the early turning on of the current source device will eliminate the charge injection mismatch due to the switching of the current source device.

5. MISMATCH EFFECTS

In this section the effect of mismatch on the sensing operation in an SRAM, such as the mismatch in the threshold voltages, *W/L* ratios, mobilities and oxide capacitances for a pair of equal size transistors is considered. A complete static analysis of the mismatch should take into account the bitline architecture and cell, as well as the sense amplifier structure. The structure shown in the Fig. 4a, is the model used for this analysis. It includes the pull-up devices, the cell, the switching circuitry (which is simply modeled as a lossy wire) and the sense amplifier itself. The efficiency of the lossy wire is quantified by α. The information about the value of the bit of data stored in the cell is embedded in the current difference seen on the bitlines, which is the differential current of the cell

$$I_{cell} = I_n + I_p$$

This model can be further simplified to the model shown in Fig. 4b. The V_{osn} and V_{osp} represent the threshold mismatch of the NMOS and PMOS devices, respectively.

5.1 Threshold Mismatch

In this subsection we only consider the effect of threshold mismatch and in the next subsection we extend the results to other forms of static mismatches.

Assuming small values of the offset in the model of Fig. 4b, an offset voltage in threshold voltage can be translated into a current mismatch in the drain with a gain of g_m. Assuming the worst polarity for the offset voltages, the maximum effective offset voltage at the regenerative nodes is

$$v_{offset} = (g_{mn}v_{osn} + g_{mp}v_{osp})R_{eff}(t)$$

Where g_m and v_{os} are the transconductance and threshold mismatch of the corresponding devices, respectively, and $R_{eff}(t)$ represents the effective resistance seen between the two regenerative nodes. This impedance varies drastically as the equilibrating device is turned off. The effective resistance seen between the two terminals changes from a positive value to a negative value due to positive feedback. The behavior of the $R_{eff}(t)$ with time can be quite complex, but as will be seen shortly, the detail of this behavior with time will not affect the final result. From Fig. 4c, it can be seen that I_{cell} results in a useful voltage which is a representative of the data in the cell being read. This voltage is

$$\Delta V_{useful}(t) = I_{cell} \cdot R_{eff}(t)$$

It is the relative size of the useful voltage to the effective offset voltage across the differential nodes that determines the safety margin for sensing rather than the absolute value of the offset voltage. We define the ratio of the useful voltage across the differential nodes to the effective offset voltage as the safety margin. The ratio has the advantage of not changing with scaling to lower voltages, so it can be chosen as a figure of merit indicating safety margin of a given design

$$Margin = \frac{\Delta V_{useful}}{\Delta V_{offset}} = \frac{\alpha I_{cell}}{g_{mn}v_{osn} + g_{mp}v_{osp}}$$

As can be seen the *Margin* does not depend on the variations of the $R_{eff}(t)$ with time to the first order. Therefore this ratio can be used as a time-independent figure of merit to indicate the robustness of the sense amplifier. This ratio can be interpreted as the ratio of the cell current to the equivalent offset current mismatch. So the effective offset current is:

$$I_{offset} = g_{mn}v_{osn} + g_{mp}v_{osp}$$

Note that I_{offset} unlike V_{offset}, does not strongly depend on the size of the equilibrating device.

5.2 Transconductance Mismatch

The transconductance mismatch can be translated to an equivalent threshold mismatch. This mismatch is mainly due to lithographic error in W*s* and L*s* of the MOS devices, the mismatch in channel mobilities and the gate capacitances. We assume the following behavior in the saturation region for the MOS devices:

$$I_D = k(V_{gs} - V_T)^{\gamma}$$

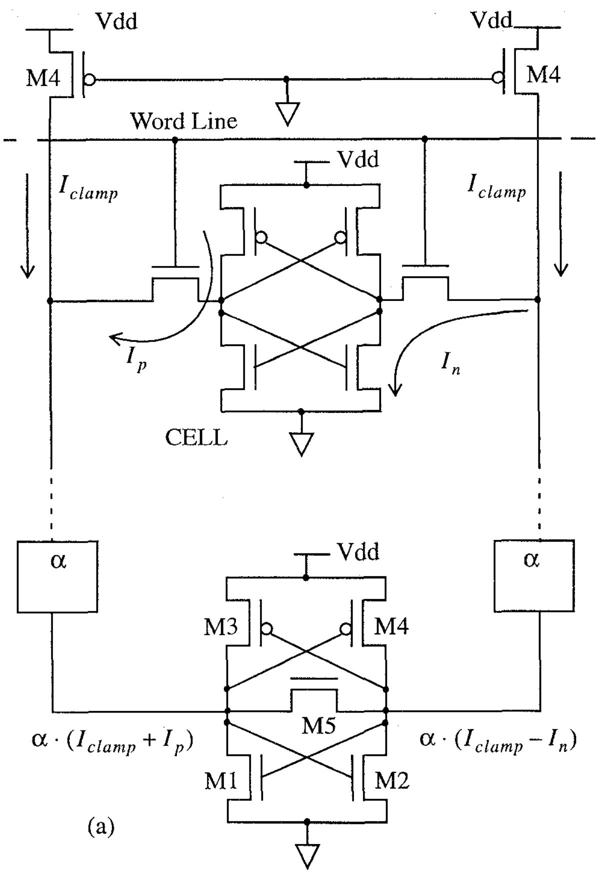
Where γ is a function of effective channel length and varies between 2 and 1. Applying the differential sensitivity method to the above equation we obtain the following for small variations in the variables

$$\frac{\Delta k}{k} + \gamma\frac{\Delta V_T}{V_T} = \frac{\Delta I}{I}$$

So the effect of the variations in the transconductance factor, κ on the output current can be transformed to an equivalent mismatch in threshold voltage, as follows

$$\Delta V^{\dagger}_T = \frac{\Delta k}{k} \cdot \frac{V_T}{\gamma}$$

The $\Delta V^{\dagger}_T$ term is the amount of threshold voltage offset that would have resulted in the same amount of offset caused by transconductance offset. So the worst case offset can be obtained



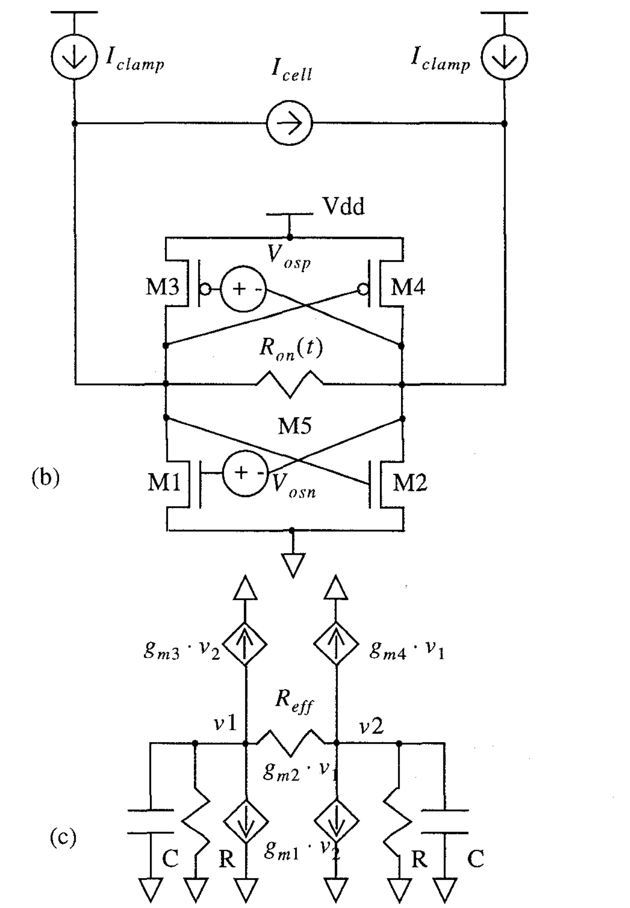


Figure 4. The bitline structure and the offset definitions.

based on the assumption that all different offset effects are added in the worst possible way, *i.e.*

$$V^*_{osn} = \Delta V_{Tn} + \frac{\Delta k_n}{k_n} \cdot \frac{V_{Tn}}{\gamma}$$

$$V^*_{osp} = \Delta V_{Tp} + \frac{\Delta k_p}{k_p} \cdot \frac{V_{Tp}}{\gamma}$$

Note that the $\frac{\Delta k}{k}$ term can be expanded as:

$$\frac{\Delta k}{k} = \frac{\Delta W}{W} + \frac{\Delta L}{L} + \frac{\Delta \mu}{\mu} + \frac{\Delta C_{ox}}{C_{ox}}$$

For small values of L and/or W the dominant term is the transconductance mismatch term; there are two sources for this dominance. The term $\Delta k/k$ is proportional to $1/L + 1/W$, so decreasing L and/or W will result in a larger transconductance mismatch term. Also due to short channel effects, for shorter Ls the exponent γ will decrease. The most important conclusion from the above development is that it is the relative values of the cell current to the effective offset current of the sense amplifier that determines the safety margin of the sensing. So any measurement, simulation or calculation of the sense amplifier offset without considering the effect of the cell and bitline structure can result in misleading predictions.

6. CONCLUSION AND ACKNOWLEDGEMENT

The detailed analysis of the cross-coupled pair sense amplifier shows that the speed of this sense amplifier can deviate from what is predicted by the basic theory due to several practical limitations on the design. Through an analytical approach these deviations are considered, and the trade-offs involved are discussed. Also, a practical method to quantify and compare the effect of offset in such a sense amplifier is developed.

The authors would like to acknowledge SUN Microelectronics and the global SRAM group where this work was done.

7. REFERENCES

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