# A 10-Watt X-Band Grid Oscillator

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*Abstract*—**A 100-transistor MESFET grid oscillator has been fabricated that generates an effective radiated power of 660 W at 9.8 GHz and has a directivity of 18.0 dB. This corresponds to a total radiated power of 10.3 W, or 103 mW per device. This is the largest recorded output power for a grid oscillator. The grid drain-source bias voltage is 7.4 V and the total drain current for the grid is 6.0 A, resulting in an overall dc-to-rf efficiency of 23%. The pattern of the SSB noise-to-carrier ratio was measured and found to be essentially independent of the radiation angle. The average SSB noise level was −87 dBc/Hz at an offset of 150 kHz from the carrier. An average improvement in the SSB noise-to-carrier ratio of 5 dB was measured for a 100-transistor grid compared to a 16-transistor grid.**

## I. Introduction

For many years there has been a substantial effort to obtain more power from high-frequency solid-state devices. For this reason, power combining schemes involving solid-state devices quasi-optically coupled in free space have received considerable attention as an efficient means of combining the output power of many devices at microwave and millimeter-wave frequencies. A quasi-optical grid oscillator consists of a two-dimensional array of active devices producing a planar sheet with a reflection coefficient greater than unity. A resonator can be used to provide feedback to couple the devices together to form a high-power oscillator. By integrating large numbers of devices into the grid, very large powers should be achievable.

Recent work on grid oscillators [1,2,3] has convincingly demonstrated proof of concept. However, these grids have all used relatively low-power devices and have not delivered the promised large powers. To date, the highest published total radiated power for a transistor grid oscillator is 550 mW at 5 GHz from a 100-transistor grid [2]. In order to demonstrate greater output powers from a grid oscillator, we have developed a 100-transistor X-band grid using medium-power Fujitsu FLK052XP MESFET chip transistors as the active devices. The grid oscillator is shown in Fig. 1. Each transistor lies in the center of a unit cell which is defined by the grid symmetry. The drain and source leads lie vertically while the meandered gate leads runs horizontally across the grid. Forced air blown across the grid surface cools the grid. In addition, the transistors are soldered onto the relatively thick drain lead of the grid metal pattern to aid cooling. The grid was designed to oscillate near 10 GHz. The dimensions of the grid were chosen to control load impedance, feedback loop gain, and compensate for device parasitics to obtain maximum power from the devices. The unit cell is 7.50-mm square. The vertical lead is 1.10-mm wide and the meandered lead is 1.25-mm wide with a line width of 0.15 mm. The grid pattern was fabricated on a Duroid substrate with a dielectric constant of 2.2. The substrate is 1.6-mm thick and is placed in front of a planar mirror.

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## II. Grid Oscillator Design

We analyze the grid by considering a transistor in an equivalent-waveguide unit-cell [2] with electric walls on the top and bottom and magnetic walls on each side, as shown

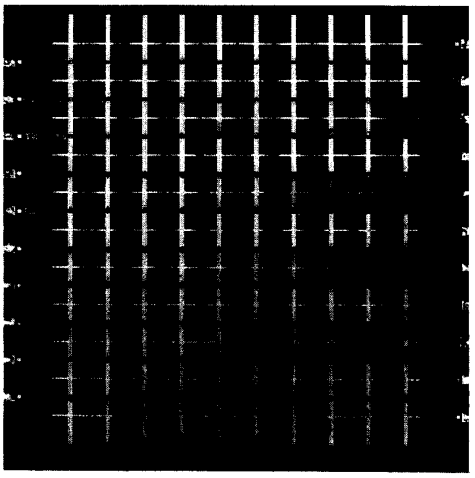

**Figure 1.** Photograph of the 100-transistor grid oscillator. The grid produced 10.3 W total radiated power with a dc-to-rf efficiency of 23%. Quarter-wave vertical stubs are added at the grid top and bottom edges to try to simulate an electric wall. Ferrite slabs are added along the vertical grid edges to suppress bias-line oscillations.





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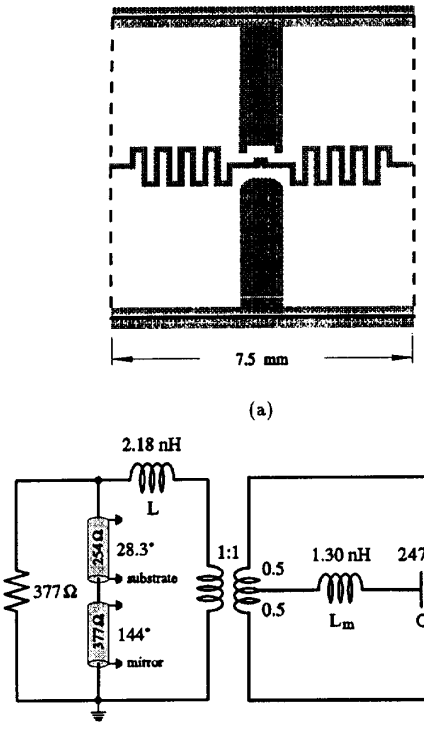


**Figure 2.** (a) Equivalent-waveguide unit-cell metal pattern for the grid oscillator. Boundary conditions are imposed by grid symmetry. The solid lines are electric walls and the dashed lines are magnetic walls. (b) Equivalent-circuit model used to predict the theoretical performance of the grid at 10 GHz.

in Fig. 2(a). The Hewlett-Packard High-Frequency Structure Simulator can be used to analyze the impedances presented to the transistor terminals placed in the equivalent waveguide. Such an analysis leads to the transmission-line model shown in Fig. 2(b). Free space is modelled by a 377-Ω resistor, and a mirror placed behind the grid is modelled as a shunt short-circuited transmission line. Currents in the vertical leads couple to the radiated field through a center-tapped transformer. The coupling of the currents to evanescent TM and TE modes is approximated with reactive elements.

In order to get the most power out of the transistors, the grid must be designed to provide an optimum impedance between the drain and source terminals. A simple load-line analysis can be used to compute the approximate optimal load impedance to present to the transistor for maximum power [4]. The optimal load is defined as the impedance that allows the transistor output terminals to swing between the maximum allowable voltage and current limits. This optimal load resistance $R_{opt}$ is given by $2V_{DC}/I_{DSS}$, where $V_{DC}$ is the drain-source dc bias voltage and $I_{DSS}$ is the maximum saturated drain current. This resistance is presented to the current-source terminals of the transistor equivalent circuit. For the Fujitsu FLK052XP transistor biased at 10 V and 120 mA, this optimal load impedance is 83 Ω.

For maximum oscillator power, Johnson has shown that the transistor must be operating at the point where maximum power-added efficiency occurs [5]. Since this is a function of gain compression, or transistor saturation, it can be controlled by varying the amount of feedback applied to the transistor. An analysis of the Fujitsu FLK052XP MESFET shows that at 10 GHz the maximum power-added efficiency occurs at 4.1 dB of gain saturation with a theoretical maximum oscillator output power of 338 mW per device. Most grid oscillator designs to date have used unit cells that provide a feedback path that is largely internal to the grid and result in much larger loop gains. Fortunately, the loop gain can be lowered by meandering the horizontal gate lead to increase the center-tapped inductance, $L_m$, of the grid equivalent circuit.

The grid was designed to oscillate at 10 GHz and the cell dimensions were adjusted to try to present the optimal load impedance of 83 Ω to the transistor with a loop gain as close as possible to the desired value of 4.1 dB. The final design was a compromise with a transistor load impedance of 85+j30 Ω and a loop gain of 3.7 dB (Fig. 3). Fortunately, the excess reactance in the load impedance can be tuned out by placing a double slug tuner, consisting of two quarter-wave *Duroid* slabs, in front of the grid.

## III. Grid Oscillator Performance

The measured oscillation frequency of the 100-transistor grid was 9.80 GHz. This is within 2% of the design value of

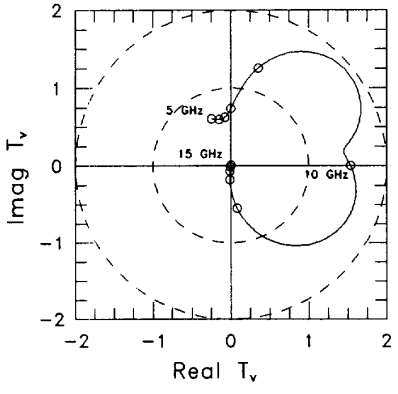


**Figure 3.** Theoretical loop gain ($T_v$) of the grid from 5 to 15 GHz. The predicted oscillation frequency, where the locus crosses the zero-phase point, is 10.0 GHz and the corresponding loop gain is 3.7 dB. Intervals of 1 GHz are marked with a (o).

10.0 GHz. The measured effective radiated power (ERP) for the grid was 660 W. This corresponds to a total radiated power of 10.3 W, or 103 mW per device. The grid drain-source bias voltage was 7.4 V, and the total drain current for the grid was 6.0 A (21 mA per device on the top and bottom rows and 70 mA per device on the inner rows), resulting in an overall dc-to-rf efficiency of 23%. This efficiency is comparable to that observed for previous MESFET grid oscillators [2,3].

A nonlinear simulation of the equivalent-waveguide unit cell using the EEsof Libra harmonic-balance software gave a predicted oscillation frequency of 9.88 GHz and a power of 210 mW per device for a drain bias of 7.4 V and 70 mA. The predicted dc-to-rf conversion efficiency is 41%.

Unfortunately, the measured power is still 5 dB lower than the theoretical maximum of 338 mW per device. This is attributable partly to the use of a dc bias voltage of 7.4 V, instead of the recommended value of 10 V. In addition, the devices on the top and bottom rows were biased at a lower current to keep them locked. Attempts to run the grid at a dc bias above 7.4 V resulted in the failure of the center-row devices on the vertical grid edge where the drain and source dc bias lines are attached. Very high currents were present—bond wires fused on several of the devices. The drain bias lines also melted. Various ferrite slab edge terminations were investigated, but the problem persisted, preventing operation of the grid above 7.4 V. Finally, there is the possibility that some degradation of the devices occurred during the extensive testing period.

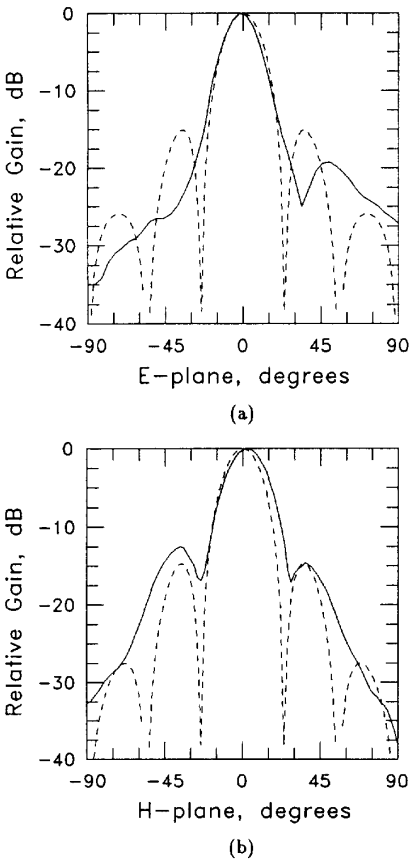


**Figure 4.** Measured E-plane (a) and H-plane (b) patterns (solid lines) and theoretical patterns (dashed lines) for the grid oscillator with 0.4-mm mirror spacing. Aperture blockage occurs in the E-plane for angles between −60° and −90°.

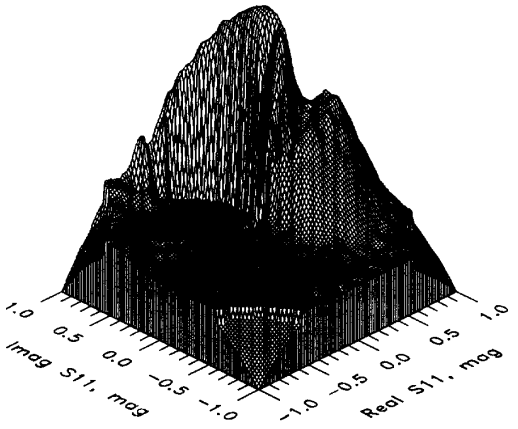


**Figure 5.** Load-pull contour measured for the grid oscillator. The scale is linear in ERP and is plotted as a function of reflection coefficient referenced to 377 Ω at the grid face.

The measured directivity of the grid was 18.0 dB which is close to the estimated directivity of 18.8 dB computed by assuming the effective area of the grid at 9.8 GHz is equal to the sum of the physical area of the unit cells. Fig. 4 shows the measured and theoretical E-plane (a) and H-plane (b) radiation patterns. The theoretical patterns were calculated for a uniform array of infinitesimal dipoles on a substrate. The patterns agree well, except that the E-plane sidelobes are better than predicted. This may be a result of the bias arrangement. The devices in the top and bottom rows were biased at a lower level than the devices on the inner rows, and this may have tapered the current distribution.

A load-pull measurement was performed on the grid (Fig. 5). The impedance was varied with a double-slug tuner, consisting of two quarter-wave Duroid slabs with a dielectric constant of 10.5, in front of the grid. The peak power occurs for an impedance of $490 + j660\,\Omega$.

The single-sideband noise patterns for both a 16-transistor grid and a 100-transistor grid were measured. For a

multiple-device oscillator, Kurokawa predicts an improvement in oscillator noise proportional to the number of devices [6]. For a 100-transistor grid, we expect to see an improvement of 100/16 (8.0 dB) over an equivalent 16-transistor grid. Fig. 6 shows the measured SSB noise pattern in the E and H planes for the two grids. The noise was measured at a 150 kHz offset from the carrier using a spectrum analyzer with a resolution bandwidth of 30 kHz. The SSB noise level averaged over both E and H planes was -87 dBc/Hz. The mean measured improvement in H-plane SSB noise of the 100-transistor grid compared to the 16-transistor grid was 4.9 dB. For the E-plane, the mean measured improvement for the SSB noise was 5.9 dB.

The noise-to-carrier ratio was essentially independent of angle, indicating that the noise had the same radiation pattern as the carrier. This initially surprised us. The fact that the noise-to-carrier ratio improved in the larger grid indicated that the fundamental noise sources were uncorrelated, and we had thought that this would lead to a noise pattern that was much broader than the carrier pattern. One explanation might be that the gain for the oscillating mode is much larger than for other possible modes in the grid.

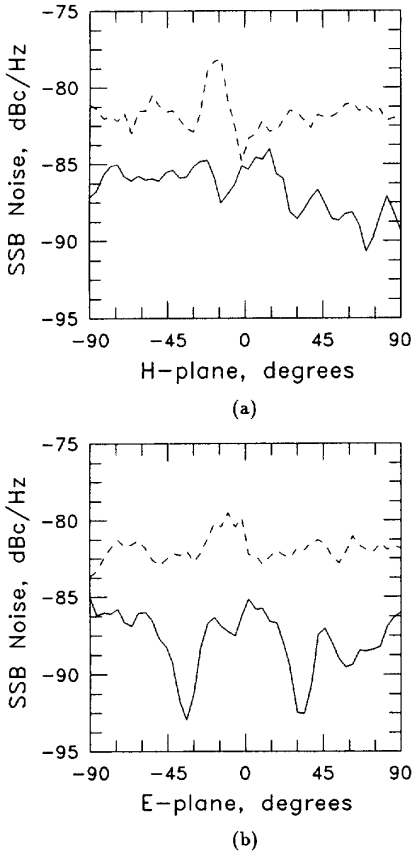


**Figure 6.** Measured SSB noise at 150 kHz offset from the carrier for a 100-transistor grid (solid line) and a 16-transistor grid (dashed line) in (a) the H-plane and (b) the E-plane.

## IV. Conclusion

A high-power X-band 100-transistor grid oscillator has been demonstrated based on commercial MESFET power transistors. The grid embedding circuit was designed to provide the optimal load impedance and feedback loop gain to the transistor for maximum power. The measured effective radiated power was 660 W and the directivity was 18.0 dB. This corresponds to a total radiated power of 10.3 W, or 103 mW per device. This power is competitive with the 3–7 W reported for state-of-the-art MMICs [7]. The grid drain-source bias voltage was 7.4 V and the total drain current for the grid was 6.0 A, resulting in an overall dc-to-rf efficiency of 23%. The SSB noise-to-carrier pattern was found to be essentially independent of the radiation angle. The average SSB noise level was -87 dBc/Hz at an offset of 150 kHz from the carrier. An average improvement in SSB noise of 5 dB was measured for a 100-transistor grid compared to a 16-transistor grid.

## References


[1] Z.B. Popović, M. Kim, D.B. Rutledge, "Grid Oscillators," *Int. J. Infrared and Millimeter Waves, vol. 9*, no. 7, pp. 647–654, 1988.

[2] Z.B. Popović, R.M. Weikle, M. Kim, D.B. Rutledge, "A 100-MESFET Planar Grid Oscillator," *IEEE Trans. Microwave Theory Tech., MTT-39*, no. 2, pp. 193–200, Feb. 1991.

[3] R.M. Weikle, M. Kim, J.B. Hacker, M.P. De Lisio, D.B. Rutledge, "Planar MESFET Grid Oscillators using Gate Feedback," *IEEE Trans. Microwave Theory Tech., MTT-40*, no. 11, pp. 1997–2003, Nov. 1992.

[4] S.C. Cripps, "Old-Fashioned Remedies for GaAsFET Power Amplifier Designers," *IEEE Microwave Theory Tech. Newsletter*, no. 128, pp. 13–17, Summer 1991.

[5] K.M. Johnson, "Large Signal GaAs MESFET Oscillator Design," *IEEE Trans. Microwave Theory Tech., MTT-27*, pp. 217–227, Mar. 1979.

[6] K. Kurokawa, "The Single-Cavity Multiple-Device Oscillator," *IEEE Trans. Microwave Theory Tech., MTT-19*, no. 10, pp. 793–801, Oct. 1971.

[7] D.T. Bryant, *et al*, "Ku-Band Monolithic 7-Watt Power Amplifier using AlGaAs-GaAs 0.25 $\mu$m T-Gate Heterostructure FET Technology," 1993 *IEEE MTT-S Intl. Microwave Symp. Dig.*, pp. 1373–1376.