Probing the size and density of silicon nanocrystals in nanocrystal memory device applications

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Structural characterization via transmission electron microscopy and atomic force microscopy of arrays of small Si nanocrystals embedded in SiO_2, important to many device applications, is usually difficult and fails to correctly resolve nanocrystal size and density. We demonstrate that scanning tunneling microscopy (STM) imaging enables a much more accurate measurement of the ensemble size distribution and array density for small Si nanocrystals in SiO_2, estimated to be 2–3 nm and $4\times10^{12}-3\times10^{13}$ cm^{-2}, respectively, in this study. The reflection high energy electron diffraction pattern further verifies the existence of nanocrystallites in SiO_2. The present STM results enable nanocrystal charging characteristics to be more clearly understood: we find the nanocrystal charging measurements to be consistent with single charge storage on individual Si nanocrystals. Both electron tunneling and hole tunneling processes are suggested to explain the asymmetric charging/discharging processes as a function of bias. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1852078]

Silicon nanocrystal memories[1] have attracted much attention in recent years. To fully exploit their potential advantages over conventional floating gate memory, it is essential to control as accurately as possible Si nanocrystal size, depth distribution, and areal density, as well as nanocrystal surface passivation and oxide defect density in SiO_2 matrix, all in a process compatible with ultra-large-scale integration. Transmission electron microscopy (TEM) is the most widely used tool to characterize nanocrystal size and distribution with high resolution,[2–4] and sometimes electron diffraction is used to further substantiate the existence of crystallites. We have used a combination of contact-mode atomic force microscopy (AFM) and reflection high energy electron diffraction (RHEED) to identify the existence of nanocrystals, and used an ultrahigh vacuum scanning tunneling microscope (UHV STM) to estimate nanocrystal size and areal density. Compared with TEM, using RHEED with very small incident angle enables high sensitivity to nanocrystal structure, and the resolution of STM is sufficiently high to detect nanometer size crystallites. The charging, discharging, and retention behaviors of the MOS capacitor nanocrystal memory structures were investigated by capacitance–voltage ($C-V$) measurements. The results obtained from both structural and electrical characterization are combined for complete analysis of nanocrystal floating gate memory devices made via Si ion implantation.

The samples investigated consist of 15 nm dry oxide grown on p-type silicon substrate ($N_A=3\times10^{18}$ cm^{-3}) implanted with 5 keV Si^+ ions to a fluence of 1.27×10^{16} cm^{-2}. The samples were annealed at 1080 °C for 5 min in an atmosphere containing 2% O_2 to allow formation of Si nanocrystals. Control samples without implantation were fabricated with the same structure and treated with the same condition as samples with nanocrystals. Cross-sectional high resolution TEM characterization did not clearly reveal individual Si nanocrystals, although the 15 nm SiO_2 and the crystalline phase of the (100) Si substrate are clear in the image. Electron diffraction is also unable to confirm the existence of a crystalline Si phase in the SiO_2 layer. We attribute this result to the small sizes of nanocrystals and electron scattering by the surrounding amorphous SiO_2 matrix. Due to small Z contrast between Si and SiO_2, it is hard to detect Si nanocrystals with electron microscopy at sizes of approximately 2 nm.

AFM and RHEED were used to characterize samples etched with buffered hydrofluoric acid approximately halfway through SiO_2 layer (Fig. 1). The inset shows the RHEED pattern. The continuous background from amorphous SiO_2 confirms that etching only happened halfway

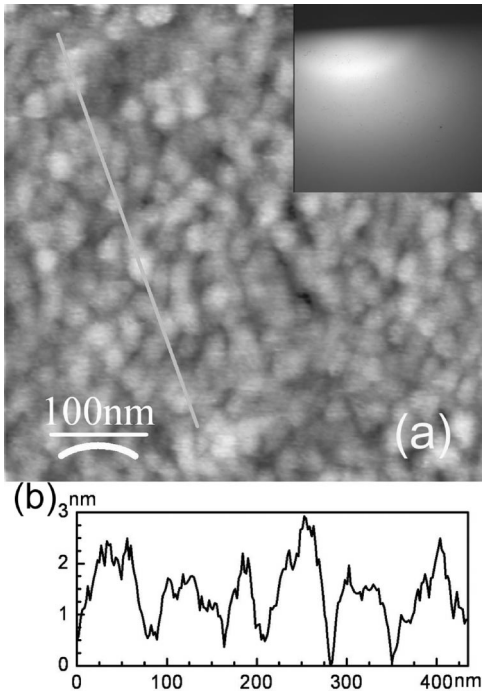

FIG. 1. (a) AFM image (500 nm×500 nm) of half-etched SiO_2 film containing Si nanocrystals. Inset shows the corresponding RHEED pattern. (b) Cross section along the line indicated in (a).

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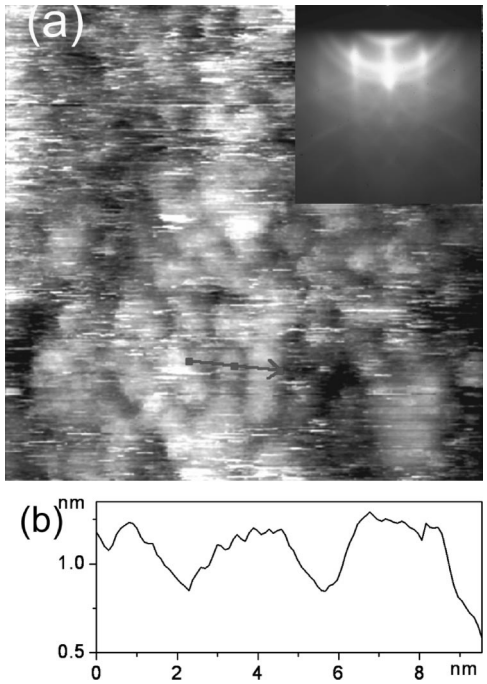

FIG. 2. (a) STM topography image (50 nm×50 nm) of Si nanocrystals on Si substrate. Inset shows the corresponding RHEED pattern. (b) Cross section along the arrow in (a).

down. Compared with the pattern from a control sample under exactly the same experimental condition (not shown), it is different since at least one bright ring can be seen. After digitally subtracting the diffraction pattern of the control sample from the diffraction pattern of the half-etched sample, more rings could be found. These rings indicate the existence of Si nanocrystals with random crystalline orientations. Figure 1(a) shows contact mode AFM images with 0.5 μm field of view. Using this result, a nanocrystal areal density can be estimated to be 1.6×10^{11} cm^{-2}. This is an underestimated value. Because the tip size is much larger than nanocrystal sizes, the observed "particles" in the images are in fact clusters of dozens of nanocrystals,[5] which is verified by STM measurement on a fully etched sample. With the results from contact-mode AFM and RHEED, the nanocrystal formation in SiO_2 layer is identified qualitatively.

To evaluate quantitative data like nanocrystal sizes and density, STM is found to be a better tool. Millo *et al.* have used STM to characterize CdSe and InAs quantum dots on Au.[6,7] The STM measurements of Si nanocrystals fabricated through low pressure chemical vapor deposition[8] and nanocrystalline silicon films obtained by boron implantation of amorphous Si layers[9] have also been reported. In our case, samples have to be etched with buffered hydrofluoric acid to completely remove SiO_2, leaving Si nanocrystals terminated with hydrogen and adhering directly on the Si substrate. Within several minutes after etching, samples were loaded into the chamber of an ultrahigh vacuum STM. The vacuum inside the chamber was kept at 1×10^{-10}Torr to avoid further oxidation of Si. Figure 2(a) shows the resolved Si nanocrystals in a cluster. The lateral dimension of the image is 50 nm. The sizes of the particles are quite uniform in this area, with smallest interparticle distances of about 3 nm [Fig. 2(b)]. Based on this information, we set an upper bound of nanocrystal size to be 3 nm. Because tip convolution effects occur even for a sharp STM tip, the scan profile of an individual nanocrystal cannot be used to obtain an accurate width or aspect ratio. Larger area scans of half-etched sample [Fig. 1(b)] indicate surface variation of about 3 nm, and photoluminescence (PL) measurements by Biteen *et al.* give a size of 3.2 nm[10] when compared with calculations by Puzder *et al.*[11] Both are consistent with STM results. It should be noted the size obtained from PL data may be overestimated due to the energy transfer from small nanocrystals to large nanocrystals. The areal density of nanocrystals on fully etched sample is measured to be around 4×10^{12} cm^{-2}, which is 25 times higher than the result from AFM. Consider the loss of nanocrystals during etching process, this value is still a lower bound. Assuming an average nanocrystal size of 2.5 nm, the calculation using total fluence of implanted Si^+ ions gives an area density of 3×10^{13} cm^{-2}, which is an upper bound. Some Si^+ may be implanted into Si substrate, and there is also Si loss by defusing into the substrate during high temperature annealing. Even for Si atoms remaining in the SiO_2, not all contribute to the formation of nanocrystals. The actual nanocrystal density should be between these two values. The inset of Fig. 2(a) shows RHEED pattern, in which diffraction spots and Kikuchi lines from single crystal substrate and diffraction rings from nanocrystals can be clearly seen, while the pattern of the control sample does not contain diffraction rings. The clear rings in diffraction pattern of fully etched sample further prove the observed nanoparticles in STM images are crystalline.

To evaluate the potential applications of such nanocrystals in memory device, 800-Å-thick gold was deposited with mechanical masks on top of samples with nanocrystals embedded in 15 nm SiO_2 to form metal–oxide–semiconductor (MOS) structure. Capacitance–voltage ($C-V$) measurements were used to analyze charging and discharging phenomena. Figure 3(a) shows $C-V$ hysteresis curves with various scan ranges of gate bias. In the experiment, MOS devices were first scanned between −1 and +1 V (±1 V scan), and no hysteresis was found, indicating no charging or discharging. The observed flatband voltage is very close to the theoretical value for $Au/SiO_2/p-Si$ structure, −0.15 V.[12] The same happened for ±2 V scan. After that, there is still no hysteresis in ±3 V scan, but the curve shifts to the left by a small amount. This indicates charging of holes into the floating gate, but no erasing at positive voltages. In the subsequent ±4 V scan, erasing of holes leads to the appearance of hysteresis. Due to partial erasing, the right edge of the $C-V$ curve is still to the left of initial curves of the ±1 V scan and ±2 V scan, until the positive voltage is large enough for complete erasing, which happened at 4.5 V. After that, both hole charging and electron charging of the floating gate can be observed, resulting in a wider and wider hysteresis loop. The retention times were obtained with capacitance decay measurements at 0 V, after MOS capacitor is charged at +5.5 and −5.5 V, respectively [Fig. 3(b)]. It is within the range that capacitance changes about linearly with voltage shift, which is proportional to areal density of stored charges. So the shift of capacitance can be an indication of charges left in the floating gate. Logarithmic dependence on time was observed as has been reported.[13] This is also consistent with leakage current decay measurement at 0 V, which shows a $1/t$ dependence on time. The estimated time to lose 30% of holes is about 10^4 h, while it is about 1 h for electrons.

In the experiments, higher voltages are needed to shift the $C-V$ curve to the right, while the corresponding electron

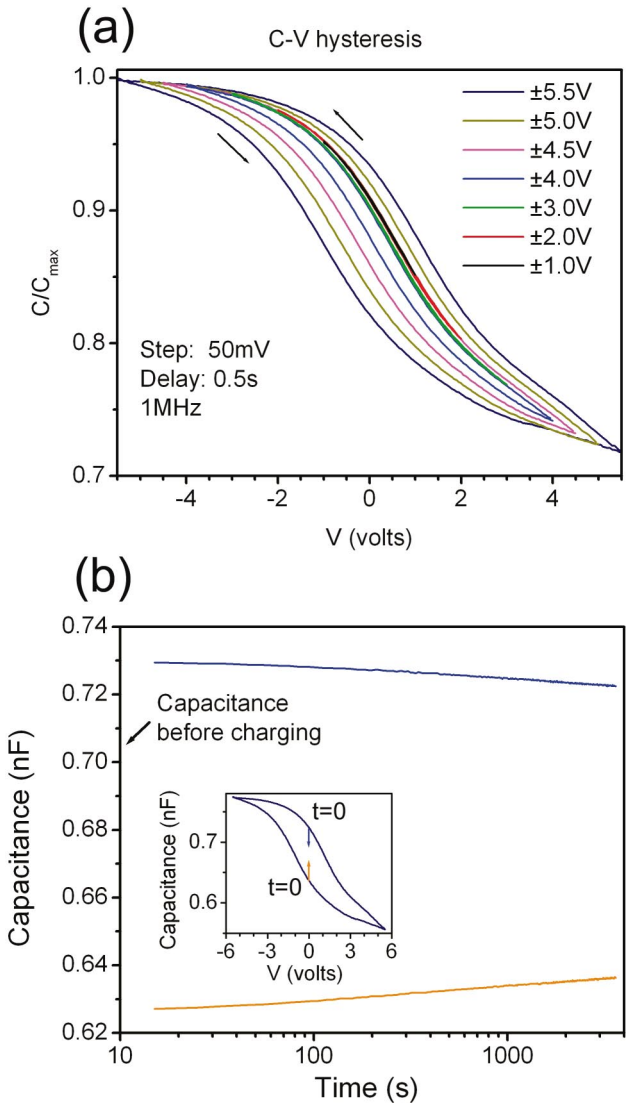

FIG. 3. (Color) (a) The $C-V$ characteristics obtained by sweeping gate voltage back and forth between different biases. For example, ±1 V indicates that gate voltage is swept between −1 and +1 V. Measurements were performed with ascending order of sweeping ranges. (b) Capacitance decay measurements at $V_G=0$ after charge injection at +5.5 V (blue curve) and −5.5 V (orange curve). The inset indicates the corresponding discharging proceedings.

discharging happens faster. To explain this phenomenon, we suggest electron tunneling occurs under positive programming voltage, and hole tunneling occurs under negative programming voltage. For Fowler–Nordheim tunneling, the energy barrier is about 4.7 eV for holes and about 3.1 eV for electrons between Si and SiO_2. So the tunneling component due to holes is much smaller than the electron tunneling component. This difference becomes smaller as the oxide thickness is scaled down into direct tunneling region, which makes hole tunneling possible.[14] During programming, an *n*-type inversion layer has to be formed inside the channel before pronounced electron tunneling from the channel to nanocrystal floating gate becomes possible. But this is not necessary for hole tunneling, which makes hole charging easier than electron charging. During discharging, the smaller loss rate for holes results from the higher tunneling barrier just mentioned. But short retention time for electrons still suggests leakage paths between nanocrystals and channel, which need be addressed to achieve an optimal memory performance.

For those $C-V$ hysteresis curves shown in Fig. 3(a), the largest voltage shift is 2 V, corresponding to a charge density of 4×10^{12} cm^{-2}. This value is probably smaller than or at most equal to the areal density of nancrystals in floating gate, indicating at most one charge per nancrystal on average. Adding a second charge is unlikely to happen due to large Coulomb charging energy for such small nanocrystals. Note that if the nanocrystal density estimated from AFM image is applied, an unlikely result of 25 charges per nanocrystal can be obtained. Obviously, use of AFM or TEM alone may lead to an inaccurate estimate of nanocrystal array density that is inconsistent with the observed electrical charging and discharging data. More accurate nanocrystal density and size measurements made by STM enable the electrical measurements to be more clearly understood.

In conclusion, structural and electrical characterization of Si nanocrystal memory fabricated by ion-implantation and annealing were performed. During structure characterization, contact-mode AFM and RHEED were applied to verify the existence of nanocrystals inside SiO_2 qualitatively. With the application of ultrahigh vacuum STM on fully etched sample, nanocrystal size and density were evaluated and STM is proved to be an effective alternative to TEM to characterize extremely small nanocrystals. In electrical characterization, memory effects were evaluated through $C-V$ measurements. The asymmetric charging and discharging processes were explained by the differences between electron tunneling and hole tunneling. Comparison between flatband voltage shift and nanocrystal density indicates no more than single charge per nanocrystal on average.

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