NANO MICRO small

Supporting Information

for *Small*,DOI: 10.1002/smll.201200940

Silicon Nanowire Charge-Trap Memory Incorporating Self-Assembled Iron Oxide Quantum Dots

*Ruo-Gu Huang and James R. Heath**

Supporting Information for DOI: 10.1002/smll.201200940

Silicon Nanowire Charge-Trap Memory Incorporating Self-assembled Iron Oxide Quantum Dots

Ruo-Gu Huang and James R. Heath[*]

[*] Dr. R. Huang and Prof. J. R. Heath

Division of Chemistry and Chemical Engineering, California Institute of Technology

1200 E. California Blvd, MC 127-72, Pasadena, CA 91125 (USA)

FAX: (+1) 626-395-2355

E-mail: heath@caltech.edu

Superlattice nanowire pattern transfer

The superlattice wafer consisting of 100 alternating layers of GaAs (60-nm) and $Al_xGa_{(1-x)}As$ (10-nm) was created by metal-organic chemical vapour deposition (MOCVD) (IQE Ltd., Cardiff, UK). The SNAP process begins by cleaving a small piece (~2-mm wide and 5-mm long) of superlattice that was served as a template for nanowire patterning. The template was then selectively etched (NH_3: H_2O_2: H_2O=1:20:300 v/v, 10s; H_2O_2, 5s; H_2O, 20s) to remove partial GaAs on the surface, leaving a comb of ~50-nm-high parallel $Al_xGa_{(1-x)}As$ ridges. A thin layer (~100 Å) of Pt was evaporated on the template to create Pt nanowires along the $Al_xGa_{(1-x)}As$ ridges. The Pt nanowires were brought into contact with the substrate coated with a thin layer of heat-curable epoxy (20 drops part A to 2 drops part B (Epoxy Bond 110, Allied High Tech Products, Ranch Dominguez, CA) plus 0.25-ml poly(methyl methacrylate) in 15-ml chlorobenzene). After epoxy curing, the entire assembly was

immersed in the etchant (H_2O_2: H_3PO_4: H_2O=1:5:50 v/v, 6~7 hr). The template was slowly dissolved to release the Pt nanowires to the substrate. The Pt nanowires served as an etch mask for directional RIE to convert the underlying thin film into a nanowire array.

Template-assisted assembly technique

The as-purchased FeO QDs (Ocean NanoTech, Arkansas) was in solution form, in which chloroform was used as the solvent. The solution was diluted by toluene to a concentration of 1 mg/ml, followed by 1 hr sonication. The resulting solution should be homogeneous without any precipitates. Before starting the template-assisted assembly, the memory chip was cooked in Remover PG (MicroChem, Massachusetts) at 150 °C for 30 min to remove any organic contamination on the surface. The clean chip was then baked (150 °C, 15 min), followed by surface functionalization with hexamethyldisilazane (HMDS). The functionalization was performed by exposing the chip to HMDS vapour in a sealed box for 15 min. The functionalized chip was soaked in the FeO QD solution and slowly withdrawn via a syringe pump (NE-1000 syringe pump, New Era pump Systems). The well-controlled speed was optimized for~ 2 mm/min to reach the best assembly result.

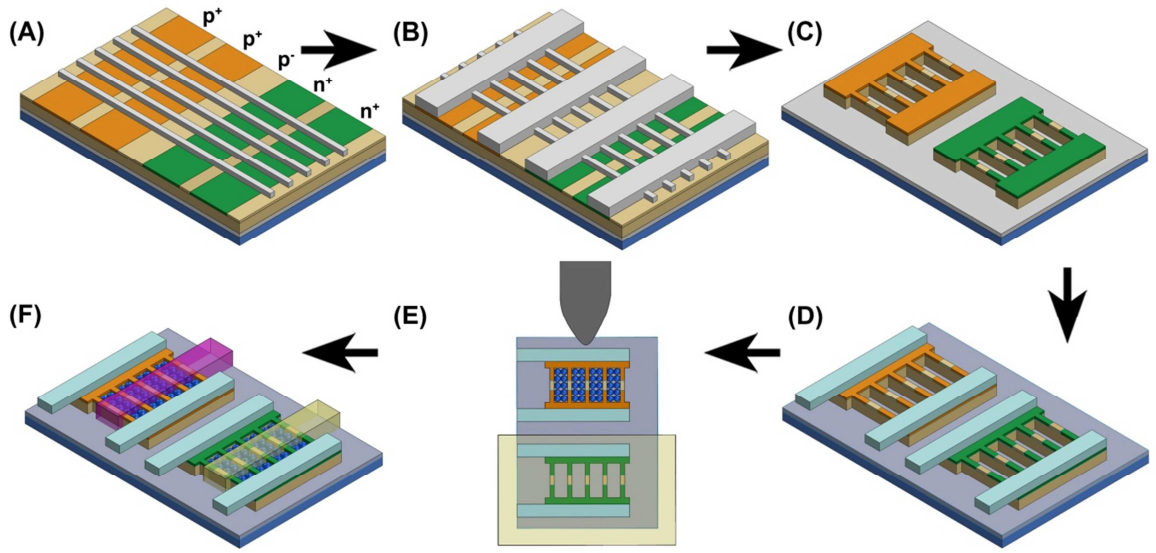


Figure S1. The device fabrication scheme. A) SNAP Pt NWs are released onto the pre-doped SOI substrate. B) An additional Pt mask is patterned over the Pt NWs to protect the micro-scale Si contacts. The mask pattern is transferred into the underlying Si with directional RIE. C) The transferred and sectioned pattern consists of lightly-doped SiNWs connected to highly-doped Si contacts. The entire pattern is fabricated from the same single crystal Si film. D) After surface treatment and source/drain metallization, a thin layer of HfO_2 is deposited as the tunnel oxide. E) The template-assisted assembly technique is carried out to align the FeO QDs into the SiNW trenches. F) The device is finished after patterning the metal gates atop the HfO_2 control oxide.

Device fabrication

Both n- and p-type memory devices were simultaneously fabricated on 6" (100) SOI wafers with a ~30-nm (100) Si film atop 250-nm buried SiO_2. The non-self-aligned doping procedure can achieve ~0.1-μm accuracy via the Moiré technique.[1] Two ion implantations were sequentially carried out to heavily dope the n- and p-type source and drain regions (phosphorus dose of 3.2×10^{14} cm^{-2} at 10 keV; boron dose of 3.8×10^{14} cm^{-2} at 5 keV, Core Systems). A 1-μm channel length was defined by the spacing between the adjacent source and drain. After cleaning, the implanted wafers were annealed under N_2 at 900 °C for 10s to activate the dopants. Next, the SNAP method[2, 3] was used to prepare highly ordered arrays of 2-mm-long, 10-nm-wide SiNWs on the pre-doped wafers. The Pt NWs were initially produced as an etch mask by using SNAP (Figure S1A). To fabricate low-resistivity micron-scale ohmic contacts, the Pt contact mask was made by using photolithography and lift-off process (Figure S1B).[4] Then the NW/micropatterned mask was transferred into the underlying silicon with a

directional reactive ion etch (RIE) (CF_4 to He 20:30, 5 mTorr, 40 W, 4 min). After metal removal and device sectioning, the resulting SiNW arrays accompanied with micron-scale Si contacts were fabricated (Figure S1C). All devices reported here have 20 SiNWs in their channel regions. Prior to source/drain metallization, the devices were cleaned and oxidized in a rapid thermal processor (O_2, 1000 °C, 35 °C/s, 15 s hold time) followed by a forming gas anneal (5% H_2 in N_2, 475 °C, 5 min). A ~4-nm thermal silicon dioxide (SiO_2) was grown to passivate the Si surface. This surface treatment can dramatically reduce the SiNW surface state density[5, 6] and significantly improve the performance metrics of SiNW FETs.[7] In addition, growing a high-quality SiO_2 on Si surface is also a key step to integrate hafnium oxide (HfO_2) gate dielectrics.[8-10] The HF-resistant Cr/Au (10-nm/50nm) interconnect was used to sustain the frequently-used HF etching process, which was used to etch HfO_2. To make good ohmic contacts, the interconnect was designed to directly contact the micro-scale Si pads (Figure S1D), on which the native oxide was removed aforehand via buffered oxide etch (BOE). In our memory devices, the high-κ HfO_2 was utilized as the tunnel and control oxide. Compared to SiO_2, HfO_2 has two major advantages. First, the lower electron/hole barrier height to SiNWs can enhance the tunnel current to accelerate the program operation.[11, 12] Second, the larger dielectric constant allows the HfO_2 tunnel oxide to have much thicker physical thickness while keeping the same electrical equivalent oxide thickness (EOT).[11-13]. A thicker HfO_2 tunnel oxide can improve the data retention performance by reducing the gate leakage current. Herein a ~6.4nm-thick HfO_2 was conformally coated onto the substrate using atomic layer deposition (ALD).

Figure S1E illustrates the template-assisted assembly technique[14-16] that was used to align FeO QDs into the SiNW trenches. The substrate was first baked to remove the surface moisture, followed by the chemical functionalization with hexamethyldisilazane (HMDS). The entire substrate was then soaked into the FeO QD solution (FeO QDs in chloroform, Ocean NanoTech) and slowly withdrawn via a syringe pump. The FeO QDs were self-assembled to form a close-packed matrix (Figure 1(c)) inside the SiNW trenches via interfacial capillary force and geometric confinement[15]. Both solution

concentration and withdraw speed were carefully optimized to get a well-packed FeO matrix. This assembly technique can apply to varying-sized FeO QDs to reach a controllable packing density (Figure 3A). The assembled FeO QDs can offer numerous available DOS to store the injected charges. A thick layer of HfO_2 (~18.9-nm) was then deposited as the control oxide to block the injected charges. Before the device characterization, the HfO_2 atop the probing pads was completely removed by repeating the HF wet etching. Thus, the HF-resistant Cr/Au was used as the interconnect to avoid the metal corrosion. The device fabrication was finalized by patterning the top metal gates, as shown in Figure S1F.

The charge transport mechanism of the memory devices

The current density of Fowler-Nordheim (F-N) tunneling has the form[17]

$$J = A \cdot E^2 \cdot \exp\left(\frac{-B}{E}\right) \quad (1)$$

where E is the electric field, and A and B are constants in terms of effective carrier mass and energy barrier height. Equation (1) can be rewritten as

$$\ln\left(\frac{J}{E^2}\right) = \ln(A) - \frac{B}{E} \quad (2)$$

A plot of equation (2) is known as F-N plot. If the charge transport is dominated by F-N tunneling, its F-N plot shows the linear dependence on the inverse of electric field.

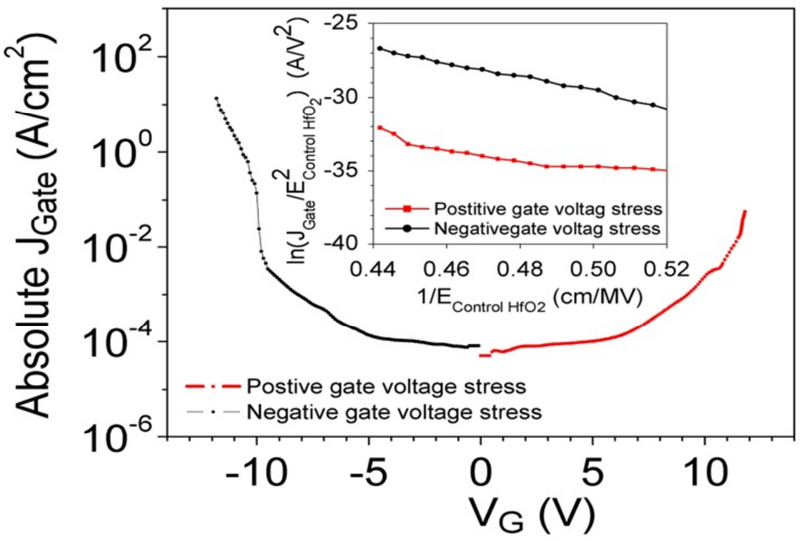


Figure S2. The transfer characteristics of the gate current density as a function of gate voltage. The tested memory device has ~8.8-nm tunnel oxide, ~15.8-nm control oxide and 10-nm FeO QDs.

To determine the transport mechanism of our memory devices, the gate current as a function of gate voltage is measured. The gate current density can be obtained by dividing the gate current by the SiNW surface area, as shown in Figure S2. The current density starts to increase rapidly when the absolute gate voltage is greater than 10V. The inset shows the device F-N plot biased at high gate voltage, ranging from 9.5V-12V. The result exhibits the linear dependency on 1/E, which demonstrates F-N tunneling is the transport mechanism of our memory devices.

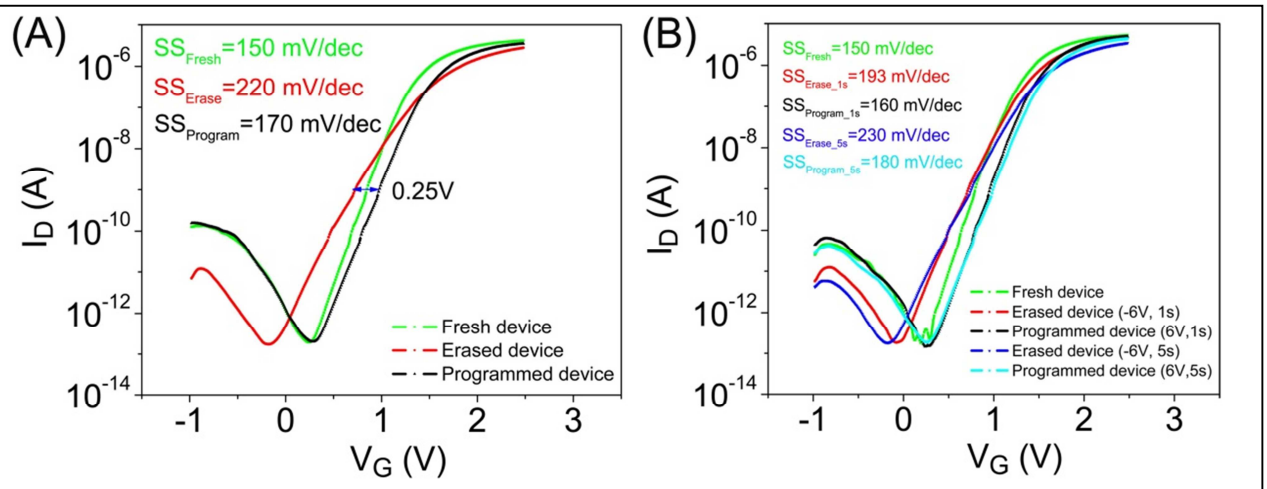


Figure S3. The transfer characteristics of n-type memory devices biased at ±8V (A) and ±6V (B) gate voltage. Compared to the p-type counterparts, the n-type devices have smaller memory window under the same gate bias. Furthermore, they are more vulnerable to gate voltage stress, which can be represented by the increasing subthreshold swing (SS). A large SS degradation is observed after one program/erase operation is performed.

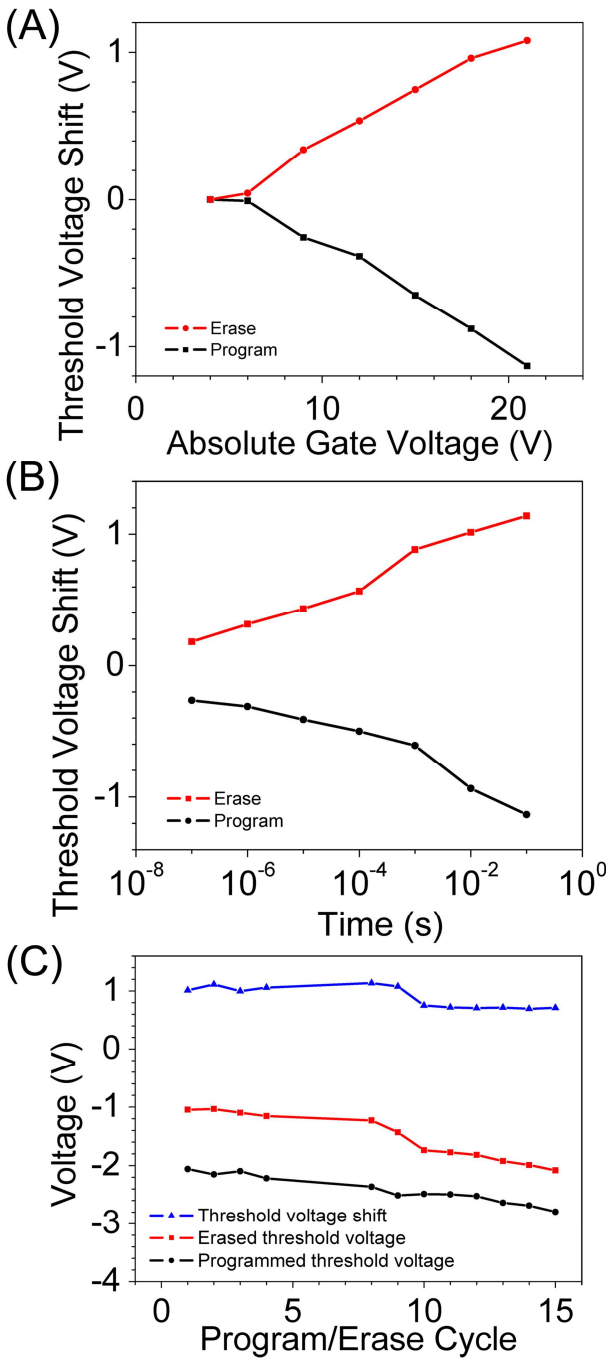
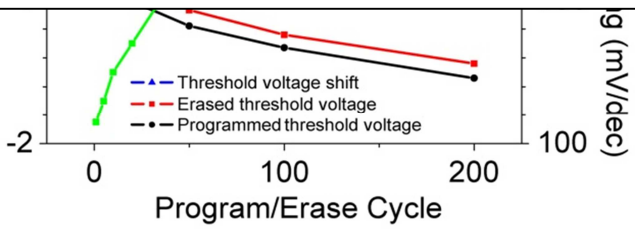


Figure S4. A) Evolution of the threshold voltage shift as a function of gate voltage. The program/erase duration is set to 52.5 ms. B) The device speed test. The erase/program voltage is set to +/- 21 V. C) All tests use the same memory device that integrates 10-nm FeO QDs.



Calculation of the capacitive coupling ratio of a memory device

The capacitive coupling ratio of the memory device can be calculated based on the simplified model shown in Figure S6. The equivalent capacitor of each layer is modeled by its physical thickness (t) and the dielectric constant (ε_r). The following is the parameters used in this calculation. Control HfO_2: t = 18.9 nm, ε_r = 15.9; FeO QD: t = 10 nm, ε_r = 14.2; Tunnel HfO_2: t = 6.4 nm, ε_r = 15.9; Passivation SiO_2: t = 4 nm, ε_r = 3.9. The calculated capacitor ratio is as follows: $C_{C\text{-}HfO2} : C_{QD} : C_{T\text{-}HfO2} : C_{SiO2}$ = 0.863 : 1.456 : 2.548 : 1.

To keep charge conservation, the ratio of voltage drop across each capacitor is inversely proportional to its capacitor value. Thus, the ratio of the voltage drop across the SiO_2 to the applied gate voltage is given by

$$\gamma = \frac{V_{SiO_2}}{V_{Gate}} = \frac{{}^{1}/_{C_{SiO_2}}}{{}^{1}/_{C_{C-HfO_2}} + {}^{1}/_{C_{QD}} + {}^{1}/_{C_{T-HfO_2}} + {}^{1}/_{C_{SiO_2}}} \quad (3)$$

Substitute the capacitor ratio into equation (1), the value of γ is ~0.31. For the device that was tested at a gate voltage of +/- 21V, a 6.5-V voltage drop across the 4-nm SiO_2 can result in an electric field (~1.6 × 10^7 V/cm) higher than its dielectric strength (10^7 V/cm). We can reduce γ by using thicker control oxide (smaller $C_{C\text{-}HfO2}$) or larger FeO QDs (smaller C_{QD}).

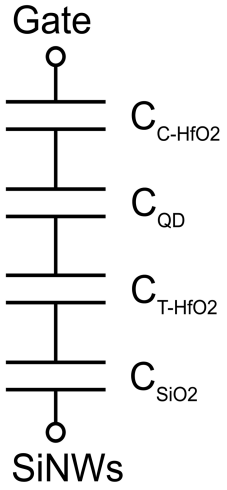


Figure S6. The simplified capacitor model of the memory device.

Calculation of the average number of stored charges per FeO QD

To estimate the total stored charges in the memory device, we first need to know the total capacitance of the control oxide. It can be approximated[18] by

$$C_{C-HfO_2} = \frac{N_{eff} \cdot 2\pi \cdot \varepsilon_{HfO_2} \cdot {r_{QD}}^2}{t_{C-HfO_2} + \frac{\varepsilon_{HfO_2}}{\varepsilon_{QD}} \cdot r_{QD}} \quad (4)$$

where N_{eff} is total number of QDs, r_{QD} is the radius of FeO QDs, $t_{C\text{-}HfO2}$ is the control oxide thickness, ε_{HfO2} and ε_{QD} are the permittivities of HfO_2 and FeO QD, respectively. The total stored charges, N_{Charge}, can be described by

$$N_{Charge} = \frac{C_{C-HfO_2} \cdot \Delta V_{TH}}{q} \quad (5)$$

here ΔV_{TH} is the threshold voltage shift. The average number of stored charges per FeO QD, n_{Charge},can be expressed as

$$n_{Charge} = \frac{N_{Charge}}{N_{eff}} = \frac{2\pi \cdot \varepsilon_{HfO_2} \cdot {r_{QD}}^2 \cdot \Delta V_{TH}}{q \cdot (t_{C-HfO_2} + \frac{\varepsilon_{HfO_2}}{\varepsilon_{QD}} \cdot r_{QD})} \quad (6)$$

From our statistic data, the average ΔV_{TH} of 18- and 5-nm FeO QDs are -0.418 and -0.156 V, respectively. Substitute the following parameters ($t_{C\text{-}HfO2}$ = 14.2 nm, ε_{HfO2} = 15.9, ε_{QD} = 14.2) into

equation (6), the calculation shows each18-nm FeO QD holds ~7.7 unit charges but each 5-nm FeO QD only holds 0.3 unit charges. The result implies the charging energy of FeO QDs, which can be expressed as $q^2/(8\pi\times\varepsilon_{HfO2}\times r_{QD})$,[18] dominates the charge transport of this type of memory devices.

REFERENCE

[1] M. C. King, D. H. Berry, *Appl. Opt.* **1972**, *11*, 2455.

[2] N. A. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P. M. Petroff, J. R. Heath, *Science* **2003**, *300*, 112.

[3] J. R. Heath, *Acc. Chem. Res.* **2008**, *41*, 1609.

[4] D. Wang, Y. Bunimovich, A. Boukai, J. R. Heath, *Small* **2007**, *3*, 2043.

[5] S. Wolf, *Silicon Processing for the VLSI Era Volume 2 –Process Integration*, Lattice Press, California, USA, **1990**.

[6] K. I. Seo, S. Sharma, A. A. Yasseri, D. R. Stewart, T. I. Kamins, *Electrochem. Solid-State Lett.* **2006**, *9*, G69.

[7] R.-G. Huang, D. Tham, D. Wang, J. Heath, *Nano Res.* **2011**, *4*, 1005.

[8] T. Rudenko, N. Collaert, S. De Gendt, V. Kilchytska, M. Jurczak, D. Flandre, *Microelectron. Eng.* **2005**, *80*, 386.

[9] M. J. H. van Dal, N. Collaert, G. Doornbos, G. Vellianitis, G. Curatola, B. J. Pawlak, R. Duffy, C. Jonville, B. Degroote, E. Altamirano, E. Kunnen, M. Demand, S. Beckx, T. Vandeweyer, C. Delvaux, F. Leys, A. Hikavyy, R. Rooyackers, M. Kaiser, R. G. R. Weemaes, S. Biesemans, M. Jurczak, K. Anil, L. Witters, R. J. P. Larder, P. Japan Soc Appl, in *2007 Symp. VLSI Technol., Dig. Tech. Pap.*, Kyoto, Japan, 2007, 110.

[10] C. A. Richter, H. D. Xiong, X. Zhu, W. Wang, V. M. Stanford, W.-K. Hong, T. Lee, D. E. Loannou, Q. Li, *IEEE Trans. Electron Devices* **2008**, *55*, 3086.

[11] J. J. Lee, X. G. Wang, W. P. Bai, N. Lu, D. L. Kwong, *IEEE Trans. Electron Devices* **2003**, *50*, 2067.

[12] Y. M. Cai, R. Huang, X. N. Shan, Y. Li, F. L. Zhou, Y. Y. Wang, *Semicond. Sci. Technol.* **2006**, *21*, 507.

[13] G. Chakraborty, C. K. Sarkar, *J. Appl. Phys.* **2008**, *104*.

[14] K. Xu, L. Qin, J. R. Heath, *Nat. Nanotechnol.* **2009**, *4*, 368.

[15] Y. N. Xia, Y. D. Yin, Y. Lu, J. McLellan, *Adv. Funct. Mater.* **2003**, *13*, 907.

[16] Y. Cui, M. T. Bjork, J. A. Liddle, C. Sonnichsen, B. Boussert, A. P. Alivisatos, *Nano Lett.* **2004**, *4*, 1093.

[17] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, New York, USA, **1981**.

[18] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, Y. Lee, *IEEE Electron Device Lett.* **1997**, *18*, 278.