Differential Amplifier With Regulator Achieves HIGH STABILITY, LOW DRIFT

Unique circuit configuration of this direct-coupled differential amplifier makes possible low drift and high common-mode rejection ratio. Meets requirements of missile telemetry systems

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WHEN d-c signals are to be amplified, the usual approach is to use a direct-coupled circuit. The difficulty of maintaining sufficiently low drift in a direct-coupled configuration led to the development of chopper and chopper-stabilized circuits, where a mechanical chopper reduces drift to low values. Unfortunately, other shortcomings arise, and in most applications the direct-coupled d-c amplifier would be preferable if the drift could be reduced to an acceptable value. The advantages over the chopper or the chopper-stabilized types include rapid recovery from overload, freedom from hash, simplicity and small size due to absence of transformers and capacitors.

A d-c amplifier for airborne or missile telemetry use must meet many specifications. The usual requirements for differential input, single-ended output, signal levels and linearity are easy to meet. Those which are difficult to achieve, especially simultaneously, are low drift over a wide temperature range, stable though adjustable gain, wide frequency response, high input impedance, high common-mode rejection factor, insensitivity of performance to source resistance, small size, weight and low power requirements. The d-c amplifiers described here provide exceptional performance in all these respects simultaneously. There is no unique set of specifications, since the design can be tailored for particular applications.

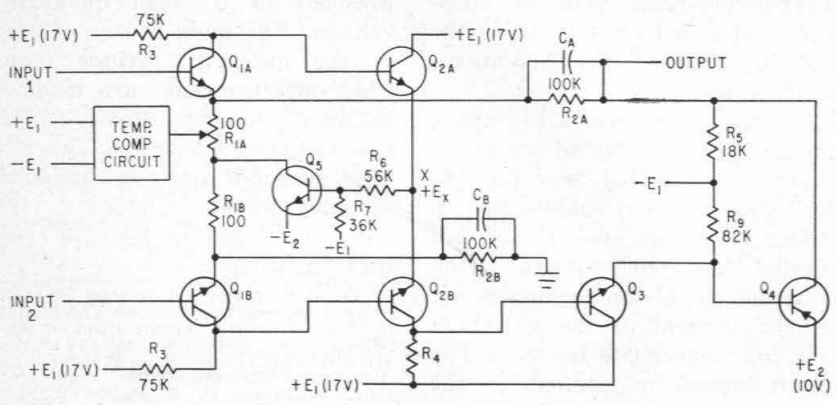
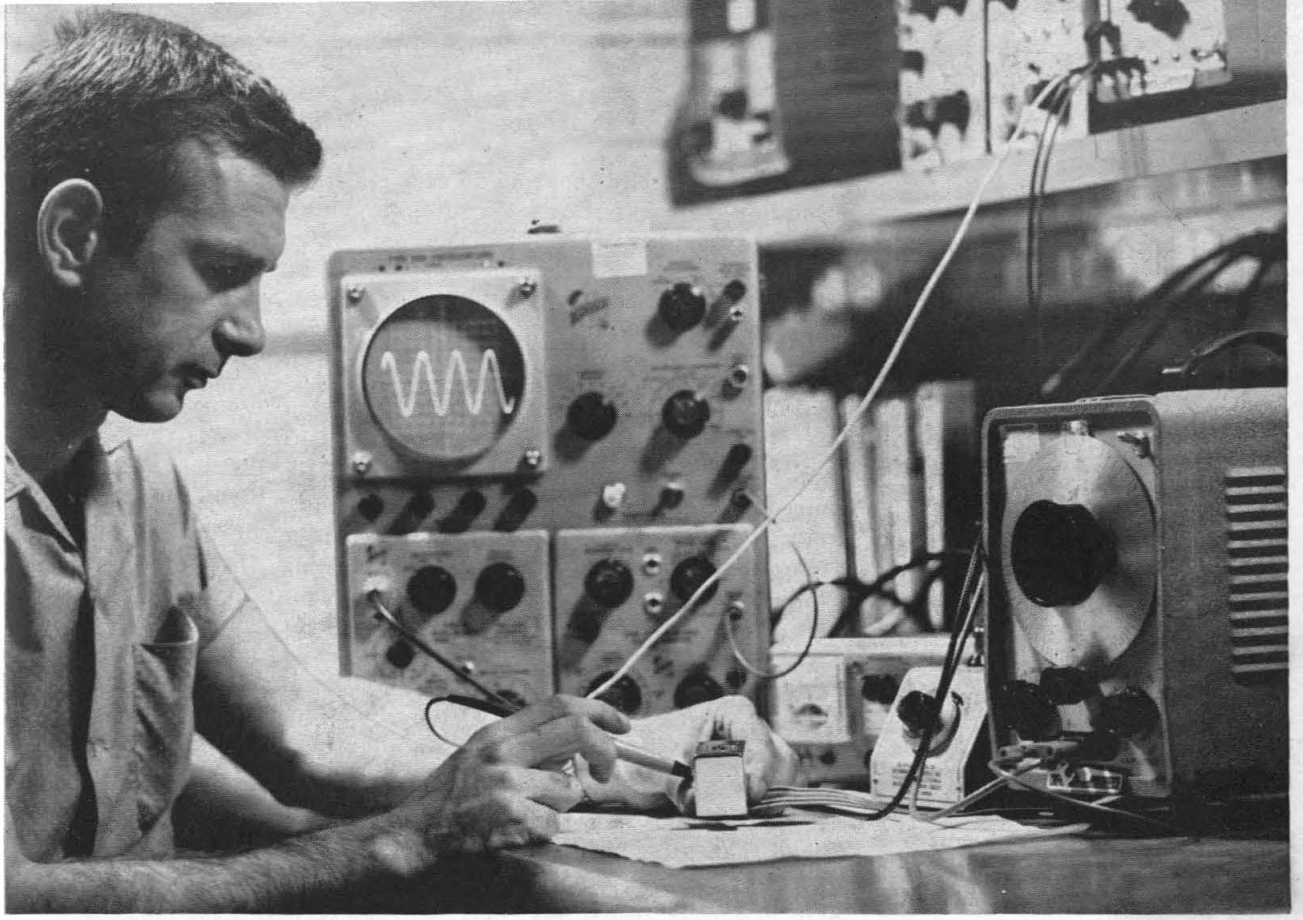


FIG. 1—Basic circuit of the amplifier. Voltages E_1 and E_2 are obtained from a reference diode string fed from the power supply. Resistor R_9 serves as a gain control

The following figures are typical: gain stability ±0.75 percent; frequency response ±1 percent to 10 Kc, 3 db down at 50 Kc; differential input resistance greater than 1 megohm; common-mode rejection factor 120 db to 400 cps, 100 db to 2 Kc, for common-mode voltage ±5 v peak and for a gain of 1,000. The gain is adjustable over a 2-to-1 range with maximum preset to any value between 200 and 1,000. For a gain of 1,000 the maximum differential input signal is ±5 mv peak. The output capability is ±5 v into 20,000 ohms with output re-



The low-drift transistor d-c amplifier under test. To alleviate temperature problems, differential amplifier uses a pair of matched transistors in one can

sistance less than 100 ohms, and with up to 100 percent offset adjustment. The drift is to some extent a function of the signal source and a typical equivalent input drift is ± 100 μv for eight hours over a temperature range of 25 C to 100 C.

For extreme temperature environments, an amplifier is available with an internal heater so that eight-hour input drifts of ± 100 μv can be maintained over ambient temperatures from -55 C to 100 C. Size and weight are tailored to meet environments, and are typically 3 cubic inches and 4 ounces for the heaterless models. Required power supplies are 20 ma at plus and minus not less than 18 v ± 1 percent. The model containing a heater is about 7.5 cubic inches, weighs 6 ounces, and requires an additional input of up to 300 ma (for -55 C ambient) at $+28$ v unregulated.

The circuit of the heaterless d-c amplifier is shown in Fir. 1. Transistors Q_{1A} and Q_{1B} form a differential first stage, Q_{2A} and Q_{2B} a differential second stage, and Q_3 and Q_4 form the single-ended third and fourth stages. Overall negative feedback is taken from load resistance R_5 and applied in series with the differential input. Resistance R_5 is an internal load; any external load is connected between output and ground. The circuit is inherently capable of converting a differential input to a single-ended output, and is superior in three respects to a circuit which is differential throughout and in which only one output of the two is used: the output resistance is considerably lower for the same loop gain, much better common-mode rejection is obtained, and fewer transistors are required.

With zero input signal, there is no voltage between the output terminal and ground. Internal load resistance R_5 is connected to negative supply voltage E_1 to permit operating current to flow in output stage Q_4 under quiescent conditions.

With a differential input signal, input 1, for example, goes positive and input 2 goes an equal amount negative. The current in Q_{1A} increases while that of Q_{1B} decreases. The current changes in resistances R_3 (both) cause the input voltage to Q_{2A} to decrease and that of Q_{2B} to increase. The increased current in Q_{2B} causes an increased voltage drop across R_4, and reduces the input voltage to emitter-follower stage Q_3. The lower emitter voltage of Q_3 causes an increase in the base-emitter voltage of Q_4, hence Q_4 conducts more current through R_5 and the output voltage goes up. A resistance from the emitter of Q_3 to negative supply voltage $-E_1$, to provide correct operating current, is not shown in the schematic. A fraction of the voltage between output and ground is injected in series with the input through negative feedback path R_{2A}, R_{1A}, R_{1B} and R_{2B}.

Transistor Q_5 does not act as a constant-current sink for the currents in R_{1A} and R_{1B}, as it would if resistance R_6 were returned to a fixed supply voltage. Instead, the connection allows Q_5 to fulfill two important requirements. Imagine that the half of the circuit containing Q_{1B} and Q_{2B} is folded over to lie on top of the half containing Q_{1A} and Q_{2A} (see Fig. 2). The path

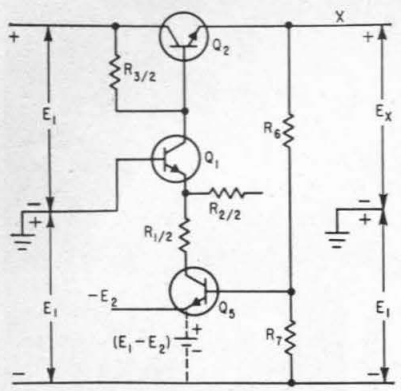


FIG. 2—Differential stages folded over and drawn to reveal a voltage regulator circuit

from point X through Q_5, $Q_{1A,B}$ and $Q_{2A,B}$ back to point X is a voltage regulator circuit in which $(E_1 - E_2)$ is the reference, and $(E_X + E_1)$ is the regulated output voltage. Transistor Q_5 is the error amplifier, and Q_2 is the series element whose current is controlled by Q_5[1]. Transistor Q_1 does not contribute to this mode of operation of the circuit, and serves merely to transmit the collector current variations of Q_5 to the base of Q_2.

The voltage between X and the negative suply $-E_1$ is constrained to be closely equal to $(E_1 - E_2)(R_6 + R_7)/R_7$. The higher the common-mode loop gain, designated G_c, the more highly regulated will be the voltage E_X at X. Since the voltage across each R_3 is approximately $E_1 - E_X$, the collector currents of Q_{1A} and Q_{1B} are stabilized, which is the first of the two functions of Q_5. Each collector current is set to 100 μa, this low value being chosen to make the noise contributions of Q_{1A} and Q_{1B} small, and to allow a large value of R_3 which makes the common-mode loop gain G_c large.

To understand the second function of Q_5, it must be recognized that in the presence of arbitrary voltages at the two amplifier inputs, the collector current of Q_5 contains both differential and common-mode components. These result from conditions imposed by the feedback path. A high value of G_c permits the collector current of Q_5 to adjust as required to the inputs, while the collector currents of Q_{1A} and Q_{1B}, and hence their base currents, hardly change. Thus, the second function of Q_5 is to maintain high signal impedances at the inputs to Q_{1A} and Q_{1B}.

There is typically about 45 db of overall negative feedback in the complete amplifier, which implies a differential loop gain of about 200. This high value ensures low output resistance, high differential input resistance, and stable gain determined essentially by the feedback elements. Close, but not necessarily exact, equality between R_{1A} and R_{1B}, and between R_{2A} and R_{2B}, is required. Under these conditions, gain G_1 from input 1 and gain G_2 from input 2 may be written $G_1 = (R_{1A} + R_{2A})/R_{1A}$

$$G_2 = G_1\left[1 + \frac{R_1}{R_2}\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2}\right)\right]$$

where $R_{1A} \approx R_{1B} \approx R_1$, $R_{2A} \approx R_{2B} \approx R_2$, $R_{1B} - R_{1A} = \Delta R_1$, and $R_{2B} - R_{2A} = \Delta R_2$. For a gain of 100, typical values are $R_1 = 1$ K and $R_2 = 100$ K, hence for small percentage unbalances $\Delta R_1/R_1$ and $\Delta R_2/R_2$ the gain G_2 is very nearly the same as G_1. Both gains are determined by R_{1A} and R_{2A}, with only weak dependence on R_{1B} and R_{2B}. The frequency response of the amplifier can be controlled by capacitance C_A, with only weak dependence on C_B.

The degree of rejection of common-mode input signals is sensitive to asymmetry in the resistance pairs R_1 and R_2. The amplifier common-mode rejection factor C, defined as the ratio of the common-mode input voltage to the differential input voltage which produces the same output voltage, is given by

$$\frac{1}{C} = \left[\frac{\Delta R_1}{R_1}\left(1 - \frac{1}{G_c}\right) - \frac{\Delta R_2}{R_2}\right]\Big/ G$$

where $G_1 \approx G_2 \approx G$, and G_c is the common-mode loop gain previously defined. The value of C is maximized by adjustment of R_{2B} and C_B, which may be designated as common-mode adjustments with negligible effect on the gain or on the frequency response. However, the converse is not true. Any attempt to alter the gain by changing R_{2A} would have a disastrous effect on the common-mode rejection factor. Means must be found to change the effective ratio of R_{1A} to R_{2A} without destroying the symmetry.

Gain variation can be accomplished by bridging a gain control resistance between symmetrical tapping points on R_{2A} and R_{2B}, as shown in Fig. 3A. In the gain equations, R_{2A} (or R_{2B}) should then be replaced by the effective value R_{2E} given by $R_{2E} = R_2 + 2(R_1 + R_3)(R_2 - R_3)/R_3$.

It is possible to achieve gains variable over a two-to-one range without interaction between the gain and common-mode adjustments.

Care must also be taken to avoid upsetting the optimum common-mode rejection when changing the quiescent output level. The most convenient way to introduce an output level control which satisfies this requirement is to remove R_{2B} from its ground connection and to return it to the slider of a potentiometer across the supply voltages. The impedance level of the potentiometer must be low enough that the effective value of R_{2B} is changed by an acceptably small percentage throughout the desired level range, to avoid undue degradation of the common-mode rejection factor. Alternatively, the common-mode adjustment can be reset for a particular output voltage level.

In the presence of a level control, the lower output terminal remains at ground, as shown in Fig. 3B.

The amplifier common-mode rejection factor is sensitive to unbalance in the signal source resistances. If the rejection factor is adjusted to be infinite with equal source resistances, the common-mode rejection factor C' in the presence of an unbalance ΔR_s in the source resistances is given by $1/C' = \Delta R_s/\beta_1 R_2 G_c$ where β_1 is the common-emitter current gain of Q_{1A} or Q_{1B}. It is the absolute and not the percentage unbalance of the source resistances which is significant. A typical value for C' is 10^6, or 120 db, for $\Delta R_s = 100$ ohms, therefore the common-mode rejection factor is little affected by normal source resistance unbalances.

Although the above description of the amplifier indicates excellent characteristics with respect to its signal-handling capabilities, the crucial test of a d-c amplifier is its drift performance. Drift in a direct-coupled d-c amplifier origi-

nates almost exclusively in the differential input transistors, and arises primarily because of aging and temperature changes in the saturation currents, the base-emitter voltages, and the current gains. Use of silicon transistors with room temperature saturation currents in the order of 1 na (millimicroamp) effectively eliminates this source of drift with normal low-impedance signal sources such as strain gages and thermocouples. However, the other two drift sources are important.

The base-emitter voltage of a silicon transistor is stable with time but exhibits marked temperature dependence, decreasing by approximately 2 mv for every degree centigrade rise in temperature. Even though the base-emitter voltage drops of Q_{1A} and Q_{1B} are in series opposition, and even if Q_{1A} and Q_{1B} are exactly matched, an equivalent input drift of 20 μv will result for every 0.01 deg C temperature differential between these two transistors. The availability of two matched transistors in one can, the FSP-2 of Fairchild Semiconductor Corp., has alleviated the problem of temperature differentials.

In addition to this effect, there is also a drift source due to unavoidable unbalance in the temperature dependences of the base-emitter voltages in Q_{1A} and Q_{1B}. In the double unit, the values of dV_{be}/dT are typically matched to about 1 part in 100, but even this would give rise to an equivalent input drift of 20 μv for every degree change in ambient temperature. This is unacceptable, but because the base-emitter voltage at constant current is closely linear with temperature, compensation is possible. The compensation function is provided by an auxiliary circuit which supplies a current linearly dependent on temperature.[2] As shown in Fig. 1, this current is injected at a tapping point on the resistance R_{1A} or R_{1B}, thus generating a voltage in series with the inputs which is linearly dependent on temperature. Adjustment of the tapping point permits the inherent unbalance of dV_{be}/dT in Q_{1A} and Q_{1B} to be reduced by a factor of as much as 100. The equivalent input drift from this cause can be held to about 20 μv over a range of 100 deg C. This high degree of cancellation depends upon closely equal temperatures of Q_{1A}, Q_{1B} and the compensating circuit, an equality which is in turn limited by the thermal design.

The remaining source of drift is the variability in the current gains of Q_{1A} and Q_{1B}. Since the collector current of each transistor is stabilized by Q_5, each base current flows through the resistance of its signal source and thereby gives rise to a spurious input signal. It is apparent, that the drift performance of the amplifier cannot be specified independently of the signal-source characteristics. However, performance can be so specified that the expected drift can be determined for a particular source configuration. A typical value for the current gain of a double unit is 40 at 25 C, with a possible unbalance between the two units of about 10 percent. Since in the amplifier each collector current is stabilized at 100 μa, each base current is nominally 2.5 μa at 25 C. If the ambient temperature increases, each base current decreases fairly linearly at about 15 na/deg C, again with a possible unbalance between the two units of about 10 percent. These figures make possible an estimate of the temperature drift in the presence of given source resistances. For example, if the source resistance in series with each input is 0.5 K, then an equivalent input drift up to ± 0.1 $(0.5 \times 15) = \pm 0.75$ μv per deg C could be expected. The fact that this drift is approximately linear with temperature permits compensation. If the source resistance is known, drift due to current gain changes can be cancelled along with that due to base-emitter voltage changes and it is necessary to set the temperature compensation adjustment in the presence of the desired source resistances. There then remains only drift due to the varying base current flowing in any unbalanced source resistance. For example, if the 500 ohm source resistances were unbalanced by 5 ohms, an uncompensated equivalent input drift of about 0.075 μv per deg C would result.

The examples indicate the dependence of the amplifier drift performance on the signal-source configuration. If the drift thus obtainable is undesirably great, or if independence of the source configuration is desired, it is necessary to use an internal heater to eliminate temperature-dependent changes in the amplifier parameters. The heater used in these amplifier models is continuously controlled by an internal subsidiary amplifier referenced to a thermistor sensor, and the main amplifier temperature is maintained very nearly constant. As a result, low drifts can be achieved over wide ambient temperature ranges.

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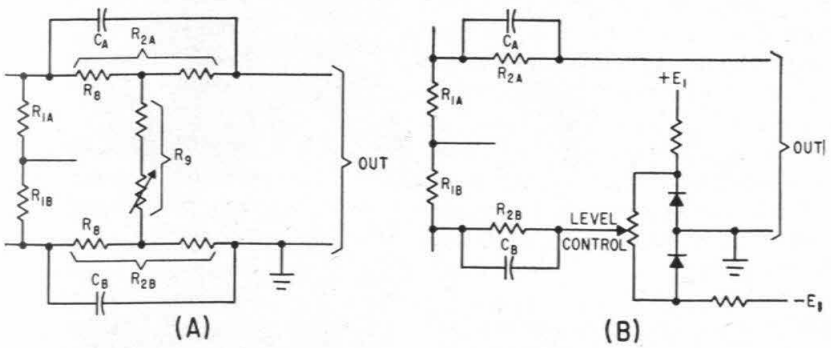

FIG. 3—Introduction of a gain control by bridging resistance across symmetrical tapping points on R_{2A} and R_{2B}, in (A); introduction of a level control by connecting R_{2B} to a low-impedance potentiometer across a bias voltage, (B)

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