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Three-dimensional etching of silicon for the fabrication of low-dimensional and suspended devices†

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In order to expand the use of nanoscaled silicon structures we present a new etching method that allows us to shape silicon with sub-10 nm precision. This top-down, CMOS compatible etching scheme allows us to fabricate silicon devices with quantum behavior without relying on difficult lateral lithography. We utilize this novel etching process to create quantum dots, quantum wires, vertical transistors and ultra-high-aspect ratio structures. We believe that this etching technique will have broad and significant impacts and applications in nano-photonics, bio-sensing, and nano-electronics.

Recently silicon has undergone a rebirth as both the electronic and optical material of choice – combining both ease of processing and the availability of low-cost substrates.[1] Specifically, advances in fabrication techniques and methods have produced new low-dimensional structures such as nanowires, nanopillars and quantum dots that can exhibit fundamentally new behavior not seen in bulk silicon. While devices made with these new methods can display remarkable optical, mechanical and electronic effects[2–4] the fabrication strategies utilized tend not to be CMOS compatible, relying on stochastic bottom-up synthesis or requiring specialized silicon on insulator substrates. Examples of these methods include the creation of silicon nanowires *via* vapor–liquid–solid (VLS) growth employing metals such as copper or gold as catalysts[5] and the stochastic precipitation of silicon quantum dots from silicon rich oxide or nitride.[6]

The ability to construct such three-dimensional structures with top-down, CMOS compatible fabrication has several advantages. The deterministic nature of top-down fabrication allows for the alignment of multiple contact or gate layers to individual nanoscale devices using optical lithography. This allows any created structure to be immediately produced and integrated at the wafer scale rather than as a one-time device. Furthermore, CMOS compatibility ensures that devices can be produced by existing silicon foundries with minimal delay. Finally, the capacity to construct three-dimensional devices, perpendicular to the bulk substrate, allows for denser placement of devices as the footprint of the device does not appreciably expand when source, drain, or gate regions are added.

In terms of top-down, three-dimensional fabrication there have been several methods explored to fabricate silicon nanostructures. These approaches can be split into two main categories – wet and dry processing. Wet processing methods which produce the best results utilize hydrofluoric acid as the etchant in conjunction with an electrochemical current to serve as the catalyst.[7–9] While this has proven successful and could possibly be adapted to work in a fabrication line, the method lacks the fine control to precisely shape silicon at the nanometer scale. Various dry approaches, utilizing cryogenic[10] or chopped Bosch[11] plasma etching techniques, have begun to approach three-dimensional silicon sculpting but still rely on complicated planar electron beam lithography to create sub-10 nm features.

Here we demonstrate the fabrication of three-dimensional silicon devices using a novel, top-down, CMOS compatible etching technique. With this method it is possible to manipulate silicon with sub-10 nanometer precision and create fully suspended structures without the use of sacrificial layers or critical point drying. Moreover, the ability to shape silicon in three dimensions at such scales also allows the geometric tuning of the bandgap and the creation of quantum dots and heterojunctions out of bulk, single crystal silicon.

Previously, we reported[12] on the use of aluminum oxide as a robust etch mask with respect to a fluorine plasma etch chemistry. Alumina has the dual benefits of yielding a non-volatile fluorine etch product and being a hard material. The deposition and patterning of the aluminum oxide masks used in this communication are done by reactive sputtering and electron beam lithography, respectively, and are discussed in detail in the ESI†.[12] Although we have found alumina to be the

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most effective mask material, the results in this paper can be replicated with a suitably strong resist or a hard-mask. While electron beam lithography is used to pattern the devices discussed in this communication, the minimum written feature size (≥50 nm) can be replicated with state-of-the-art optical lithography.

The etching process presented in this communication is based on the mixed-mode 'pseudo-Bosch' process[12] that utilizes simultaneous etching (with SF_6) and passivation (with C_4F_8). We have seen that this etch chemistry is not orientation dependent and from our testing we have found that it etches (100), (110), and (111) silicon wafers identically. The etching is conducted in an inductively coupled plasma reactive ion etcher (ICP-RIE). The use of the ICP allows for independent control of the degree of gas species ionization (ICP power) from the forward (RF) power that accelerates ions towards the sample. This gives a unique capacity to tune the physical and chemical character of the etch.

It is important to note that the ions accelerated by the forward power in the ICP-RIE etcher are not perfectly perpendicular to the substrate; rather these ions have a small angular spread defined as the ion angular distribution (IAD).[13] The spread is a result of collisions between the ions and other gas species within the plasma and is a function of the pressure within the chamber. The ion collimation can be improved by increasing the forward power, at the expense of mask lifetime, leading to a greater amount of forward angle scattering. The main consequence of broad IAD is a lateral etching underneath the masked regions, known as mask 'undercut,' that becomes more severe as the etch progresses into the substrate. This lateral etching rate is usually a small fraction of the vertical etching rate. However over the course of a deep etch, the undercut can have a significant effect on the feature size.

In order to create devices with vertical side-walls[12] the flow rates of SF_6 and C_4F_8 are tuned such that the forward power allows the etching ions to mill only through the C_xF_y coating on the horizontal surfaces leaving a fluorinated polymer coating on the side-walls. Thus the etch progresses into the substrate with the lateral dimensions solely defined by the extent of the mask. Fig. 1a shows an array of 50 nm diameter nanopillars etched to a depth of 1 micron using the pseudo-Bosch method.

By modifying the conditions within the chamber during etching it is possible to sculpt the profile of silicon as the etch progresses into the substrate. If we simply reduce the flow of the passivation gas, the ion bombardment due to the IAD will overcome the deposition of polymer on the side-walls, causing lateral etching underneath the mask. This undercut becomes progressively greater as the etch proceeds into the substrate; the effect is shown in Fig. 1b through the narrowing of the pillar diameter with etch depth. In order to make vertically uniform structures, this behavior can be compensated by reducing the IAD spread as a function of etch depth. This allows the etch to progress vertically at a *fixed* undercut for the entirety of the process – replicating the masked region at a smaller scale defined by the reduction in the ratio of passivation to etch gas. This technique transfers challenging lithographic tolerances into easily controlled etch parameters – an example of this is seen in Fig. 1c. Rather than attempting to pattern a 15 nm diameter disk to create a 15 nm vertical nanopillar, we defined a 50 nm disk and used the fixed undercut to scale the mask down in size. A head and a foot region, etched under zero undercut conditions, are added to the structure for purposes of electrical contacting and mechanical stability, respectively. By tuning the forward power and passivation gas flow we can specify the morphology of the side-wall as the etch progresses deeper into the substrate. If the passivation gas flow rate is rapidly oscillated between under and over passivation a series of linked beads can be fabricated in a vertical stack. Fig. 1d shows the creation of a scalloped structure with several different sized diameter beads that are each 75 nm tall. Note that the diameters of the beads get progressively smaller as the etch depth increases since the forward power has not been adjusted to compensate for the depth of the etch.

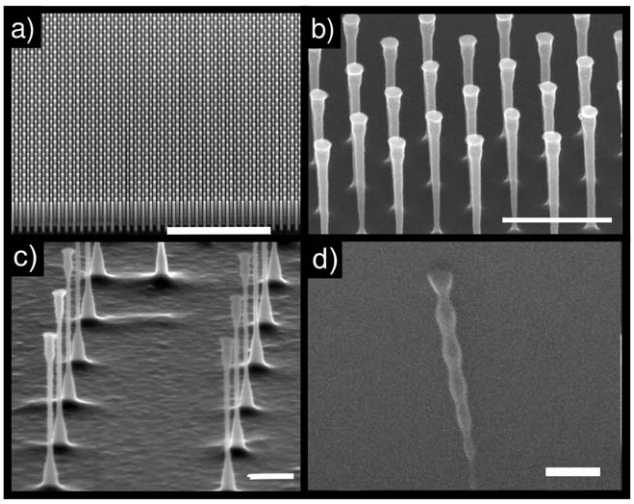
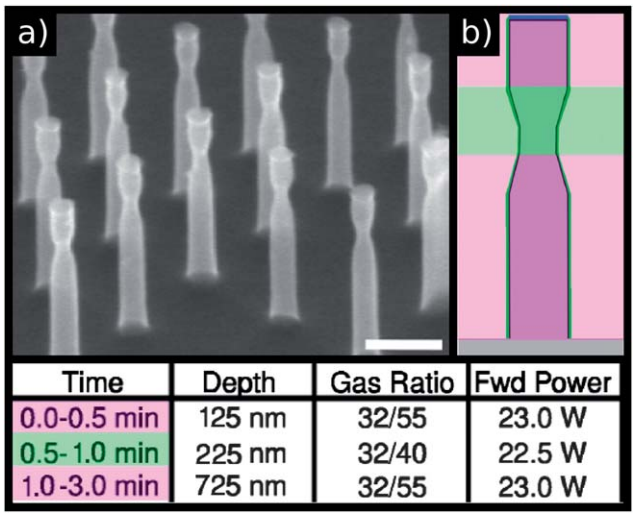


Fig. 1 SEM images of vertical silicon structures etched under different conditions. (a) An array of 50 nm diameter nanopillars etched to a depth of 1 micron. Scale bar is 2 microns. (b) An array of 100 nm diameter silicon nanopillars etched under constant under-passivation conditions. Scale bar is 500 nm. (c) An array of 15 nm diameter silicon nanopillars etched under IAD compensated etching conditions. Scale bar is 100 nm. (d) Single silicon nanopillar etched under oscillating etch conditions to produce a periodic surface morphology (pillar is lying down on the substrate). Scale bar is 100 nm.

In order to characterize the parameters of the etch to achieve precise control, a sequential investigation into etching progressively more complicated features was carried out. The following section presents the recipes that were used to develop our etching process – it is important to note that while these recipes can serve as a guide, specific parameters (flow rates, pressure, forward power, *etc.*) will have to be found for individual machines.

The simplest structure to create was a notch – shown in Fig. 2a. A three step etch procedure is carried out where the color on the schematic in Fig. 2b corresponds to the color of the step in the table. The notch is created during the second step (shown in green) where both the passivation gas flow and the forward power are reduced. The lowered forward power increases the angular distribution of the etching ions taking advantage of the thinner side-wall passivation to carve out the notch. The angled side-wall is created in the time between start



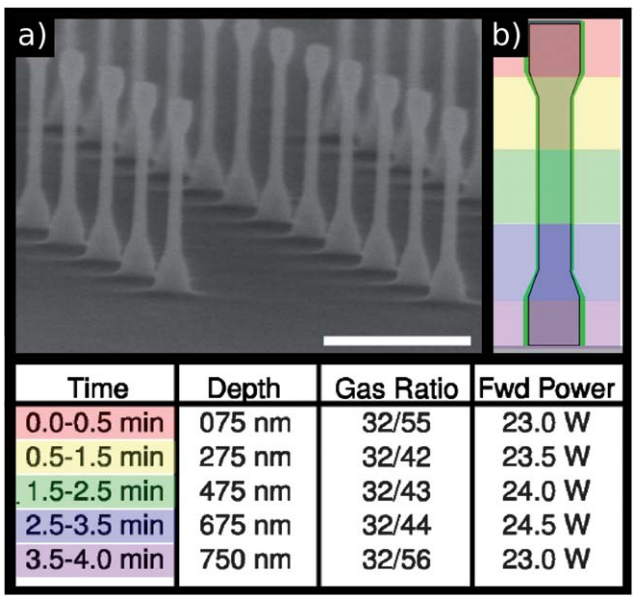
Time	Depth	Gas Ratio	Fwd Power
0.0-0.5 min	125 nm	32/55	23.0 W
0.5-1.0 min	225 nm	32/40	22.5 W
1.0-3.0 min	725 nm	32/55	23.0 W

Fig. 2 Etch recipe for a single notch in a silicon nanopillar. (a) An array of silicon pillars with a 15 nm notch in a 75 nm diameter pillar. Scale bar is 200 nm. (b) Schematic of a pillar with the various etch steps highlighted; the conditions are described in the table.

of the etch step with reduced gas flow and the time when the gas concentration stabilizes. Once the gas stabilizes, the etch continues vertically until the passivation gas flow is increased again and the etched pillar diameter begins to widen.

The next step was to characterize the narrowed, straight side-wall feature seen in Fig. 1c and 3a. Using this technique it is possible to uniformly shrink the mask dimensions and vertically etch them into the silicon substrate. In order to maintain straight side-walls both the forward power and the passivation gas flow were increased roughly every 200 nm the etch progressed into the substrate. The changes in the etch conditions are marked with colors on both the schematic in Fig. 3b and in the table. Note that the etch maintains a diameter of 35 nm over the course of 500 nm length of the stem. A recipe to fabricate a set of identically sized 'beads' similar to those seen in Fig. 1d is included in the ESI.† Combinations of these features can be used to create a variety of interesting structures, which, when combined with a self-terminating oxidation step we have previously reported,[14,15] can have features as small as 2 nm and novel band structures.

The ability to tune the bandgap of silicon based on a combination of etching and oxidation is a powerful tool. Using standard CMOS techniques in conjunction with the etch presented in this communication it would be possible to create wide bandgap (~2.0 to 2.5 eV) silicon transistors that can retain low leakage currents at higher temperatures than traditional silicon electronics. Furthermore, it is possible to leave certain features of a structure larger to ease in making electrical contact while keeping the active region sub-10 nm in dimension. Fig. 4a shows an example of a vertical nanopillar field effect transistor (VNPFET) at an intermediate fabrication step, with a 15 nm channel surrounded by 10 nm of thermal oxide and its tungsten wrap-around gate. This pillar was fabricated as described in Fig. 3. Adding an insulating spacer and a top contact completes the VNPFET. The wide head on the pillar gives an approximately 35 nm wide area of silicon to contact rather than contacting the narrow channel directly. This contacting scheme is particularly useful when interfacing with channels smaller than 5 nm. Fig. 4b shows the measured source–drain current of an array of 400 such devices in parallel as a function of wrap-around gate voltage. The ambipolar



Time	Depth	Gas Ratio	Fwd Power
0.0-0.5 min	075 nm	32/55	23.0 W
0.5-1.5 min	275 nm	32/42	23.5 W
1.5-2.5 min	475 nm	32/43	24.0 W
2.5-3.5 min	675 nm	32/44	24.5 W
3.5-4.0 min	750 nm	32/56	23.0 W

Fig. 3 Etch recipe for a 500 nm long, extended notch in a silicon nanopillar. (a) An array of silicon pillars with a 35 nm diameter stem on a 75 nm diameter pillar. Scale bar is 500 nm. (b) Schematic of a pillar with the various etch steps highlighted and the conditions are described in the table.

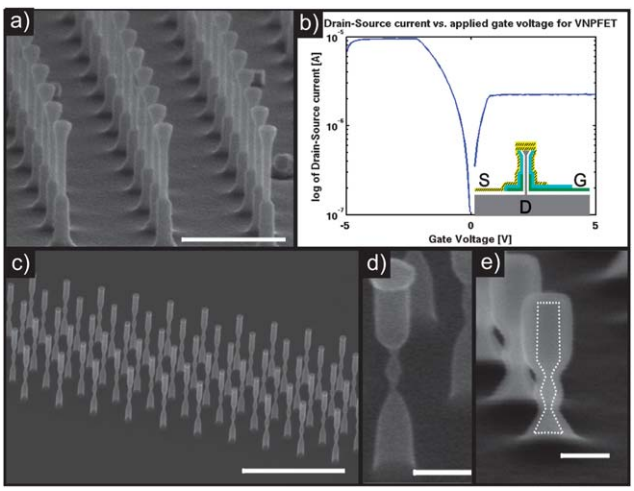


Fig. 4 VNPFET and resonant tunneling structures. (a) VNPFET at an intermediate fabrication step. The channel width of the shown structures is 15 nm and the wrap-around gate is made of tungsten. Scale bar is 500 nm. (b) Drain–source current measured as a function of applied gate voltage for the devices shown in (a). Inset shows the biasing scheme – current flows through the pillar and substrate. (c) An array of 'bow-tie' silicon structures. Scale bar is 1 micron. (d) Magnified view of a 'bow-tie' structure – the constrictions on either side of the bead are approximately 10 nm. Scale bar is 100 nm. (e) A post-oxidation SEM of a 'bow-tie' structure with the remaining silicon core highlighted. Scale bar is 50 nm.

behavior of the devices stems from the narrow channel width. As the channel width decreases, the probability of finding a dopant atom within the remaining silicon core drops until the channel can be considered, on average, to be intrinsic. Therefore the gate can serve to attract either holes or electrons depending on the polarity of the biasing. This effort shows the first attempts at making these structures and current efforts continue on examining the behavior of various material parameters (mobility, saturation velocity, *etc.*) in *single pillar* versions of these transistors as the channel width is narrowed to sub-5 nm diameters.

Such *geometric bandgap engineering* enables the creation of single material heterojunctions made from bulk silicon. This expands the standard silicon CMOS toolkit, adding devices such as heterojunction bipolar transistors (HBTs) or vertical tunneling field effect transistors (VTFETs) that used to be the domain of expensive, grown III–V semiconductors or SiGe alloys. The vertical sculpting presented here allows for the creation of such VTFETs without the use of difficult, ultra-high-resolution, lateral fabrication. Fig. 4c and d show a set of 'bow-tie' pillars fabricated using 100 nm diameter circular masks. Fig. 4e shows a bow-tie structure after oxidation; the outline highlights the remaining single crystal Si core. The two sub-10 nm constrictions locally expand the bandgap and allow a lower bandgap region to be sandwiched between them. This energy landscape can produce a resonant tunneling or single electron device where a voltage applied to a wrap-around gate can shift the band-edge energy of the sandwiched region into and out of resonance to allow tunneling between the adjacent regions. Efforts are currently underway to measure the electronic properties of these devices. There has been previous work[4] where similar structures were fabricated by lateral patterning and islands of silicon approaching 100 nm in diameter showed quantum effects at cryogenic temperatures.

Using the previously described sculpting methods, it is also possible to construct completely suspended over-hang structures without the use of sacrificial layers or SOI wafers. Creating a mask that has features with two distinct sizes allows one set of features to be undercut while the other remains as a support. An example of this is shown in Fig. 5a–c. The schematic mask has a 50 nm wide bar between two 100 nm disks. If this structure is etched vertically or with a small degree of undercut the pattern is simply transferred into silicon. Fig. 5b shows such a mask having been etched vertically for 100 nm, followed by a moderate 'notch' etch to create an undercut region 400 nm in length and once again vertically to produce a thin, electron transparent membrane. If the notch undercut is chosen to be greater than half the width of the bar, 25 nm in this case, the region below the bar is etched away. Fig. 5c shows a similar structure where the etch is initially vertical and then undercut to a larger degree to produce a suspended cross-bar. By tuning the undercut to free only portions of the masked regions it is possible to create extremely high aspect ratio structures with a single mask and dry etching step. The beam shown in Fig. 5d is 100 nm wide and 50 microns long – the image is taken from a foreshortened perspective to capture the high (500 : 1) aspect ratio of the beam. Similar to the fabrication of the beads above,

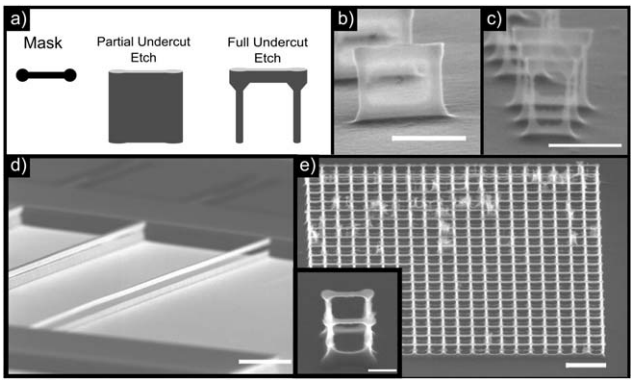


Fig. 5 Suspended structures. (a) A schematic drawing of the mask and (b) and (c) etching results. (b) Suspended beam etched with a partial undercut such that a thin electron transparent membrane remains. Scale bar is 500 nm. (c) Set of beams etched with a full undercut resulting in hoops. Scale bar is 500 nm. (d) Suspended beam 100 nm wide and 50 microns long etched and suspended with a single step. The image is taken from a foreshortened angle to fit the entire beam. Scale bar is 2 microns. (e) Three-dimensional silicon mesh created with a single etch step. Scale bar is 1 micron. Inset shows a single silicon wire-frame cube. Scale bar is 250 nm.

by utilizing the vertical uniformity of the etch it is possible to make multiple vertical iterations of (*i.e.* stacked) suspended structures for optical or structural applications. The start of a second iteration is seen below the bar in Fig. 5d. Creative mask design also allows for the fabrication of interlocking structures such as 3D silicon lattices, as shown in Fig. 5e, and interlocking hook and loop type fasteners based on the structures in Fig. 5c. Silicon lattice or nanomesh structures have found use as novel thermoelectric materials[16] and simplifying their fabrication and moving towards three-dimensional structures can decrease the cost to produce them and increase the material volume. Furthermore such structures can have a variety of applications as customizable or electronic scaffolding in the field of tissue engineering or on-chip neuron growth.

We have demonstrated and explained CMOS compatible, three-dimensional etching of silicon nanostructures to create devices with novel behavior as well as suspended structures. Utilizing the unique tools provided by an ICP etcher we can laterally sculpt silicon as an etch progresses into the substrate. This has allowed the top-down fabrication of arrays of ambipolar VNPFETs with channel widths of 15 nm while maintaining large head and foot regions for electrical contacting. The ability to sculpt silicon at the single nanometer scale in combination with thermal oxidation enables the geometric engineering of the silicon bandgap. This technique opens the door for the CMOS compatible fabrication of sub-10 nanometer scale devices without the pressure placed on lateral lithography.

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