Antimony doping of Si layers grown by solid-phase epitaxy*

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We report here that layers of Si formed by solid-phase epitaxial growth (SPEG) can be doped intentionally. The sample consists initially of an upper layer of amorphous Si (~1 μm thick), a very thin intermediate layer of Sb (nominally 5 Å), and a thin lower layer of Pd (~500 Å), all electron-gun deposited on top of a single-crystal substrate (1–10 Ω cm, *p* type, ⟨100⟩ orientation). After a heating cycle which induces epitaxial growth, electrically active Sb atoms are incorporated into the SPEG layer, as shown by the following facts: (a) the SPEG layer forms a *p-n* junction against the *p*-type substrate, (b) the Hall effect indicates strong *n*-type conduction of the layer, and (c) Auger electron spectra reveal the presence of Sb in the layer.

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It has been demonstrated that epitaxial layers of Si [1–3] and Ge [4] can be grown by solid-phase transport. In these studies, a layer of amorphous semiconductor material was deposited on a metal film covering a single-crystal semiconductor substrate. In the case of Ge where the transport metal is Al, the grown layer is found to be electrically doped due to the incorporation of Al atoms during the transport of the amorphous Ge layer.[4] In the case of Si,[3] the epitaxial layer is obtained by transporting the amorphous Si through a palladium silicide layer. It is the objective of this letter to report that epitaxial Si layers obtained by solid-phase epitaxial growth (SPEG) can be electrically doped by the addition of a doping layer (Sb in this work) to the thin-film structure prior to heat treatment.

In this investigation, commercially polished ⟨100⟩ *p*-type Si substrates of resistivity between 1 and 10 Ω cm were used. A layer of Pd ranging between 500 to 1000 Å in thickness was evaporated onto the Si substrates, followed by a deposition of nominally 5 Å of Sb and about 1 μm of amorphous Si. All evaporations were carried out at a pressure of $\sim 1\times10^{-6}$ Torr. The samples were then annealed in a vacuum furnace at a pressure of 2×10^{-6} Torr. During the heating cycle the samples were first annealed at 280 °C for 20 min to form Pd_2Si; then, without breaking vacuum, the temperature was increased to between 480 and 550 °C at a rate of 0.2–5 °C/min. Transport of the amorphous Si through the Pd_2Si layer and the incorporation of Sb atoms in the epitaxially grown layer took place during the higher-temperature annealing step. The details of sample preparation and heat treatment have been previously reported.[2]

Elemental distribution profiles in depth were studied by Auger electron spectrometry (AES) and MeV $^4He^+$ backscattering spectrometry (BS). Figure 1 shows AES depth profiles for Si, Pd, and Sb observed from a sample after Pd_2Si formation (a), and after the final growth stage (b). The original Pd, Sb, and Si thicknesses for this sample as measured by BS were 970, ~5, and 9700 Å, respectively.[5] As Fig. 1(a) shows, the Sb is essentially localized at the interface between the amorphous Si and Pd_2Si after heat treatment at 280 °C. However, after the higher-temperature anneal, two major changes are seen to occur [Fig. 1(b)]: the amorphous Si has been transported through the Pd_2Si layer to the substrate and the Sb atoms are incorporated into the grown layer during the transport process. Using sputtering rates estimated from BS film thickness measurements, the width of the Sb distribution is calculated to be about 2000 Å in the grown layer. Some of this observed width in the Sb signal may result from a deterioration of depth resolution at this depth. The amount of Pd trapped in the grown layer was determined by electron microprobe and AES to be about 1 at.%. In the AES measurements quantitation was performed by ratioing the Sb

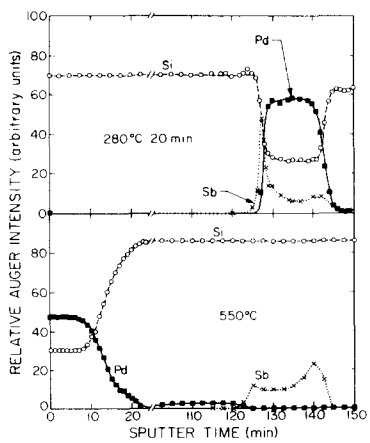

FIG. 1. Depth profiles of Si, Pd, and Sb obtained by Auger electron spectroscopy for a sample consisting originally of a top layer of amorphous Si (~1 μm), a very thin intermediate layer of Sb (~5 Å), and a bottom layer of Pd (~500 Å) on a single-crystal substrate in ⟨100⟩ orientation, (a) after Pd_2Si formation by annealing at 280 °C for 20 min, (b) after solid-phase epitaxial growth of the amorphous Si upon annealing to 550 °C. The vertical sensitivity is different for each element and each figure.

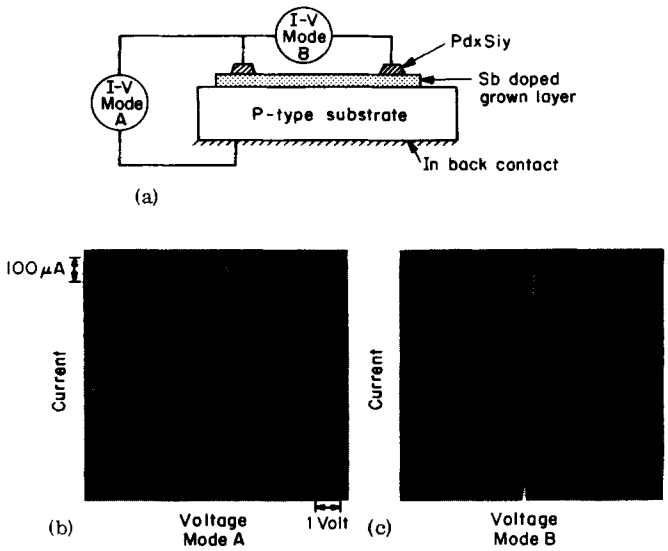

FIG. 2. *I-V* characteristics showing a rectifying junction between the SPEG layer and the substrate (mode A) and the Ohmic behavior of the SPEG layer itself (mode B).

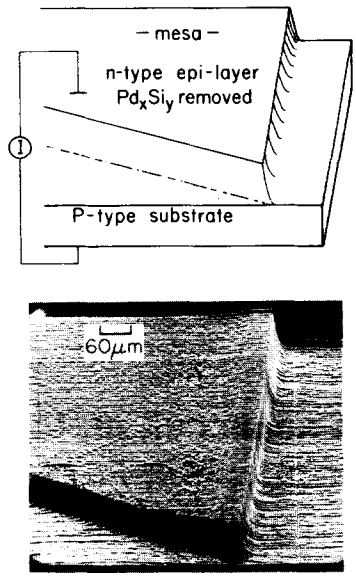

FIG. 3. Scanning electron micrograph obtained in the electron-beam-induced current mode of a mesa-etched SPEG layer. The Pd silicide layer was chemically removed before mesa etching. The SEM scan is taken with the electron-beam-induced current generating the *y* deflection.

signal to the matrix signal after each had been normalized to the pure element spectrum.[6]

We have investigated the electrical characteristics of silicon SPEG layers with incorporated Sb atoms by *I-V* and Hall-effect measurements, and with a scanning electron microscope operated in the electron-beam-induced current (EBIC) mode. The electrical conductivity and the *I-V* characteristics of the SPEG layer against the *p*-type substrate are shown in Fig. 2. The schematic on top of Fig. 2 shows a cross section of a mesa structure for Hall-effect measurements employing the van der Pauw configuration. Rectifying behavior was observed between the top Pd silicide (Pd_xSi_y) contact and the indium back contact on the *p*-type substrate (mode A), while Ohmic behavior and low resistance were observed between two palladium silicide contacts on the top of the epitaxial layer (mode B). These *I-V* characteristics clearly show that the SPEG layer has good electrical conductivity and has rectifying behavior against the *p*-type substrate. Hall voltage polarity shows that the grown layer has *n*-type conductivity. Hall-effect measurements at room temperature give a sheet resistivity of approximately 100 Ω/□, an electron Hall mobility of approximately 50 cm^2/Vs, and a surface concentration N_s of electrons of approximately $1\times10^{15}/cm^2$. The Hall mobility observed in the grown layer is in general agreement with results reported for heavily doped *n*-type materials.[7]

For one sample, a direct comparison of the amount of Sb (number of atoms/cm^2) measured by backscattering spectrometry and the electron surface concentration (number of atoms/cm^2) measured by the Hall effect was made. The surface concentration of Sb obtained by BS is $2.4\times10^{15}/cm^2$ and represents the total amount of evaporated Sb atoms before transport. The Sb surface concentration deduced from the Hall effect is $1.3\times10^{15}/cm^2$. This value is less than that obtained by BS, but the measurement is sensitive only to the electrically active Sb atoms in the grown layer.

Carrier concentration profiling of SPEG layers by Hall measurements combined with anodic stripping has also been attempted.[8] The preliminary results show a region of electrical conductivity in the SPEG layer in close proximity to the substrate [as anticipated from the Auger profile in Fig. 1(b)]. In this region, the concentration of electrically active Sb atoms is of the order of $10^{19}/cm^3$.

The lateral uniformity of the *p-n* junction between the SPEG layer and the underlying *p*-type substrate was examined with a scanning electron microscope operated in the EBIC mode (see Fig. 3). The presence of a laterally continuous junction is indicated by the uniform collection of induced current in the space-charge region between the *n*-type grown layer and the *p*-type substrate across the area shown (0.5×0.5 mm).

The combined results of four different types of measurements (*I-V*, Hall effect, AES, and EBIC SEM) show that the epitaxially grown layer is doped with electrically active Sb atoms, and forms a rectifying junction against a *p*-type substrate. The junction appears continuous across dimensions limited only by the size of the samples.

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High-performance solar cell material: *n*-AlAs/*p*-GaAs prepared by vapor phase epitaxy

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Solar cells with measured sea level sunlight power conversion efficiencies of 13–18% and areas of several cm^2 have been prepared by vapor phase epitaxial growth of *n*-AlAs on *p*-GaAs substrates. The cells are provided with an antireflective passivating anodically grown coating and have much improved stability in the laboratory atmosphere.

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The well-known close lattice-constant match between AlAs and GaAs permits fabrication of a variety of interesting and potentially very important heterostructure devices. To date, notable successes which have been achieved are the cw room-temperature semiconductor laser[1] and high-efficiency GaAs *p-n* solar cells with *p*-type $Ga_xAl_{1-x}As$[2,3] or AlAs[4] windows, all of which were prepared by liquid phase epitaxy (LPE). We report here successful fabrication of large-area solar cell devices by vapor phase epitaxial (VPE) growth of *n*-AlAs on *p*-GaAs. The Al-Ga interface in our devices appears to be abrupt (see below), in contrast to what is to be expected in LPE growth. We have also verified (using optical and electron microscopy, and thermal surface probe testing of selectively etched samples) that the *p-n* junction is coincident with the metallurgical interface. While our measured sea level solar conversion efficiencies (13–18%) are not so good as the best (18–21%) reported to date for the LPE GaAs-$Ga_xAl_{1-x}As$ devices,[2,3] it is important that our cells are significantly larger in area and that our ability to grow larger devices is limited by purely mechanical considerations and substrate size. We have measured (for air mass 1.4, bright sunlight) open-circuit voltages up to 0.92 V and short-circuit current densities of 30 mA cm^{-2} per 100 mW cm^{-2} insulation. Our "best" junction (V_{oc} = 0.92 V) was 2.7 cm^2 in area. These values are equal to those reported in Ref. 3. Our lower measured power efficiency is due to the simple stripe contact and concomitant series resistance of our devices.

The *n*-AlAs epitaxial layers were grown, on (100) GaAs:Zn substrates, from 6N Al and electronic-grade AsH_3 by an HCl transport process similar to that described by Ettenberg *et al.*[5] Similar substrate preparation was also employed. An important difference in our technique is the complete elimination of silica components in the hot region of the growth reactor. With the exception of a small quantity of W sheet and wire used to hold the substrate, all components of our growth reactor are made from high-purity (99.8%) Al_2O_3 ceramic. This material remains unaffected after hundreds of hours exposure to the highly reactive AlCl atmosphere. In contrast to the observations of Sigai *et al.*[6] we find no evidence for an insulating or type-converted layer at the GaAs-AlAs interface, for growth either on the Zn-doped ($p \sim 2\times10^{18}$) device substrates or on Cr-doped ($\rho > 10^8$ Ω cm) GaAs substrates. This we attribute to elimination of Si contamination, which is borne out by analysis of a large quantity of "bulk" AlAs taken from the immediate vicinity of the growth region. That analysis showed a faint trace (<0.2 ppm) of Si and no observed Cu, Mg, or Fe. The alumina components also permit higher operating temperatures than those explored in Refs. 4 and 5. The devices described here use layers grown at ~1000 °C and flow rates of ~500 cm^3/min of 2% HCl/H_2 and 2% AsH_3/H_2, which appear

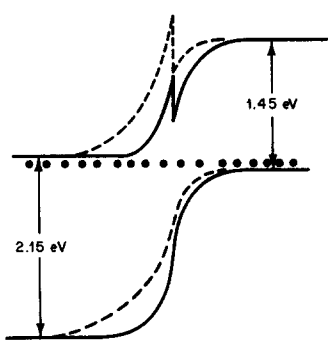

FIG. 1. Schematic band diagram for *n*-AlAs/*p*-GaAs heterojunction. Solid line, equal carrier concentrations; broken line, *n*-side carrier concentration ~1/3 that on *p* side.