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Coulomb blockade in vertical, bandgap engineered silicon nanopillars

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Vertically oriented, bandgap engineered silicon double tunnel junction nanopillars were fabricated and electrically addressed. The devices were tested at liquid nitrogen and room temperatures. Distinctive staircase steps in current were observed at cryogenic temperatures indicative of the Coulomb blockade effect present in asymmetric double tunnel junction structures. These features disappeared when the device was measured at room temperature. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4799059]

Silicon nanowires (SiNWs) have attracted considerable attention as platforms for nanoscale physics experiments over the past twenty years.[1] Recent work has used nanowires as cell probes,[2] ion sensors,[3] as thermoelectric,[4] and as basic electronic components such as SiNWFETs.[5]

The fabrication of SiNWs has progressed along two distinct paths: "Top-Down" and "Bottom-Up." The bottom-up approach concentrates on growing wires using the vapor-liquid-solid technique.[5] This method is performed in a high-temperature reactor filled with a silicon containing gas such as SiH_4 or $SiCl_4$. A metal nanoparticle is used to dissolve and concentrate the silicon, which then precipitates out as a growing single crystal. Unfortunately, the thermodynamics of this growth require that either [111] or [110] substrates be used to form vertical SiNW. Furthermore, difficulty in specifying nanoparticle size and position has led to most groups relying on stochastic growth techniques. Typically nanowires are grown, cleaved off and suspended in a solvent, spun onto a receptive substrate, and then an SEM is required to find appropriate targets for electrical contacting. Although this technique has been used with great success to create innovative devices, it is unfortunately limited to the laboratory as it would be difficult to insert into the current CMOS fabrication paradigm.

In response to these challenges, several groups have begun fabricating top-down planar or vertical SiNW devices via electron beam patterning and etching processes.[6–8] For clarity, we will refer to etched, vertical, structures as silicon nanopillars (SiNPs) to distinguish them from their nanowire and planar counterparts. The use of established fabrication methods allows for the integration of SiNPs into standard CMOS fabrication lines and the vertical orientation leads to easy electrical and optical access.

In this study, we adopt the sculpted vertical nanopillar geometry we demonstrated previously in Walavalkar *et al.*[9] We have also shown in previous work that constraining silicon to sub-10 nm dimensions forces the silicon bandgap to widen due to both band-structure folding and oxidative strain.[10,11] By modulating the radial dimension of the nanopillar during the vertical progression of the etch, we can create sandwiched regions of high and low bandgap energy—in effect creating heterostructures out of silicon alone. This *geometric bandgap engineering* allows us to create custom energy landscapes. In this paper, we use this method to fabricate a double tunnel junction device and to demonstrate quantum conductivity oscillations.

The device fabrication utilized etching techniques explained in detail in previous work.[9] Briefly, a single disk of aluminum oxide was defined using electron beam lithography. This disk served as the mask for a sculpted SiNP etch,[9] producing the structure seen in Figure 1(a). The device was then oxidized using a self-terminating oxidation method,[10–12] leaving a silicon core with a severely constrained geometry, shown in TEM in Figure 1(b). It is important to note that the two sub-10 nm constrictions seen in Figure 1(b) feature expanded bandgaps, while the wider region between the two maintains the lower, bulk silicon bandgap. A schematic of the resultant energy diagram is shown in Figure 1(c). Polymethyl-methacrylate (PMMA) was spun on in order to mask the pillar side-wall, and hydrofluoric acid was used to "decapitate" the pillar, exposing the inner silicon core. Aligned lithography was used to contact the exposed silicon and a second contact was placed on the backside of the chip. A schematic of the fabricated device is shown in Figure 1(d) and an SEM of the resulting metal coated structure is shown in panel 1(e). To create reliable ohmic contacts, the chip was placed in a rapid thermal annealer and heated to 400 °C in a forming gas environment ($5\%H_2/95\%N_2$) for 1 min. Finally, the chip was wirebonded and placed into a vacuum cryostat for testing at both liquid nitrogen and room temperature.

Measurements were carried out with a computer controlled voltage supply and pico-ammeter. Each data point was polled several times and the mean value and variance of the measured current was kept. Figure 2 shows the current-voltage measured for the pillar in Figure 1(a) at both room and cryogenic temperatures. The data at cryogenic temperatures are markedly different than that at room temperature. The low-temperature data are both an order of magnitude smaller and features clear staircase-type behavior indicative of a Coulomb blockade effect. The differential conductance of the cooled sample, shown in Figure 3 and computed from I-V measurements, displays multiple periodic peaks indicating regular jumps in conductance. At room temperature, however, these features disappear and the device shows the exponential current/voltage behavior of a single tunnel junction.

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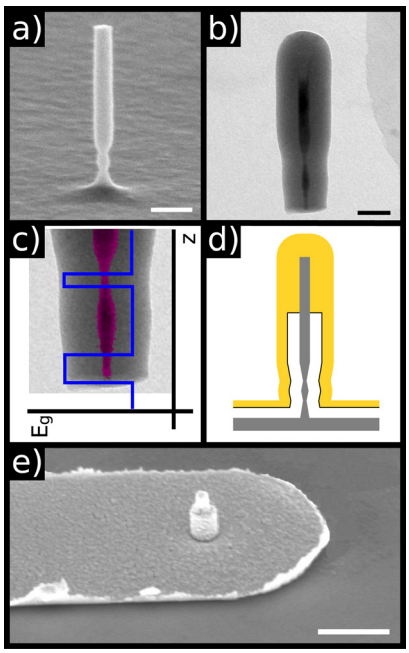

FIG. 1. Fabrication and schematic of double tunnel junction device. (a) SEM of as-etched, sculpted, silicon nanopillar. Scale bar is 100 nm. (b) TEM of oxidized double tunnel junction pillar after removal from the substrate. Scale bar is 50 nm. (c) Schematic placed over the TEM image showing regions of widened silicon bandgap after oxidation. (d) Schematic of the completed device. (e) SEM of the completed device. Scale bar is 500 nm.

The measured behavior of the device at cryogenic temperatures is demonstrative of an asymmetric double tunnel junction.[13] In this case, the capacitance, or "transparency," of one of the junctions is significantly smaller than the other, schematically shown in Figure 4(a). If the junctions were symmetric (each with a capacitance of C_j), no current would flow until forward bias reaches a voltage great enough to transfer an electron into and out of the isolated island ($V_t \sim \frac{e}{2C_j}$). Above this point, the device would function as a diode or resistor with a forward bias of $V_f = V_{applied} - \frac{e}{2C_j}$. A current voltage plot would show a turn on and the differential conductance would have a single step, both at V_t.

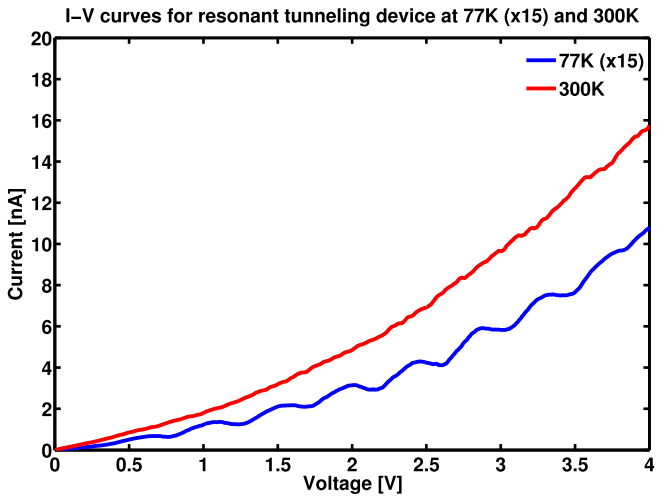

FIG. 2. Measured I-V plot of a double tunnel junction device at 300 K and 77 K. Note that the 77 K data is scaled by a factor of 15. Clear steps can be seen in the low-temperature measurement.

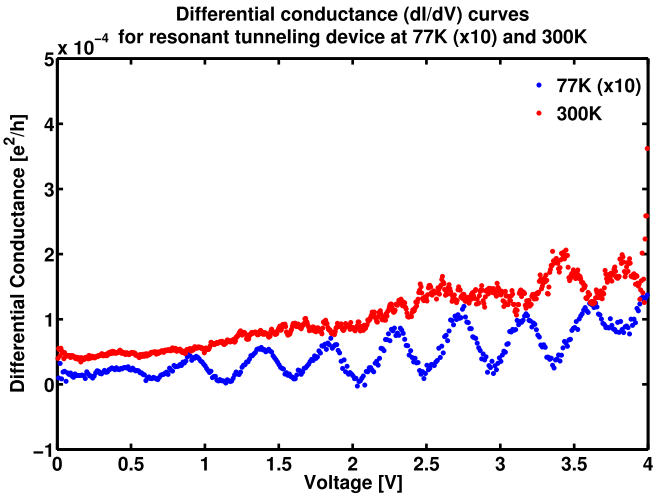

FIG. 3. Differential conductance of a double tunnel junction device at 300 K and 77 K. Plot was numerically computed from measured I-V data. Note that the 77 K data are scaled by a factor of 10. Periodic peaks can be seen with a spacing of 0.452 V.

In our case, for a small forward bias, the first tunnel barrier is easily surpassed and the island is populated with an integer number of charges (Figure 4(a)). The low transparency of the second barrier keeps the electrons trapped, and the electrostatic repulsion between electrons prevents the island from accumulating more charge. The tunneling coefficient of the opaque barrier, which determines the current allowed through the device, is a function of both the forward bias and the number of charges on the island. The approximate functional dependence can be written as $I_{tunneling} \sim I_o(V_a, n) \times \exp(\frac{\alpha V_a}{k_B T})$, where α contains the geometry of the barrier. As

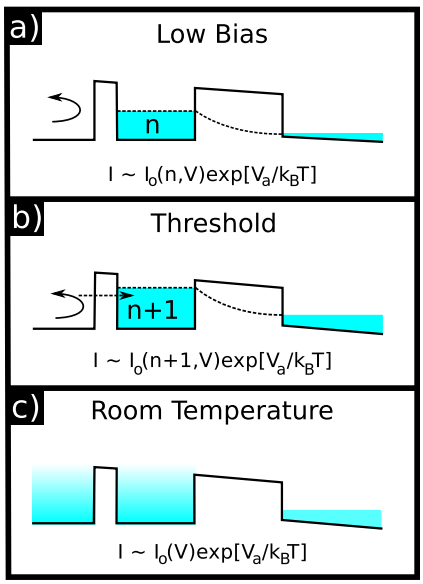

FIG. 4. Schematic illustrating the behavior of asymmetric double tunnel junction diode under different bias and temperature conditions. (a) At low bias, the island is populated and charged to saturation. Little charge can tunnel across the opaque barrier. (b) At a higher forward bias, extra electrons can be forced into the island against the electrostatic repulsion of existing charges. The increased number of electrons allows for a greater amount of current to flow through the opaque barrier. (c) At room temperature, the thermal fluctuations remove the island from isolation effectively creating a single tunnel junction device.

the applied voltage is increased, the tunneling rate through the opaque barrier increases but the fixed number of electrons allowed on the island forces the current to remain constant. When the forward bias reaches a large enough value, the electrostatic repulsion can be overcome and an additional electron is forced onto the island (Figure 4(b)). While the new charge increases the electrostatic repulsion of the island, it is equally negated by the applied voltage; so the voltage increase required to add subsequent electrons remains constant.

The increase in occupation number on the island causes a jump in the current as more charges are available to tunnel across the opaque barrier. This can be quantified as an increase in the I_o term in the tunneling current equation. These discrete jumps in current result in the staircase shaped behavior seen in Figure 2 and the periodically peaked differential conductance seen in Figure 3. From the spacing of the conductance peaks in Figure 3, we can extract the voltage required to add a single charge to the device and estimate the quantum capacitance. Taking the average spacing to be 0.452 V, the capacitance of the device is 0.356 aF.

When the device was measured at room temperature, the lack of distinct current steps can be attributed to the addition of thermal noise. The effect of thermal broadening on the distribution of electron energy is to provide a background charge density on the island great enough to effectively remove it from isolation by shorting the more transparent tunnel junction.[13] The resultant structure behaves as a single rectangular tunnel barrier (schematically shown in Figure 4(c)), displaying the characteristic exponential behavior where $I \sim \exp(\frac{\alpha V_{fwd}}{kT})$ in which the α prefactor contains the relevant geometry of the barrier. At small voltages ($V_{fwd} < 1V$), some small peaks in conductance can be seen (the red plot in Figure 3), but this behavior seems to be rapidly swamped by the noise introduced at higher voltages. Careful measurements made with greater precision will be done in the future to quantify the possible presence of Coulomb blockade effects at room temperature. The oscillations present in the differential conductance at larger voltages are likely a result of high-energy injection effects and not from a blockading effect.

It is important to note that the "semi-classical" treatment of this device does not include secondary effects such as the charge dependent modification of the bandstructure or strain effects. We can see hints of the influence of one of these phenomena as the small decrease in current present after each "step" in the I-V plot in Figure 2. (This corresponds to a negative differential conductance in Figure 3.) The origin of the dip in current is believed to come from the build-up of electrons at the interface of the opaque junction. This collection of charges opposes the tunneling of electrons, dropping the magnitude of the current. Careful study of this behavior is required to quantify this effect and can be done by either cooling the sample to liquid helium temperatures or creating a device with a greater asymmetry in junction transparency. Future studies will also explore methods to quench the collection of fractional charge on the island. This charge can be measured by examining the I-V curve for asymmetries across zero applied voltage.[14] It is hoped that the elimination of this excess charge will help to push the Coulomb blockade behavior to higher temperatures.

This letter reports the fabrication and testing of a unique silicon quantum device. Etching dependent geometric modification of the silicon bandstructure was used to create an asymmetric, double tunnel junction, energy landscape. Measurements taken at liquid nitrogen temperature show clear Coulomb blockade effects and quantum conductance oscillations. Further research will focus on gating such structures and creating sharper deviations in the etch profile with the aim of bringing the Coulomb blockade behavior into the room temperature regime and creating single electron transistors.

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