

# The Class-E/F Family of ZVS Switching Amplifiers

Scott D. Kee, Ichiro Aoki, *Member, IEEE*, Ali Hajimiri, *Member, IEEE*, and David Rutledge, *Fellow, IEEE*

**Abstract**—A new family of switching amplifiers, each member having some of the features of both class E and inverse F, is introduced. These class-E/F amplifiers have class-E features such as incorporation of the transistor parasitic capacitance into the circuit, exact truly switching time-domain solutions, and allowance for zero-voltage-switching operation. Additionally, some number of harmonics may be tuned in the fashion of inverse class F in order to achieve more desirable voltage and current waveforms for improved performance. Operational waveforms for several implementations are presented, and efficiency estimates are compared to class-E.

**Index Terms**—Class E, class E/F, class F, harmonic tuning, high-efficiency amplifier, switching power amplifier, zero voltage switching (ZVS).

## I. INTRODUCTION

FOR power-amplifier and power-inverter applications, harmonic-tuned switching amplifiers such as class E [1], [2] and class F [3] offer high efficiencies at high power densities. By operating the active device as a switch rather than a controlled current source, the voltage and current waveforms can, in principle, be made to have no overlap, reducing the theoretically achievable device dissipation to zero. At the same time, unlike in class-C operation, the output power of switching modes can be comparable to or greater than that of class A or class B for the same device peak voltage and current. For applications wherein AM/AM and AM/PM distortion can be tolerated [4], or compensated for [5], such amplifiers can improve efficiency and reduce heat-sink requirements. High-speed power converters, such as dc-dc converters, similarly benefit from improved RF power-amplifier efficiency [6].

Unfortunately, only two types of amplifier tunings appropriate for high-frequency operation, i.e., class E and class F, have been explored. Class-E amplifiers have found most application as a higher performance alternative to class-D amplifiers due to their compensation for transistor output capacitance and elimination of turn-on switching losses. Additionally, the class-E design may be implemented with a relatively simple circuit. These benefits have allowed class-E designs to push far beyond the frequencies achievable by class-D designs, with recent results reporting 55% at 1.8 GHz using CMOS devices [7] and

74% at 800 MHz using GaAs HBT devices [8]. Recently, current-mode class D (or class  $D^{-1}$ ) [6] has also been implemented as a high-frequency amplifier [9], although it has not been clear how this topology can be modified for large transistor output capacitance.

Class F and its recently popularized dual inverse class F (class  $F^{-1}$ ) [10]–[12] have been developed primarily as a means of increasing saturated performance of class-AB and class-B designs. As a result, the attainable operating frequencies are somewhat higher, e.g., [5], [13] than those for class-E circuits, but the performance limitations due to the tuning requirements [14], [15] and the lack of a simple circuit implementation, e.g., [16], suitable for nearly ideal switching, make class F a poor alternative at frequencies where a lumped-element class E can be implemented.

Nonetheless, there is reason to believe the waveforms achievable in principle by class F and/or  $F^{-1}$  should allow benefits over class E. Although Raab has shown that the efficiencies of properly tuned class E and class F are identical when the efficiency is limited primarily by the harmonic content of the waveforms [17], the case wherein the transistor is switching nearly ideally and the efficiency is limited primarily by the device's on-resistance would seem to favor class F and  $F^{-1}$  with their reduced peak voltages and, in the case of class  $F^{-1}$ , rms current. As will be shown in Section III, these differences in the waveforms should provide advantages in efficiency and saturated gain. Additionally, the class-E approach has limited tolerance for large transistor output capacitance [18], providing an identifiable limit to its high-frequency performance.

This paper presents a new family of harmonic tunings with the promise to achieve the performance benefits of class F by reducing the peak voltage and rms current of class-E designs. Additionally, this tuning method allows increased tolerance to large transistor output capacitance, improving the high-frequency performance and extending the frequency range of this new tuning beyond that of class E. This new E/F family of tunings unifies class E and class  $F^{-1}$  into a single framework, and demonstrates varying degrees of tradeoff between the simplicity of class E and the high performance of class  $F^{-1}$ . All members of the E/F family have exact time-domain solutions, can be made to achieve class-E switching conditions, and have implementations that absorb the switch output capacitance.

This technique has been used to implement several amplifiers at high and microwave frequencies. The  $E/F_{2, \text{odd}}$  tuning has been used in the construction of a compact high-efficiency power amplifier producing in excess of 1 kW at 7 MHz [19]. A similar design modified to achieve the  $E/F_{\text{odd}}$  tuning in the 7- and 10-MHz bands achieves over 200 W of output power in each of these bands with drain efficiencies higher than 90% [20]. Another fully integrated CMOS amplifier uses the  $E/F_3$

Manuscript received June 13, 2002. This work was supported by the Jet Propulsion Laboratory, by the Lee Center for Advanced Networking, by the National Science Foundation, by the Army Research Office, and by the Xerox Corporation.

S. D. Kee was with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125-4806 USA. He is now with Axiom Microdevices Inc., Orange, CA 92868 USA.

I. Aoki is with Axiom Microdevices Inc., Orange, CA 92868 USA.

A. Hajimiri and D. Rutledge are with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125-4806 USA.

Digital Object Identifier 10.1109/TMTT.2003.812564

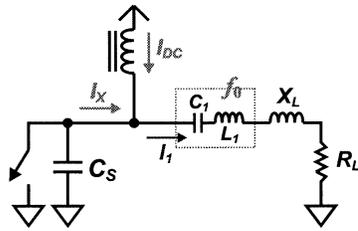


Fig. 1. Class-E amplifier topology.

mode to produce 2.2 W of output power at 2.4 GHz [21]. This result uses the distributed active transformer on-chip matching and power-combining structure [22], [23], which is not compatible with either the class-E or class-F tunings. In this case, the E/F technique enables the use of a saturated amplifier mode in the DAT power-combining structure.

## II. CLASS E AND CLASS F

This section reviews class-E and class-F, comparing their relative advantages and disadvantages. Finally, a “wish list” is presented of properties desirable in any new tuning.

### A. Class E

The class-E tuning approach, depicted in Fig. 1, has been developed [1], [2], [24] mainly as a time-domain technique, with the active device treated as a nearly ideal switch. Specifically, the switch is assumed to be effectively open circuit during the “off” duration and a perfect short-circuit during the “on” duration, and that the time required to switch between states is effectively zero. These conditions will be denoted as *strong switching*.

Under strong switching, a common problem is efficiency degradation due to discharge of the switching device’s output capacitance. If the voltage across the switch prior to a transition from the “off” state to the “on” state is nonzero, the energy stored in this capacitance is dissipated by a discharge current through the switch. Since this occurs once per cycle, this loss increases linearly with the operating frequency and can be considerable even at relatively low frequencies. As a result, much effort has been devoted to finding means of eliminating this loss mechanism, e.g., [2], [6], [25]. The class-E approach is one such method, wherein the switch voltage is driven to zero prior to turn-on by an appropriately tuned resonant circuit. This technique is known as zero voltage switching (ZVS).

Using the circuit of Fig. 1, the switch is made to conduct with 50% duty cycle at frequency  $f_0$ , and its parasitic output capacitance is absorbed into the switch parallel capacitance  $C_S$ . The resonator consisting of  $L_1$  and  $C_1$  is used to block the harmonic frequencies and dc, forcing the current  $I_1$  to be a sinusoid with frequency  $f_0$ . The choke is assumed to be ideal so that it only conducts the dc current  $I_{DC}$ . The current into the switch/capacitor combination  $I_X$  must then be a dc offset sinusoid.

This current is commutated between the capacitor and switch. When the switch is closed, the voltage is forced to zero, fixing the capacitor’s charge, thus forcing the current through the switch. When the switch is open, the capacitor must conduct the current. By appropriately adjusting the amplitude and phase

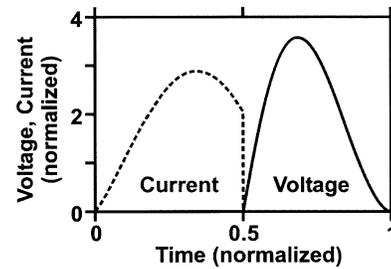


Fig. 2. Class-E amplifier dc normalized waveforms.

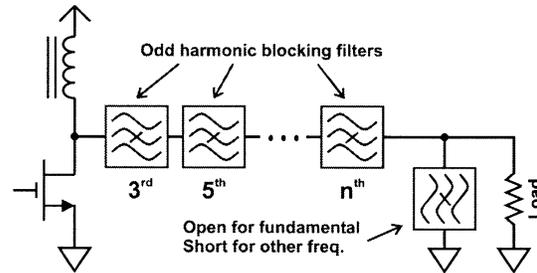


Fig. 3. Example class-F amplifier topology.

of the sinusoidal component of the current, a solution is found with zero capacitor charge just prior to turn on. This leaves an additional degree of freedom, which is typically used to set the capacitor *current* to zero at turn on. This results in a switching waveform with zero voltage (no capacitor charge) and zero voltage slope (no capacitor current) at turn on, conditions now known as the *class-E switching conditions*. The resulting voltage and current waveforms are depicted in Fig. 2.

### B. Class F and Class F<sup>-1</sup>

The class-F approach has been developed [3], [14] in the frequency domain as a means of increasing the efficiency of class-A/B and class-B amplifiers. Rather than using the strong-switching assumption, it is assumed that the amplifier is only partially compressed so that a relatively small number of harmonics have been generated at the drain. Although the transistor is acting as a switch for some parts of the cycle, it is spending considerable time transitioning between switching states, where this time is limited by the harmonic composition of the drain waveforms. The class-F approach seeks to determine how best to utilize these few harmonics to improve efficiency.

A class-F amplifier implementation is depicted in Fig. 3. Starting with a standard class-B amplifier, wherein a parallel resonant filter is used to force the load voltage to be sinusoidal, additional resonators are added in series with the load/resonator combination to open-circuit the transistor drain at several low-order odd harmonics. As a result, the compressed voltage waveform will begin to increasingly resemble a square wave as the generated odd voltage harmonics will tend to flatten the top and bottom of the waveform, as can be seen in Fig. 4. This flattening decreases the voltage across the transistor during the time it is conducting, thus increasing the efficiency. The more harmonics open circuited, the greater the flattening and the higher the resulting efficiency can be. The limiting all-harmonics-tuned case is the class-D square-wave.

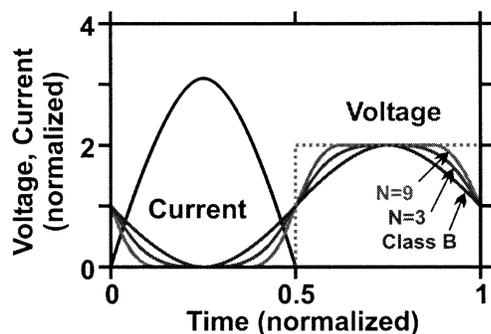


Fig. 4. Class-F maximally flat dc normalized waveforms for various numbers of harmonics tuned and class-B drive conditions.

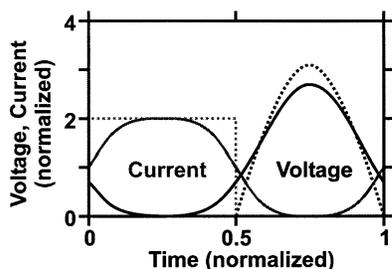


Fig. 5. Class- $F^{-1}$  maximally flat dc normalized waveforms for tuning up to the third harmonic. Broken-line waveforms are the limiting all-harmonics-tuned case.

The efficiency increase beyond the theoretical class-B limit of 78% is substantial for low-order harmonics, but diminishes with increasing harmonic number. For instance, if the harmonics appear in a manner so as to make the voltage waveform maximally flat around the voltage minimum [14], the maximum efficiencies for tuning up to the third, fifth, and seventh harmonics are 88%, 92%, and 94%, respectively. In the limiting all-harmonics-tuned case, the voltage becomes a square wave and the achievable efficiency is 100%. These maxima are set by the tuning and the true efficiency is further reduced by other factors such as on-resistance, switching speed, passive losses, etc.

Class  $F^{-1}$  is the dual tuning of class F. Where class-F short circuits even harmonics and open circuits odd harmonics, class- $F^{-1}$  open circuits even harmonics and short circuits odd harmonics. This has the effect of interchanging the voltage and current waveforms so that, as the number of tuned harmonics increases, the voltage waveform increasingly resembles a half-sinusoid and the current waveform increasingly resembles a square wave. Several recent studies suggest that class  $F^{-1}$  compares favorably to class F [10], [11], although the efficiency limits imposed by the waveforms are the same [17]. Example waveforms for a class- $F^{-1}$  amplifier are shown in Fig. 5.

### C. Comparison and Motivation for E/F

Comparing class E to the two class-F tunings, several advantages and disadvantages are apparent. Class E has the advantage of being capable of strong switching operation even with a very simple circuit, whereas class F allows this only as a limiting case using a circuit with great complexity. From Fig. 4, it is easily seen that even with tuning up to the ninth harmonic, the voltage and current waveform exhibit significant overlap.

Whereas the class-E amplifier is limited only by the intrinsic switching speed of the active device, class-F amplifier tunings may find their switching speed dominated by the limited number of harmonics, which have been utilized in the waveforms.

Additionally, class E has the advantage of incorporating the output capacitance of the transistor into the circuit topology. The simple class-F implementation shown in Fig. 3 will not work in the presence of large output capacitance since the harmonics that were intended to be open circuited at the transistor will instead be capacitive. Although a tuning network can be implemented to resonate with this capacitance to produce open circuits at each required frequency, this technique can add design complexity and tuning difficulty. The class-E tuning not only absorbs the capacitance into the basic network, but also allows ZVS operation, eliminating discharge losses from this capacitor. The tuning of class-E circuits is also very simple, requiring only one parameter to be adjusted to achieve high-efficiency ZVS operation.

Classes F and  $F^{-1}$  also have advantages. First, they present more desirable waveforms. As explained in the following section, it is desirable to have waveforms with low peak voltage and rms current.<sup>1</sup> Examining the waveforms of Figs. 2, 4, and 5, it is clear that class-F and  $F^{-1}$  amplifiers can perform better in these respects.

Additionally, the allowable output capacitance in the class-E case is limited. The switch parallel capacitance  $C_S$ , which must be at least as large as the transistor output capacitance, is determined by the output power, dc voltage, and operating frequency. This restriction on the size of the transistor can limit the performance of class-E amplifiers [18]. Class-F tunings, however, can, in principle, utilize a transistor with any output capacitance provided that it is properly resonated out at the appropriate frequencies. Although this approach might be used to resonate part of the output capacitance of a class-E tuned transistor at each harmonic, the resulting circuit complexity would be at least that of class F. Since class-F tunings present better waveforms, it would seem to be a poor approach. It would be better, if possible, to find a tuning strategy that increases the capacitance tolerance without adding such complexity.

These issues motivate the search for more desirable strong-switching amplifier tunings, which would, ideally, have some of the best features of both the class-E and class-F tunings. If such a harmonic tuning strategy is to be found, it would ideally have the following features:

- incorporation of the transistor output capacitance into the tuned circuit, where this capacitance may be as large as possible;
- ZVS to eliminate discharge loss from this capacitor;
- simple circuit implementation;
- use of harmonic tuning to achieve improved waveforms for better performance.

### III. WAVEFORM EVALUATION

The final point on the above “wish list” needs further clarification. To compare “performance” of tunings, it is necessary to have a figure-of-merit. Accordingly, this section introduces

<sup>1</sup>Low peak current is desirable as well, but as will be shown in Section III, it is the rms current that primarily affects efficiency.

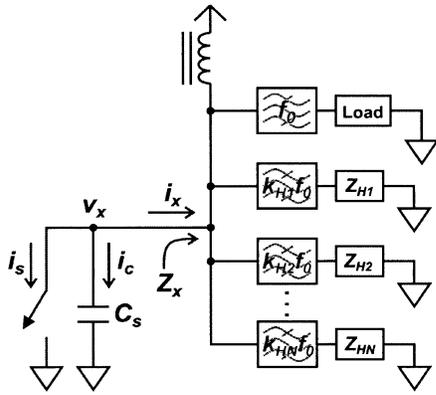


Fig. 6. Generalized harmonic-tuned switching amplifier circuit including switch output capacitance.

methods of approximating strong-switching amplifier performance from properties of the switching waveforms. First, however, it is necessary to visit some properties of switching amplifiers, to understand what a “tuning” is and how one changes under scaling of voltage and impedance. Additionally, a simple active device model is needed.

In the most general sense, a switching amplifier consists of a periodically driven switch connected to a passive load network, which is assumed to be linear and time-invariant (LTI). This one-port load includes any matching network, dc feed, and the load to be driven. The switch presents a time-varying conductance, alternating between very high conductance (i.e., “on”) and very low conductance (i.e., “off”). This forces the voltage to zero for the “on” duration of the cycle and the current to zero for the “off” duration, but leaves the waveforms otherwise unconstrained.

The voltage waveform, while switched “off,” and the current waveform, while switched “on,” are determined by the load network. Since this network is LTI, its properties may be specified by its input impedance as a function of frequency. If the waveforms are periodic, this impedance is relevant only for the fundamental and harmonic frequencies. Therefore, switching amplifier waveforms are completely specified by the impedance presented to the switch at the integer multiples of the fundamental frequency.

A generalized network suitable for implementation of most switching amplifiers is shown in Fig. 6. This topology represents the case where the switch is presented a capacitance, consisting partially of its own output capacitance, and a number of harmonic filters. Each filter presents a desired impedance at the harmonic it tunes, while leaving other harmonics unaffected. Thus, the circuit describes all switching amplifiers for which the impedance presented to the switch is capacitive at all harmonics, except for a finite number of tuned harmonics.

#### A. Scaling Properties

It is possible to analytically determine the switching waveforms of any circuit of the type shown in Fig. 6 [26]. Supposing the waveforms for one such circuit are known, it is useful to know how these waveforms change under simple scaling conditions. If waveforms are found for one case, then scaled solutions may be easily determined.

The first scaling technique needed for the results of this paper is *bias scaling*. Consider an amplifier whose solution is known for a given load network and dc-bias voltage  $V_{DD}$ . Suppose it is desired to find the waveforms of this amplifier under a bias of  $\alpha \cdot V_{DD}$ . Since the circuit is linear, albeit time varying due to the changing conductance of the switch, the scaled solution is simply the original voltage and current waveforms each scaled by a factor of  $\alpha$ . For instance, if the original current and voltage waveforms are  $I_{old}(t)$  and  $V_{old}(t)$ , respectively, the scaled current and voltage waveforms  $I_{new}(t)$  and  $V_{new}(t)$  are

$$V_{new}(t) = \alpha \cdot V_{old}(t) \quad (1)$$

$$I_{new}(t) = \alpha \cdot I_{old}(t). \quad (2)$$

The second technique is impedance scaling. Consider an amplifier whose solution is known for a given load network and dc-bias voltage. Suppose it is desired to know the waveforms for an amplifier operating at the same bias voltage, but with a load network presenting impedances  $Z_{new}(k)$  at each harmonic number  $k$ , equal to  $\alpha \cdot Z_{old}(k)$  for some real number  $\alpha$ , where  $Z_{old}(k)$  is the impedance presented by the original network. It is easily verified that the following scaled current and voltage, i.e.,  $I_{new}(t)$  and  $V_{new}(t)$ , respectively, give the correct waveforms provided that  $I_{old}(t)$  and  $V_{old}(t)$  were waveforms of the original amplifier

$$V_{new}(t) = V_{old}(t) \quad (3)$$

$$I_{new}(t) = \left(\frac{1}{\alpha}\right) \cdot I_{old}(t). \quad (4)$$

Using these scaling techniques, the initial solution can be transformed to have any independent scaling of the voltage and current. Since the waveforms of a group of thusly transformed tunings are identical in shape, and since their circuit topologies can be identical, the amplifiers in the group are considered to be using the same *tuning strategy* or *class of operation*. Thus, when comparing methods for harmonic tuning, it is implicit that the comparison is between the best amplifiers from each tuning group.

#### B. Simple FET Switch Model

A simple model for the nonideality of the switch is also required. Unlike amplifiers operating in classes A–C or F, strong-switching amplifiers do not have any built-in requirement for overlap between the voltage and current waveforms. Therefore, if the switch were ideal, the efficiency of every possible tuning would be 100%, rendering comparisons between tunings pointless. Switch nonideality, however, degrades performance to below this theoretical maximum in a manner that is dependent on the properties of the harmonic tuning.

Although bipolar switches have been popular and are suitable for many switching applications, the most capable high-frequency switching devices are field-effect transistors (FETs). A simple model suitable for FET switches is shown in Fig. 7. This model includes an on resistance, a linear output capacitance, and a simple network for input power approximation. Although not explicitly shown, it should be understood that the input power is a function of the frequency of operation. Up to the breakdown voltage  $V_{bk}$  of the switch, the off-state conductance of

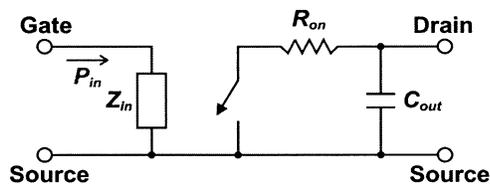


Fig. 7. Simple FET switch model.

the switch is assumed to be zero. While this model should not be expected to predict performance with great accuracy, it is useful for comparisons between tuning strategies, as it captures the first-order nonideal effects of FET switches.

Another important factor is the scalability of FET switches. By varying the effective gatewidth, the device in any given technology can be sized to optimize performance. As the size is increased, the on resistance decreases, the output capacitance increases, and the input power required to switch the transistor increases. In FETs, these parameters vary linearly or inversely with the device size. If the on resistance, output capacitance, and input power for a given device are  $\bar{R}_{on}$ ,  $\bar{C}_{out}$ , and  $\bar{P}_{in}$ , respectively, the parameters for a device scaled by a factor of  $\lambda$  are then

$$R_{on} = \left(\frac{1}{\lambda}\right) \cdot \bar{R}_{on} \quad (5)$$

$$C_{out} = \lambda \cdot \bar{C}_{out} \quad (6)$$

$$P_{in} = \lambda \cdot \bar{P}_{in}. \quad (7)$$

Reduction in on resistance is beneficial to the performance, but increase of output capacitance and input power are undesirable. Therefore, it should be expected that there is an optimal FET device size for a given technology and tuning strategy. Accordingly, comparisons between different tunings should assume the best combination of waveform scaling factors and device size.

### C. Assumptions and Limitations

Certain assumptions and design limitations help simplify the analysis. First, the effect of the nonidealities on the shape of the switching waveforms will be assumed to be small so that the conduction loss  $P_{cond}$  may be calculated using the rms value  $I_{RMS}$  of the switch current waveform for the case of an ideal switch

$$P_{cond} \approx I_{RMS}^2 R_{on}. \quad (8)$$

Using this and assuming that ZVS switching conditions are met so that no discharge loss occurs, the drain efficiency  $\eta$  can be calculated to be

$$\eta \equiv \frac{P_{out}}{P_{DC}} = \frac{P_{DC} - P_{cond}}{P_{DC}} \approx 1 - \frac{I_{RMS}^2 R_{on}}{V_{DC} I_{DC}} \quad (9)$$

where  $P_{out}$  is the output power,  $V_{DC}$  is the dc drain voltage, and  $I_{DC}$  is the dc drain current. Using this drain efficiency approximation, the power-added efficiency (PAE) is

$$PAE \equiv \frac{P_{out} - P_{in}}{P_{DC}} \approx \left(1 - \frac{P_{in}}{P_{out}}\right) \left(1 - \frac{I_{RMS}^2 R_{on}}{V_{DC} I_{DC}}\right). \quad (10)$$

The chief design limitations are that the peak voltage must not exceed the breakdown voltage for the device technology and that the switch output capacitance should not exceed the switch parallel capacitance  $C_S$ . These two limitations enforce a maximum dc bias and device size, each dependant on the properties of the tuning strategy.

Equation (9) can also be used to estimate efficiency from the waveform properties, supply voltage, and device on resistance. Rearranging (9)

$$\eta \approx 1 - \left(\frac{I_{RMS}}{I_{DC}}\right)^2 \left(\frac{R_{on}}{R_{DC}}\right) \quad (11)$$

$$R_{DC} \equiv \frac{V_{DC}}{I_{DC}} \approx \frac{V_{DC}^2}{P_{out}}. \quad (12)$$

In the high-efficiency case, this can be shown to give identical results as the well-known class-E result [6]

$$\begin{aligned} \eta_{class-E} &\approx \frac{1}{1 + \frac{\pi^2 + 28}{2 \cdot (\pi^2 + 4)} \cdot \frac{R_{on}}{R_{LOAD}}} \\ &\approx 1 - \frac{\pi^2 + 28}{2 \cdot (\pi^2 + 4)} \cdot \frac{R_{on}}{R_{LOAD}}. \end{aligned} \quad (13)$$

Using the ratio between  $R_{LOAD}$  and  $R_{DC}$ , this becomes

$$\eta_{class-E} \approx 1 - \frac{\pi^2 + 28}{16} \cdot \frac{R_{on}}{R_{DC}}. \quad (14)$$

### D. Waveform Figures-of-Merit

Using the results of the previous sections, it is possible to estimate switching amplifier performance from the basic waveforms of a tuning strategy. This section develops efficiency estimates under several design constraints.

1) *Maximum Drain Efficiency, Fixed Device Size:* Occasionally, the device size is limited to well below the theoretical performance-optimal size for the technology. This may occur at low frequencies where the optimal size is excessively large or for relatively new technologies where large devices are not available or prohibitively expensive. Accordingly, it is desirable to predict the optimized performance of a tuning strategy for a given output power  $P_{out}$ , when the device size is small and fixed. It is assumed that the device size is sufficiently small and that the output capacitance is necessarily smaller than  $C_S$ .

The terms of (9) may be rearranged to produce

$$\eta \approx 1 - \left(\frac{I_{RMS}}{I_{DC}}\right)^2 \left(\frac{V_{pk}}{V_{DC}}\right)^2 \left(\frac{R_{on}}{V_{pk}^2}\right) (V_{DC} I_{DC}). \quad (15)$$

The final term in this expression is the dc power consumed, which is  $P_{out}/\eta$ . Using this, (15) becomes

$$\eta \approx \frac{1}{2} + \frac{1}{2} \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 \left(\frac{V_{pk}}{V_{DC}}\right)^2 \left(\frac{R_{on}}{V_{pk}^2}\right) \cdot P_{out}}. \quad (16)$$

This may be expanded into the Taylor series

$$\eta \approx 1 - K - K^2 - \dots \quad (17)$$

$$K \equiv \left( \frac{I_{\text{RMS}}}{I_{\text{DC}}} \right)^2 \left( \frac{V_{\text{pk}}}{V_{\text{DC}}} \right)^2 \left( \frac{R_{\text{on}}}{V_{\text{pk}}^2} \right) \cdot P_{\text{out}}. \quad (18)$$

It is easily verified that the first term of  $K$ , the ratio between the rms and dc switch currents, is constant under both bias and impedance scaling, and is thus solely determined by the tuning strategy. Similarly, if  $V_{\text{pk}}$  is the peak voltage across the switch, the second term is also a function only of the tuning strategy. The final term is the output power, a design constraint. This leaves the third term. Since the efficiency (16) increases with increasing peak voltage, the optimum is achieved by setting this voltage as high as possible, decreasing rms current for the same output power. Since the peak voltage is limited solely by the transistor, the optimized third term is a function of the transistor technology. This optimum occurs when the peak voltage is equal to the device breakdown  $V_{\text{bk}}$ .

For comparisons between tunings, the first-order terms of (17) may be used under the assumption that efficiency is close to unity. Since the higher order terms have negative coefficients, comparisons using this simplification underestimate efficiency differences between tunings. Under the optimal condition  $V_{\text{pk}} = V_{\text{bk}}$ , this results in

$$\eta \approx 1 - \left( \frac{I_{\text{RMS}}}{I_{\text{DC}}} \right)^2 \left( \frac{V_{\text{pk}}}{V_{\text{DC}}} \right)^2 \left( \frac{R_{\text{on}}}{V_{\text{bk}}^2} \right) \cdot P_{\text{out}}. \quad (19)$$

This expression indicates that low rms to dc current ratios and low peak to dc voltage ratios are desirable. Similarly, a desirable FET device would have low on resistance relative to the squared breakdown voltage.

2) *Maximum Drain Efficiency, Optimal Device Size:* Another important case is the maximum drain efficiency for a given transistor technology where the optimal device size may be freely chosen. This might occur in cases where the cost of the incremental device area is small, and the device gain is large, allowing the drive power to be neglected. Using a similar technique as before, (9) is rearranged as

$$\eta \approx 1 - \left( \frac{I_{\text{RMS}}}{I_{\text{DC}}} \right)^2 \left( \frac{V_{\text{DC}} I_{\text{DC}}}{\omega_0 C_S V_{\text{DC}}^2} \right) (R_{\text{on}} C_{\text{out}}) (\omega_0) \left( \frac{C_S}{C_{\text{out}}} \right). \quad (20)$$

As before, effects of the waveforms have been separated from those of the transistor technology. The first term has already been encountered and is a function only of the tuning strategy. The second term is also invariant under both scaling techniques<sup>2</sup> and depends only on the tuning. The third term is a function only of the transistor technology being invariant under changes in transistor size. The next term indicates the linear degradation in optimal performance over frequency.

This leaves the final term, representing the proportion of the switch parallel capacitance  $C_S$  made up by the switch's output capacitance  $C_{\text{out}}$ . This term represents a degree of freedom, with the constraint that  $C_{\text{out}}$  cannot be greater than  $C_S$ . Clearly the best choice is to choose  $C_{\text{out}}$  as large as possible, thus the

optimal device size has the transistor output capacitance making all of  $C_S$

$$\eta \approx 1 - \left( \frac{I_{\text{RMS}}}{I_{\text{DC}}} \right)^2 \left( \frac{V_{\text{DC}} I_{\text{DC}}}{\omega_0 C_S V_{\text{DC}}^2} \right) (R_{\text{on}} C_{\text{out}}) (\omega_0). \quad (21)$$

To illuminate the meaning of the second term, consider that  $V_{\text{DC}} I_{\text{DC}}$  is approximately the output power and that  $1/(\omega_0 C_S)$  is the switch parallel capacitor's impedance magnitude at the fundamental frequency  $Z_C$

$$\eta \approx 1 - \left( \frac{I_{\text{RMS}}}{I_{\text{DC}}} \right)^2 \left( \frac{P_{\text{out}}}{\frac{V_{\text{DC}}^2}{Z_C}} \right) (R_{\text{on}} C_{\text{out}}) (\omega_0) \quad (22)$$

$$Z_C \equiv \frac{1}{(\omega_0 C_S)}. \quad (23)$$

Shown this way, the term can be viewed as a ratio between the output power and the reactive power in  $C_S$ . This measures the tuning's ability to utilize a large output capacitance (therefore, high reactive power) without necessitating large output power. Smaller values for this term allow larger device sizes for a given output power, reducing on resistance and, therefore, conduction loss.

Equation (22) indicates that it is desirable to have tunings with low rms to dc ratio in the current waveforms, and which tolerate large switch parallel capacitance relative to the output power for a given dc voltage. Similarly, a good transistor technology should have a small  $R_{\text{on}} C_{\text{out}}$  product relative to the switching period.

3) *Maximum PAE, Optimal Device Size:* The final case to be considered is the maximum PAE for a given transistor technology where the optimal sized device may be freely chosen. This is similar to the previous case, except that the gain is considered.

There are actually two possible cases. First, since drain loss is inversely proportional to the transistor size, whereas input power is proportional to this size, there is an optimum PAE point. An amplifier operating at this minimum may be said to be *gain limited* since an increase in transistor size is inadvisable due to the resulting decrease in gain. This minimum may not be achievable, however, since it is possible that the output capacitance of a device with gain-limited size might exceed the tuning's switch parallel capacitance  $C_S$ . Under this *capacitance-limited* condition, the best size will be the largest possible under the capacitance constraint, i.e., wherein  $C_{\text{out}} = C_S$ .

The gain-limited case will be examined first. Starting from (10), the transistor scaling rules of (5)–(7) are introduced as follows:

$$\text{PAE} \approx \left( 1 - \frac{\bar{P}_{\text{in}}}{P_{\text{out}}} \cdot \lambda \right) \left( 1 - \frac{I_{\text{RMS}}^2 \bar{R}_{\text{on}}}{V_{\text{DC}} I_{\text{DC}}} \cdot \frac{1}{\lambda} \right). \quad (24)$$

Optimizing over  $\lambda$  for maximum PAE results in

$$\text{PAE} \approx \left( 1 - \sqrt{\frac{I_{\text{RMS}}^2 \bar{R}_{\text{on}} \bar{P}_{\text{in}}}{V_{\text{DC}} I_{\text{DC}} P_{\text{out}}}} \right)^2. \quad (25)$$

<sup>2</sup>This term is also invariant under changes in the operating frequency since the tuning strategy is defined in terms of the impedances presented at the harmonics and, thus,  $\omega_0 C_S$  is constant over frequency for a given tuning.

Assuming the output power is approximately the dc power

$$\text{PAE} \approx \left[ 1 - \left( \frac{I_{\text{RMS}}}{I_{\text{DC}}} \right) \left( \frac{V_{\text{pk}}}{V_{\text{DC}}} \right) \left( \sqrt{\frac{\overline{P}_{\text{in}}}{\frac{V_{\text{pk}}^2}{R_{\text{on}}}}} \right) \right]^2. \quad (26)$$

The first two terms of this expression have been encountered previously and are functions only of the tuning strategy. The third term contains a degree of freedom, i.e., the peak voltage of the waveform. As before, the best performance is achieved by choosing this value as high as possible, with the limiting case being the technology's breakdown voltage. Setting  $V_{\text{pk}} = V_{\text{bk}}$  makes the third term a function only of the transistor technology, invariant under scaling of the transistor size

$$\text{PAE} \approx \left[ 1 - \left( \frac{I_{\text{RMS}}}{I_{\text{DC}}} \right) \left( \frac{V_{\text{pk}}}{V_{\text{DC}}} \right) \left( \sqrt{\frac{\overline{P}_{\text{in}}}{\frac{V_{\text{bk}}^2}{R_{\text{on}}}}} \right) \right]^2. \quad (27)$$

If the loss is small, this may be approximated as

$$\text{PAE} \approx 1 - 2 \cdot \left( \frac{I_{\text{RMS}}}{I_{\text{DC}}} \right) \left( \frac{V_{\text{pk}}}{V_{\text{DC}}} \right) \left( \sqrt{\frac{\overline{P}_{\text{in}}}{\frac{V_{\text{bk}}^2}{R_{\text{on}}}}} \right). \quad (28)$$

From this result, it is clear that rms to dc current ratios and low peak to dc voltage ratios are desirable.

The capacitance-limited case is very similar to the case of maximum drain efficiency explored in the previous section. In particular, the transistor size will be the same so that the drain efficiencies are identical. Thus, to calculate the PAE, it is only necessary to calculate the input power in the case wherein  $C_{\text{out}} = C_S$  and  $V_{\text{pk}} = V_{\text{bk}}$ . First noticing that the ratio of  $C_{\text{out}}$  to  $P_{\text{in}}$  is constant over changes in the transistor size, the input power may be expressed as

$$P_{\text{in}} = \frac{C_{\text{out}}}{\overline{C}_{\text{out}}} \overline{P}_{\text{in}} = \frac{C_S}{\overline{C}_{\text{out}}} \overline{P}_{\text{in}}. \quad (29)$$

Inserting this into the PAE expression, results in

$$\text{PAE} = \left( 1 - \frac{\overline{P}_{\text{in}} C_S}{P_{\text{out}} \overline{C}_{\text{out}}} \right) \cdot \eta. \quad (30)$$

Rearranging, keeping in mind that  $V_{\text{pk}} = V_{\text{bk}}$ , yields

$$\text{PAE} = \left[ 1 - \left( \frac{\overline{P}_{\text{in}}}{\overline{C}_{\text{out}} V_{\text{bk}}^2} \right) \left( \frac{V_{\text{DC}}^2}{Z_C} \right) \left( \frac{V_{\text{pk}}}{V_{\text{DC}}} \right)^2 \left( \frac{1}{\omega_0} \right) \right] \cdot \eta. \quad (31)$$

Combining this with (22) yields

$$\text{PAE} = \left[ 1 - \left( \frac{\overline{P}_{\text{in}}}{\overline{C}_{\text{out}} V_{\text{bk}}^2} \right) \left( \frac{F_V^2}{F_C} \right) \left( \frac{1}{\omega_0} \right) \right] \left[ 1 - (F_I^2 F_C) (\overline{R}_{\text{on}} \overline{C}_{\text{out}}) \omega_0 \right] \quad (32)$$

where the waveform factors have been represented as

$$F_V \equiv \frac{V_{\text{pk}}}{V_{\text{DC}}} \quad (33)$$

$$F_I \equiv \frac{I_{\text{RMS}}}{I_{\text{DC}}} \quad (34)$$

$$F_C \equiv \frac{P_{\text{out}}}{\frac{V_{\text{DC}}^2}{Z_C}}. \quad (35)$$

Also of note is the amplifier gain  $G$  in this case

$$G = \left( \frac{\omega_0 \overline{C}_{\text{out}} V_{\text{pk}}^2}{\overline{P}_{\text{in}}} \right) \left( \frac{F_C}{F_V^2} \right). \quad (36)$$

Although it may first appear that gain is increasing with frequency, it should be remembered that  $\overline{P}_{\text{in}}$  is itself a function of frequency. If a simple resistor/capacitor model of the input is used, this dependence is inverse with the square of the frequency. Thus, the gain of the optimally sized amplifier will reduce only inversely proportional to the frequency since the optimal device size in this case is reducing as frequency is increased.

Upon examining (32), the following conclusions are reached. As before, tunings with low rms to dc current ratio result in higher capacitance-limited drain efficiency. A low peak to dc voltage ratio improves gain. Having a large tolerance to output capacitance (i.e., low  $F_C$ ) allows for higher drain efficiency, but at the cost of reduced gain due to the associated increase in transistor size.

#### IV. CLASS-E/F AMPLIFIERS

With comparison methods in hand to decide between candidate tunings, the discussion turns toward finding these candidates. Until now, only two strong-switching harmonic tuning strategies suitable for use with large output capacitance have been introduced, i.e., class E and the "even harmonic resonant" class-E variant [27]. It would not be unreasonable to suspect that other tunings having superior characteristics may exist. From the standpoint of the  $F_I$  and  $F_V$  waveform metrics, class F is much better than class E, but has the drawback of being unrealizable in the strong switching case. An obvious first line of inquiry might attempt to achieve the benefits of class F (or  $F^{-1}$ ) tuning by constructing a hybrid tuning taking on characteristics of both E and F. The new class-E/F amplifier family, as its name suggests, is a method of achieving such a hybrid tuning between E and  $F^{-1}$ . Class  $F^{-1}$  is a natural choice for a ZVS amplifier hybrid since the ideal waveforms of this class are ZVS, unlike class F, which presents voltage discontinuities at the switching events in the ideal (all harmonics tuned) case. The E/F name is chosen to indicate that the hybrid is between E and class  $F^{-1}$  (i.e., class 1/F) rather than the more well-known class F.

Although one might suggest many different ways to compose such a hybrid, the method proposed here is a frequency-domain hybrid, choosing at each overtone to tune according to either the class- $F^{-1}$  or class-E method. In other words, some selection of even harmonics may be open circuited, some selection of odd harmonics may be short circuited, and the remaining harmonics

TABLE I  
SAMPLE CLASS-E/F HARMONIC TUNING SPECIFICATIONS IN  
FREQUENCY DOMAIN

	$f_0$	$2f_0$	$3f_0$	$4f_0$	$(5+)f_0$
$E/F_3$			short		
$E/F_{2,3}$		open	short		
$E/F_{2,4}$		open		open	
$E/F_{3,4}$			short	open	

are presented with a fixed capacitance. As in the class-E case, the fundamental frequency load resistance  $R_L$  and inductive reactance  $X_L$  are adjusted in order to achieve ZVS switching conditions.<sup>3</sup> This leaves one degree of freedom that may be used to set the slope of the voltage during the switch turn-on to zero, allowing for class-E switching conditions. If the number of class- $F^{-1}$  tuned harmonics is finite, the amplifier is realizable using the circuit of Fig. 6, although this is not necessarily the best implementation.

This technique may be used to produce many different tunings according to which overtones are tuned as class  $F^{-1}$  and, thus, a naming convention is required to differentiate between them. The names used herein are of the form Class  $E/F_{n_1, n_2, n_3, \dots}$ , where the numerical subscripts indicate the numbers of the class- $F^{-1}$  tuned harmonics. Table I shows the impedance specifications of several representative E/F amplifiers.

#### A. Waveforms and Tuning Requirements

Recently, a general analytic method for determining both the exact waveforms and fundamental frequency tuning of  $R_L$  and  $X_L$  to achieve ZVS conditions for any circuit of the form shown in Fig. 6 has been developed [26]. Although the solution details are beyond the scope of this paper, the results are summarized here.

Some sample E/F waveforms are depicted in Fig. 8. The waveforms contain features both of class-E and class- $F^{-1}$  amplifiers. Like class E, the voltage waveform switches at zero voltage and zero-voltage slope, while the current waveform has a discontinuity at the switch turn off, as is required in a ZVS amplifier [28]. The waveforms for small numbers of harmonics tuned tend to resemble class E and, as the number of tuned harmonics is increased, the resemblance to class  $F^{-1}$  increases. Low-order harmonics have the most effect, and even harmonics tend to primarily affect the current waveform, whereas odd harmonics tend to have the most effect on the voltage waveform.

<sup>3</sup>Class-E/F tunings are not limited to class-E switching conditions, and performance advantages may be found using a tuning with nonzero voltage slope at turn-on due to reduced peak voltage and larger capacitance tolerance.

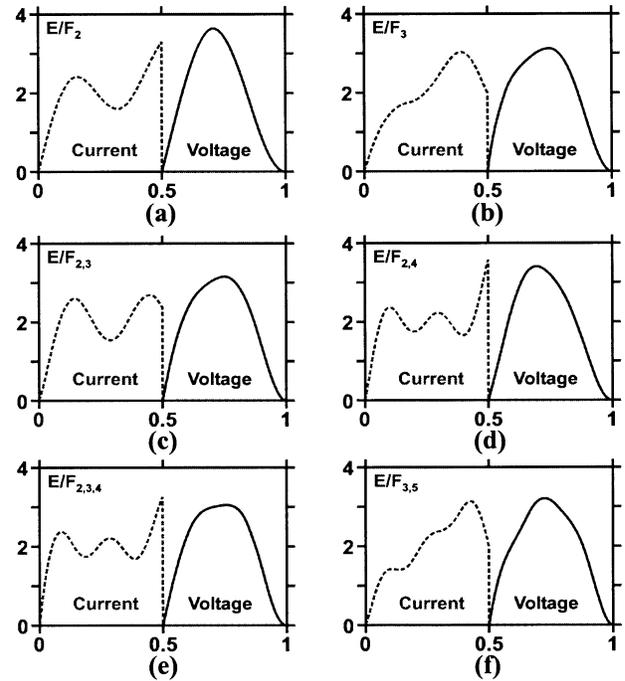


Fig. 8. Class-E/F amplifier waveforms. (a)  $E/F_2$ . (b)  $E/F_3$ . (c)  $E/F_{2,3}$ . (d)  $E/F_{2,4}$ . (e)  $E/F_{2,3,4}$ . (f)  $E/F_{3,5}$ . Waveforms are dc normalized and time is normalized to the switching period.

TABLE II  
WAVEFORM PROPERTIES FOR SAMPLE CLASS E/F AMPLIFIERS. SMALLER  
NUMBERS INDICATE BETTER PERFORMANCE

	$F_v$	$F_i$	$F_c$
E	3.56	1.54	3.14
$E/F_2$	3.67	1.48	1.13
$E/F_3$	3.14	1.52	3.14
$E/F_{2,3}$	3.13	1.47	2.31
$E/F_{2,4}$	3.43	1.46	0.97
$E/F_{2,3,4}$	3.08	1.45	1.18
$E/F_{3,5}$	3.20	1.51	3.14
$E/F_{2,3,4,5}$	3.20	1.45	2.11
$F^{-1}$	3.14	1.41	N/A

As can be seen from the sample waveforms, the peak to dc voltage ratio is generally lower than in class E, and the current waveform tends to resemble a square wave, lowering the rms to dc ratio. These effects are quantified in Table II, wherein the waveform figures-of-merit for various E/F tunings are shown.

For the tunings selected, only one of the amplifiers listed performs worse in any category than class E. Generally speaking, tuning the second harmonic tends to increase peak voltage, reduce rms current, and greatly increase tolerance to output capacitance. Tuning the third harmonic tends to reduce peak voltage, has little effect on rms current, and has a varying effect on capacitance tolerance. Tuning the fourth harmonic has varying effectiveness depending on which other harmonics have been tuned. The fifth harmonic, interestingly, usually has detrimental effects on the performance, e.g.,  $E/F_{2,3,4}$  shows better overall performance than  $E/F_{2,3,4,5}$ . This indicates that, unlike in class F and class  $F^{-1}$ , tuning of additional harmonics using the E/F method does not necessarily improve performance.

TABLE III

LOSS FACTORS FOR SELECTED E/F TUNINGS. THE FIRST THREE COLUMNS ARE DRAIN LOSS FACTORS FOR DIFFERENT CASES AND THE FOURTH COLUMN IS THE DRIVE LOSS FACTOR OF A CAPACITANCE-LIMITED AMPLIFIER

	$F_v^2 F_l^2$	$2F_v F_l$	$F_l^2 F_c$	$F_v^2 / F_c$
E	30.03	10.96	7.44	4.03
E/F <sub>2</sub>	29.57	10.87	2.49	11.9
E/F <sub>3</sub>	22.76	9.54	7.24	3.14
E/F <sub>2,3</sub>	21.25	9.22	5.02	4.24
E/F <sub>2,4</sub>	25.10	10.02	2.07	12.2
E/F <sub>2,3,4</sub>	20.08	8.96	2.50	8.00
E/F <sub>3,5</sub>	22.39	9.67	7.18	3.26
E/F <sub>2,3,4,5</sub>	21.68	9.31	4.47	4.85
F <sup>-1</sup>	19.74	8.88	N/A	N/A

Efficiency and gain factors for various E/F tunings are shown in Table III. The first column shows the waveform factor for the size-limited drain efficiency (22). As can be seen, several E/F tunings such as E/F<sub>2,3,4</sub> reduce the drain loss to around 67% that of class E. This improvement puts several class-E/F tunings into the same performance range as ideal class F<sup>-1</sup> and would serve to reduce the heat-sinking requirements by one-third. The second column shows the waveform factor for the gain-limited PAE, as in (28), and tells a similar story, although the improvements are more modest.

The application where E/F promises the most utility is the capacitance-limited drain efficiency case, as shown in the third column of this table. As can be seen, the E/F amplifiers can show extremely good performance under these conditions, in some cases reducing the expected drain loss to less than 30% that of class-E. This is accomplished by increasing the transistor size, as class-E/F tunings often show greatly increased tolerance to output capacitance, as indicated by their very low values of  $F_c$ . This additional efficiency comes at the price of gain, as shown in the fourth column of this table, but in many cases, the intrinsic device gain at the frequency of interest is high, but large output capacitance limits the device size in class-E amplifiers. Even if the designer does not wish to make full use of the available gain/efficiency tradeoff, he is free to choose any transistor size having an output capacitance smaller than the capacitance  $C_S$  with the remainder being made up by discrete capacitors.

## V. PUSH/PULL CLASS-E/F AND CLASS-E/F<sub>odd</sub> AMPLIFIERS

One issue in the implementation of class-E/F amplifiers is the difficulty of tuning the relatively large numbers of harmonics in a way that is both reasonably simple and low loss. Since each additional resonance added to the circuit introduces loss, it is desirable to reduce the stored energy in the resonators, i.e., make their loaded  $Q$ 's low. Unfortunately, this causes the effect of resonance to be broad in the frequency domain, spilling over into adjacent harmonics, usually with adverse effects. For instance, if a series  $LC$  resonator is used in a class-E/F<sub>3</sub> tuning to short circuit the third harmonic, it will present a capacitance at the second harmonic, reducing its impedance. This degrades the waveforms with regard to all three figures-of-merit, particularly  $F_c$ . Thus, either a very high loaded  $Q$  circuit must be used or additional resonances must be introduced into the circuit, increasing passive loss in either case.

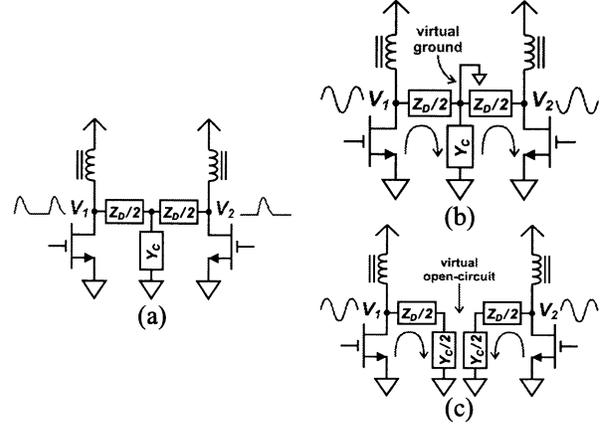


Fig. 9. Push/pull amplifier with a T network load. (a) Circuit topology. (b) Effect at odd harmonics. (c) At even harmonics.

There is, however, a more elegant way to separate the effects of the even and odd harmonic frequencies. By utilizing a symmetric push/pull switching amplifier circuit, the differing symmetries of the even and odd harmonics in the switching waveforms may be beneficially employed.

Consider, for instance, the circuit depicted in Fig. 9. The circuit uses two switches, each with 50% duty cycle, but operated such that when one switch is conducting, the other is open. Due to the symmetry, the switch waveforms are identical, except for a time delay of a half-cycle between them. Between the switches is a differential T-section load composed of a differential impedance  $Z_D$  and a common-mode conductance  $Y_C$ .

The effective impedance seen from each drain at each harmonic may be calculated. Due to the time-delay symmetry of the waveforms, the odd harmonic voltage components of each switch must be equal in amplitude, but opposite in phase. Consequently, a virtual ground develops at the line of symmetry at the center of the differential impedance, shorting across conductance  $Y_C$  so each switch sees an impedance of  $Z_D/2$ . At the even harmonics, however, the harmonic voltage components are equal in amplitude and phase. Thus, the line of symmetry becomes a virtual open circuit so the switches must share the conductance  $Y_C$ , each seeing an impedance of  $Z_D/2 + 2/Y_C$ .

Using this principle, an E/F<sub>3</sub> amplifier might be constructed by placing the third harmonic short circuit as a differential load, shorting the third harmonic using a low- $Q$  resonator without reducing the impedances of any even harmonics. Similar strategies may be used to selectively tune the impedances of even harmonics.

While this technique is itself useful for the efficient construction of the E/F amplifiers discussed in the previous section, it also opens up the very interesting possibility of short circuiting all odd harmonics by placing a differential short circuit between the two switches. To also avoid short circuiting the fundamental, a bandstop filter such as a parallel  $LC$  tank may be used to provide a differential short circuit at all frequencies other than the fundamental, as shown in Fig. 10. This technique yields an E/F<sub>3,5,7,9,...</sub> tuning, denoted hereafter as E/F<sub>odd</sub>.

This technique can be improved by further tuning several even harmonics, creating an E/F <sub>$x$ ,odd</sub> amplifier, where  $x$  is a set of tuned even harmonics. This can be accomplished with the

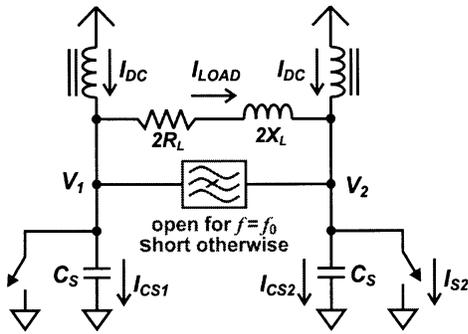


Fig. 10.  $E/F_{\text{odd}}$  circuit implementation using a push/pull amplifier and a bandstop filter.

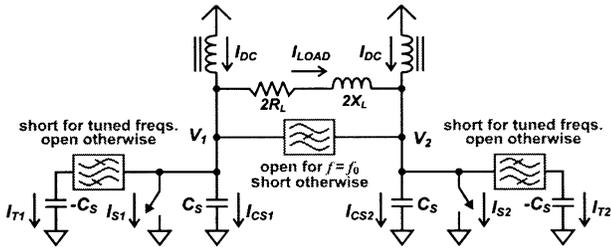


Fig. 11.  $E/F_{x,\text{odd}}$  conceptual circuit implementation. Additional resonant circuits parallel to each switch resonate with the switch capacitance  $C_S$  at selected even harmonics.

circuit of Fig. 11 using resonators added parallel to each switch. Each resonator may be treated analytically as a bandpass filter in series with capacitance  $C_S$ . The filter connects this negative capacitance parallel to the switch output capacitance at the tuned even harmonics, canceling the capacitance at these frequencies.

Unlike single-ended  $E/F$ , waveforms for  $E/F_{x,\text{odd}}$  amplifiers are derived with relative ease. In the amplifier of Fig. 11, the bandstop filter between the switches forces the differential voltage  $V_2 - V_1$  to be a sinusoid with frequency equal to the switching frequency  $f_0$ . Letting the amplitude and phase of the sinusoid be denoted  $V_D$  and  $\phi$ , respectively,

$$v_2 - v_1 = V_D \cdot \sin(\theta + \phi). \quad (37)$$

Since one switch is always on and, therefore, has zero voltage across it, the differential voltage may be used to calculate the voltages  $V_1$  and  $V_2$ . Assuming the left-most switch is closed for  $\pi < \theta < 0$

$$v_1 = \begin{cases} 0, & 0 < \theta < \pi \\ -V_D \cdot \sin(\theta + \phi), & \pi < \theta < 2\pi \end{cases} \quad (38)$$

$$v_2 = \begin{cases} V_D \cdot \sin(\theta + \phi), & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi. \end{cases} \quad (39)$$

Assuming a ZVS tuning is found, these voltage waveforms must be zero at turn on. The only nontrivial solution is for  $\phi$  to be zero, indicating that the properly tuned voltage is half-sinusoidal. As each switch is connected to the supply through an inductor, the dc voltage of each switch waveform must be the supply voltage  $V_{DC}$ . Since the peak to average ratio of a half-sinusoid is  $\pi$ , the voltages are

$$v_1 = \begin{cases} 0, & 0 < \theta < \pi \\ -\pi V_{DC} \cdot \sin(\theta), & \pi < \theta < 2\pi \end{cases} \quad (40)$$

$$v_2 = \begin{cases} \pi V_{DC} \cdot \sin(\theta), & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi. \end{cases} \quad (41)$$

From these voltages, the switch capacitor currents  $i_{CS1}$  and  $i_{CS2}$  may be calculated<sup>4</sup> as follows:

$$i_{CS1} = \begin{cases} 0, & 0 < \theta < \pi \\ -\pi \omega_0 C_S V_{DC} \cos(\theta), & \pi < \theta < 2\pi \end{cases} \quad (42)$$

$$v_1 = \begin{cases} \pi \omega_0 C_S V_{DC} \cos(\theta), & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi. \end{cases} \quad (43)$$

The frequency dependence may be removed by expressing the currents in terms of the capacitances' fundamental frequency impedance  $Z_C$

$$i_{CS1} = \begin{cases} 0, & 0 < \theta < \pi \\ -\left(\frac{\pi V_{DC}}{Z_C}\right) \cdot \cos(\theta), & \pi < \theta < 2\pi \end{cases} \quad (44)$$

$$v_1 = \begin{cases} \left(\frac{\pi V_{DC}}{Z_C}\right) \cdot \cos(\theta), & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi. \end{cases} \quad (45)$$

The even-harmonic resonator currents  $I_{T1}$  and  $I_{T2}$  may be calculated using the resonator impedance. The Fourier decomposition of the switch voltage waveforms are

$$v_1 = V_{DC} \cdot \left[ 1 - \frac{\pi}{2} \sin(\theta) - \sum_{k \in \{2,4,6,\dots\}} \left[ \frac{2}{k^2 - 1} \cos(k\theta) \right] \right] \quad (46)$$

$$v_2 = V_{DC} \cdot \left[ 1 + \frac{\pi}{2} \sin(\theta) - \sum_{k \in \{2,4,6,\dots\}} \left[ \frac{2}{k^2 - 1} \cos(k\theta) \right] \right]. \quad (47)$$

The admittance  $Y_T(k)$  of the tuning network at the  $k^{\text{th}}$  harmonic is

$$Y_T(k) = -\frac{jk}{Z_C}. \quad (48)$$

Using (46)–(48), the resonator currents  $I_{T1}$  and  $I_{T2}$  may be calculated. Denoting the set of tuned even harmonic numbers as  $T$

$$i_{T1} = i_{T2} = -\frac{V_{DC}}{Z_C} \cdot \sum_{k \in T} \left[ \frac{2k}{k^2 - 1} \sin(k\theta) \right]. \quad (49)$$

At any given time, one switch is nonconducting and the chokes conduct only dc current  $I_{DC}$ , all currents except that of the conducting switch are known. Therefore, the switch current may be found by Kirchhoff's current law (KCL)

$$i_{s1} = \begin{cases} 2I_{DC} - \frac{\pi V_{DC}}{Z_C} \cos(\theta) + \frac{V_{DC}}{Z_C} \sum_{k \in T} \left[ \frac{4k}{k^2 - 1} \sin(k\theta) \right], & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi \end{cases} \quad (50)$$

<sup>4</sup>Although the case presented here assumes a linear capacitance, the case of a nonlinear capacitance is also readily solved [19].

$$i_{s1} = \begin{cases} 0, & 0 < \theta < \pi \\ 2I_{DC} + \frac{\pi V_{DC}}{Z_C} \cos(\theta) + \frac{V_{DC}}{Z_C} \sum_{k \in T} \left[ \frac{4k}{k^2 - 1} \sin(k\theta) \right], & \pi < \theta < 2\pi. \end{cases} \quad (51)$$

With the switching waveforms in hand, the remaining task is to determine the fundamental-frequency load impedance. The load current  $i_{LOAD}$  is readily calculated using KCL

$$\dot{i}_{load} = \begin{cases} -I_{DC} + \frac{\pi V_{DC}}{Z_C} \cos(\theta) + \frac{V_{DC}}{Z_C} \sum_{k \in T} \left[ \frac{2k}{k^2 - 1} \sin(k\theta) \right], & 0 < \theta < \pi \\ I_{DC} + \frac{\pi V_{DC}}{Z_C} \cos(\theta) - \frac{V_{DC}}{Z_C} \sum_{k \in T} \left[ \frac{2k}{k^2 - 1} \sin(k\theta) \right], & \pi < \theta < 2\pi. \end{cases} \quad (52)$$

From the load current and voltage, their fundamental frequency Fourier components  $V_{LOAD}$  and  $I_{LOAD}$  are

$$V_{LOAD}(\omega = \omega_0) = j\pi V_{DC} \quad (53)$$

$$I_{LOAD}(\omega = \omega_0) = \frac{\pi V_{DC}}{Z_C} - \frac{V_{DC}}{\pi Z_C} \sum_{k \in T} \frac{8k^2}{(k^2 + 1)^2} + j\frac{4}{\pi} I_{DC}. \quad (54)$$

Computing the fundamental frequency differential load conductance as the ratio of this voltage and current yields

$$Y_{LOAD} = \left( \frac{4I_{DC}}{\pi^2 V_{DC}} \right) - j \cdot \left( \frac{1}{Z_C} \right) \left[ 1 - \frac{1}{\pi^2} \cdot \sum_{k \in T} \frac{8k^2}{(k^2 - 1)^2} \right]. \quad (55)$$

From this expression, the required load for ZVS operation is a resistance in parallel with an appropriately sized inductive susceptance, the size of which is determined by the harmonics tuned and the switch parallel capacitance.

This load conductance formula suggests a degree of freedom in the tuning. Since the conductance has no dependence on the capacitor  $C_S$  and the susceptance is a function only of this capacitance (and the tuning), the amplifier will operate in ZVS mode without retuning for any value of the load conductance and without the voltages on the switch or on the load changing. The current waveforms, however, do change. Expressing (50) in terms of the load resistance and the dc voltage yields

$$i_{s1} = \begin{cases} \frac{\pi^2 V_{DC}}{2R_L} - \frac{V_{DC}}{Z_C} \left[ \pi \cos(\theta) - \sum_{k \in T} \frac{4k}{k^2 - 1} \sin(k\theta) \right], & 0 < \theta < \pi \\ 0, & \pi < \theta < 2\pi. \end{cases} \quad (56)$$

This expression indicates that amplitude of the square wave component is a function only of the resistance, increasing as the resistance is decreased. The “ripple” component, consisting of the resonator and capacitor currents, is independent of the load resistance, being determined by the capacitance  $C_S$  and the harmonics tuned. This effect is depicted in Fig. 12, showing class-E/ $F_{odd}$  amplifier waveforms with varying load resistance.

This load invariance may be a useful in many applications, but even for systems driving a fixed load, this property may be applied. By keeping the load constant and varying  $C_S$ , an

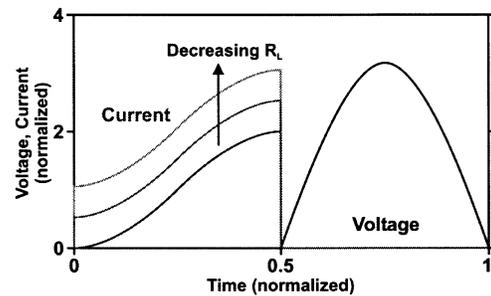


Fig. 12.  $E/F_{odd}$  waveforms for various values of load resistance  $R_L$  keeping switch parallel capacitance  $C_S$  constant.

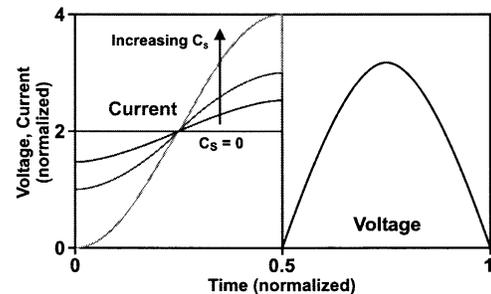


Fig. 13.  $E/F_{odd}$  normalized switching waveforms for various values of switch parallel capacitance  $C_S$ .

$E/F_{x,odd}$  tuning for a given output power and dc voltage may be found for *any* value of the capacitance  $C_S$  provided that the susceptance at the fundamental frequency is appropriately tuned. The current again changes according to (56), in this case, varying the amplitude of the ripple component as the value of the switch parallel capacitance is adjusted. If the capacitance is zero, the current is a square wave<sup>5</sup> and increasing capacitance results in higher peak and rms currents. This effect is shown in Fig. 13.

As can be seen, the rms current increases as the capacitance is increased. Unlike class E, wherein choosing too small of a value for  $C_S$  results in negative switch voltages—especially undesirable in FET devices with parasitic drain-bulk diodes—the  $E/F_{x,odd}$  circuit waveforms improve as the capacitance is decreased. Thus, unlike the class-E case, wherein capacitance is often added parallel to the switch, it would be foolish to do so in the  $E/F_{x,odd}$  case.

However, the capacitance will necessarily be small. Although the current waveforms improve with decreased capacitance, the on resistance improves with transistor size. The tunings for different output capacitances have different values of  $F_I$  and  $F_C$  and, thus, different performances. It is, therefore, necessary to indicate the size of capacitance being used in the amplifier when specifying the waveforms. Herein the waveforms will be specified by their  $F_C$  figure-of-merit relative to that of class E. For instance, a “2E” tuning would have an  $F_C$  half that of class E. Physically, this corresponds to tolerance for twice the capacitance of a class-E amplifier operating at the same output power from the same dc voltage.

Waveforms for selected  $E/F_{x,odd}$  amplifiers are shown in Fig. 14. For each of these tunings, the voltage waveform is

<sup>5</sup>This case is the well-known current mode class-D inverter [6].

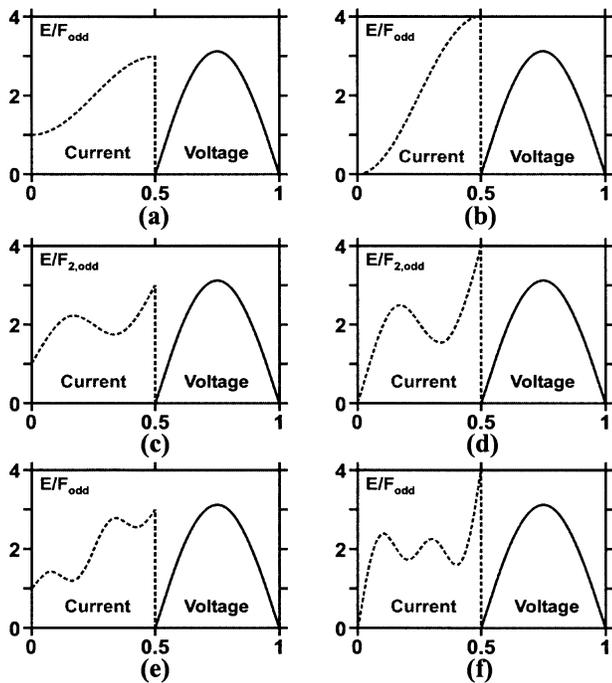


Fig. 14. Class- $E/F_{\text{odd}}$  waveforms. (a)  $E/F_{\text{odd}}$  “E” size device. (b)  $E/F_{\text{odd}}$  “2E” device. (c)  $E/F_{2,\text{odd}}$  “E” device. (d)  $E/F_{2,\text{odd}}$  “2E” device. (e)  $E/F_{4,\text{odd}}$  “E” device. (f)  $E/F_{2,4,\text{odd}}$  “2E” device. Waveforms are dc normalized, and time is normalized to the switching period.

a half-sinusoid. The current waveforms depend on the even harmonics tuned and the switch parallel capacitance. Using the basic  $E/F_{\text{odd}}$  tuning results in a nearly trapezoidal current waveform and open circuiting additional even harmonics has the effect of causing the current waveform to more closely approximate a square wave, even for very large values of the output capacitance. In this way, the even harmonic tuning is helpful for allowing even larger transistor sizes while keeping reasonable rms currents.

Waveform figures-of-merit for selected  $E/F_{x,\text{odd}}$  amplifiers are presented in Table IV. The peak voltage is in all cases equal to that of class  $F^{-1}$ , and the rms currents in many cases are nearly ideal. Like single-ended  $E/F$  amplifiers, the greatest improvement is in the capacitance tolerance factor  $F_C$ , which is dramatically improved in many cases.

Efficiency and gain factors for various  $E/F_{x,\text{odd}}$  tunings are presented in Table V. Different tunings excel in each performance category. Where transistor size is limited, the low  $F_V$  and  $F_I$  values for small capacitance tunings allow  $E/F_{\text{odd}}$  to approach the performance of class  $F^{-1}$  utilizing a circuit with only one resonator. In the gain-limited case, the lower peak voltage and the reduced rms current similarly improve performance. The capacitance limited case again promises the greatest performance improvement, with drain loss less than 30% of class E in some cases.

## VI. CONCLUSION

A new family of ZVS harmonic-tuned switching amplifiers has been introduced, each member of which may be constructed using a straightforward circuit, which absorbs the transistor output capacitance. These  $E/F$  tunings allow strong-switching

TABLE IV  
WAVEFORM FIGURES-OF-MERIT FOR VARIOUS  $E/F_{x,\text{odd}}$  TUNINGS

	$F_V$	$F_I$	$F_C$
E	3.56	1.54	3.14
$E/F_{\text{odd}}$ (E)	3.14	1.50	3.14
$E/F_{\text{odd}}$ (2E)	3.14	1.73	1.57
$E/F_{2,\text{odd}}$ (E)	3.14	1.44	3.14
$E/F_{2,\text{odd}}$ (2E)	3.14	1.51	1.57
$E/F_{2,4,\text{odd}}$ (E)	3.14	1.43	3.14
$E/F_{2,4,\text{odd}}$ (2E)	3.14	1.47	1.57
$E/F_{2,4,\text{odd}}$ (3E)	3.14	1.54	1.05
$E/F_{2,4,6,\text{odd}}$ (2E)	3.14	1.45	1.57
$E/F_{2,4,6,\text{odd}}$ (3E)	3.14	1.50	1.05
$E/F_{2,4,6,\text{odd}}$ (4E)	3.14	1.57	0.79
$F^{-1}$	3.14	1.41	N/A

TABLE V  
EFFICIENCY AND GAIN FACTORS FOR VARIOUS  $E/F_{x,\text{odd}}$  TUNINGS

	$F_V^2 F_I^2$	$2F_V F_I$	$F_I^2 F_C$	$F_V^2 / F_C$
E	30.03	10.96	7.44	4.03
$E/F_{\text{odd}}$ (E/2)	20.36	9.02	12.96	1.57
$E/F_{\text{odd}}$ (E)	22.21	9.42	7.07	3.14
$E/F_{\text{odd}}$ (2E)	29.61	10.88	4.71	6.38
$E/F_{2,\text{odd}}$ (E)	20.43	9.04	6.50	3.14
$E/F_{2,\text{odd}}$ (2E)	22.50	9.48	3.58	6.38
$E/F_{2,4,\text{odd}}$ (E)	20.14	8.98	6.41	3.14
$E/F_{2,4,\text{odd}}$ (2E)	21.36	9.24	3.40	6.38
$E/F_{2,4,\text{odd}}$ (3E)	23.38	9.67	2.48	9.42
$E/F_{2,4,\text{odd}}$ (2E)	20.89	9.14	3.32	6.38
$E/F_{2,4,6,\text{odd}}$ (3E)	22.33	9.45	2.37	9.42
$E/F_{2,4,6,\text{odd}}$ (4E)	24.34	9.87	1.94	12.6
$F^{-1}$	19.74	8.88	N/A	N/A

operation as in class E, but show a greater tolerance for transistor output capacitance and present waveforms approaching those of the more desirable class- $F^{-1}$ . The family exhibits a tradeoff between circuit complexity and performance. In addition to single-ended configurations, push/pull  $E/F_{x,\text{odd}}$  approaches take advantage of circuit symmetries to improve performance of class-E style amplifiers with little added circuit complexity.

## ACKNOWLEDGMENT

The authors would also like to thank K. Potter, California Institute of Technology, Pasadena, and J. Davis, Jet Propulsion Laboratory, Pasadena, CA, for their invaluable advice and assistance, as well as B. Kim, Pohang University of Science and Technology, Pohang, Korea, M. Morgan, National Radio Astronomy Observatory, Charlottesville, VA, H. Hashemi, California Institute of Technology, H. Wu, Axiom Microdevices Inc., Orange, CA, and D. Ham, Harvard University, Cambridge, MA, for the helpful discussions.

## REFERENCES

- [1] G. D. Ewing, “High-efficiency radio-frequency power amplifiers,” Ph.D. dissertation, Dept. Elect. Eng., Oregon State Univ., Corvallis, OR, 1964.
- [2] N. O. Sokal and A. D. Sokal, “Class-E: A new class of high-efficiency tuned single-ended switching power amplifiers,” *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 168–176, June 1975.
- [3] V. J. Tyler, “A new high-efficiency high power amplifier,” *Marconi Rev.*, vol. 21, no. 130, pp. 96–109, Fall 1958.

- [4] K. Tsai and P. R. Gray, "A 1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 962–970, July 1999.
- [5] M. D. Weiss, F. H. Raab, and Z. Popović, "Linearity of X-band class-F power amplifiers in high-efficiency transmitters," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1174–1179, June 2001.
- [6] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*. New York: Wiley, 1995.
- [7] C. Fallesen and P. Asbeck, "A 1 W CMOS power amplifier for GSM-1800 with 55% PAE," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 2001, pp. 911–914.
- [8] G. K. Wong and S. I. Long, "An 800 MHz HBT class-E amplifier with 74% PAE at 3.0 Volts for GMSK," in *IEEE GaAs IC Symp. Dig.*, Oct. 1999, pp. 299–302.
- [9] H. Kobayashi, J. M. Hinrichs, and P. Asbeck, "Current mode class-D power amplifiers for high efficiency RF applications," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 2480–2485, Dec. 2001.
- [10] B. Ingruber *et al.*, "Rectangularly driven class-A harmonic-control amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1667–1672, Nov. 1988.
- [11] C. J. Wei *et al.*, "Analysis and experimental waveform study of inverse class-F mode of microwave power FET's," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, June 2000, pp. 525–528.
- [12] A. Inoue *et al.*, "Analysis of class-F and inverse class-F amplifiers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 775–778.
- [13] W. S. Kopp and S. D. Pritchett, "High efficiency power amplification for microwave and millimeter frequencies," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Long Beach, CA, June 1989, pp. 857–858.
- [14] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2007–2012, Nov. 1997.
- [15] —, "Maximum efficiency and output of class-F power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1162–1166, June 2001.
- [16] K. Honjo, "A simple circuit synthesis method for microwave class-F ultra-high-efficiency amplifiers with reactance-compensation circuits," *Solid State Electron.*, vol. 44, no. 8, pp. 1477–1482, Aug. 2000.
- [17] F. H. Raab, "Class-E, class-C, and class-F power amplifiers based upon a finite number of harmonics," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1462–1468, Aug. 2001.
- [18] A. Mediano and P. Molina, "Frequency limitation of a high-efficiency class E tuned RF power amplifier due to a shunt capacitance," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Anaheim, CA, June 1999, pp. 363–366.
- [19] S. D. Kee, I. Aoki, and D. Rutledge, "7-MHz, 1.1-kW demonstration of the new E/F<sub>2,odd</sub> switching amplifier class," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 2001, pp. 1505–1508.
- [20] F. Bohn, S. Kee, and A. Hajimiri, "Demonstration of a harmonic-tuned class E/F<sub>odd</sub> dual band power amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, June 2002, pp. 1631–1634.
- [21] I. Aoki, S. D. Kee, D. Rutledge, and A. Hajimiri, "A 2.4-GHz, 2.2-W, 2-V fully-integrated CMOS circular-geometry active-transformer power amplifier," in *IEEE Custom Integrated Circuits Conf. Dig.*, San Diego, CA, 2001, pp. 57–60.
- [22] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer: A new power combining and impedance transformation technique," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 316–331, Jan. 2001.
- [23] —, "Fully-Integrated CMOS power amplifier design using distributed active transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, pp. 371–383, Mar. 2001.
- [24] F. H. Raab, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. SC-13, pp. 239–247, Apr. 1978.
- [25] H. Koizumi, T. Suetsugo, M. Fujii, and K. Ikeda, "Class DE high-efficiency tuned power amplifier," *IEEE Trans. Circuits Syst. I*, vol. 43, pp. 51–60, Jan. 1996.
- [26] S. D. Kee, "The class E/F family of harmonic-tuned switching power amplifiers," Ph.D. dissertation, Dept. Elect. Eng., California Inst. Technol., Pasadena, CA, 2002.
- [27] M. Iwadare, S. Mori, and K. Ikeda, "Even harmonic resonant class E tuned power amplifier without RF choke," *Electron. Commun. Japan*, pt. 1, vol. 79, no. 1, 1996.
- [28] M. K. Kazimierczuk, "Generalization of conditions for 100-percent efficiency and nonzero output power in power amplifiers and frequency multipliers," *IEEE Trans. Circuits Syst.*, vol. CAS-33, pp. 805–807, Aug. 1986.



**Scott D. Kee** was born in Albany, OR, in 1976. He received the B.E.E. degree in electrical engineering from the University of Delaware, Newark, in 1998, and the M.S.E.E. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, in 2002.

He is co-founder and Chief Technical Officer of Axiom Microdevices Inc., Orange, CA, a wireless communications startup. His current research interests include high-efficiency RF power amplifiers, switching amplifiers, and integrated circuit techniques for wireless communications.



**Ichiro Aoki** (S'98–M'01) was born in Kyoto, Japan, in 1965. He received the B.S.E.E. degree from the Universidade Estadual de Campinas, Campinas SP, Brazil, in 1987, and the M.S. and Ph.D. degree in electrical engineering from the California Institute of Technology (Caltech), Pasadena, in 1999 and 2001, respectively.

He co-founded and managed the PST Indústria Eletrônica da Amazônia Ltda., Campinas SP, Brazil (a car electronic components manufacturing company with 300 employees in 1998) from 1988 to 1998. In 2002, he co-founded Axiom Microdevices Inc., Orange, CA, a wireless semiconductor company, in where he served as acting Chief Executive Officer and is currently its Chief Architect and a member of the Board of Directors. His research interests include high-frequency silicon RF analog integrated circuits for wireless communications with emphasis on power amplifiers.

Dr. Aoki was the recipient of a Schlumberger Fellowship from 1998 to 1999 and the 2000 Walker von Brimer Foundation Award presented by Caltech.



**Ali Hajimiri** (S'95–M'98) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, in 1994, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1996 and 1998, respectively.

From 1993 to 1994, he was a Design Engineer with Philips Semiconductors, where he was involved with a BiCMOS chipset for global system for mobile communication (GSM) and cellular units. In 1995, he was with Sun Microsystems, where he was involved with

the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies (Bell Laboratories), Murray Hill, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, where his research interests are high-speed and RF integrated circuits. He coauthored *The Design of Low Noise Oscillators* (Boston, MA: Kluwer, 1999). He holds several U.S. and European patents.

Dr. Hajimiri is an associate editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING. He was a guest editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He has served as a member of the Technical Program Committees of the International Conference on Computer-Aided Design (ICCAD) and on the Guest Editorial Board of Transactions of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the Gold Medal winner of National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, The Netherlands. He was a corecipient of the International Solid-State Circuits Conference (ISSCC) 1998 Jack Kilby Outstanding Paper Award and the recipient of the IBM Faculty Partnership Award and the National Science Foundation CAREER Award.



**David Rutledge** (S'77–M'77–SM'89–F'93) received the B.A. degree in mathematics from Williams College, Williamstown, MA, the M.A. degree in electrical sciences from Cambridge University, Cambridge, U.K., and the Ph.D. degree in electrical engineering from the University of California at Berkeley.

He holds the Kiyo and Eiko Tomiyasu Chair of Electrical Engineering at the California Institute of Technology (Caltech), Pasadena. He is Director of Caltech's Lee Center for Advanced Networking.

His research has been in integrated-circuit antennas, active quasi-optics, computer-aided design, and power amplifiers. He authored the electronics textbook *The Electronics of Radio* (Cambridge, U.K.: Cambridge Univ. Press, 1999) and coauthored the microwave computer-aided software package *Puff*, which has sold 30 000 copies. Six of his former students have won Presidential Investigator and CAREER Awards from the National Science Foundation.

Dr. Rutledge was the recipient of the Microwave Prize and the Distinguished Educator Award of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), the Teaching Award of the Associated Students of Caltech, the Dough DeMaw Award of the American Radio Relay League (ARRL), and the Third Millennium Award of the IEEE. He is currently the editor-in-chief of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.