Application Notes

The General Feedback Theorem: A Final Solution for Feedback Systems

■ R. David Middlebrook

Are you an analog or mixed-signal design engineer or a reliability engineer? Are you a manager, a design-review committee member, or a systems integration engineer?

Did you "fall off a cliff" when in your first job you discovered that the analysis methods you learned in college simply don't work?

There is help available. Design-oriented analysis [(D-OA) don't forget the hyphen!] is a paradigm based on the recognition that design is the reverse of analysis, because the *answer* to the analysis is the *starting point* for design.

Conventional loop or node analysis leads to a result in the form of a "high entropy expression," which is a ratio of sums of products of the circuit elements. The more loops or nodes, the greater the number of factors in each product. By common experience, we know that we will sink into algebraic paralysis beyond two or three loops or nodes. Such an analysis result is useless for design.

In contrast, analysis results need to be derived in the form of "low entropy expressions," in which elements, such as impedances, are arranged in ratios and series-parallel combinations and not multiplied out into sums of products. This is the most important principle of D-OA, whose objective is to enable a designer to work backwards from an analytic result and change element values in an informed manner in order to make the answer come out closer to the desired result (the specification). D-OA is the only kind of analysis worth doing, since any other is a waste of time.

There are many methods of D-OA, some of them little more than shortcuts or tricks, but here the spotlight is on a new approach to analysis and design of feedback systems, based on the general feedback theorem (GFT).

A typical analysis procedure followed by designers, and integration and reliability engineers, is to throw the whole circuit into a simulator and see what it does, possibly including attempts to measure the loop gain as well as external properties. The design phase may consist of little more than tweaking and sensitivity simulations.

A much more efficient approach is to begin with a simple circuit in terms of device models absent capacitances and other parasitic effects and then to add these sequentially. Even if you do little or no symbolic analysis, successive simulations tell you in what ways which elements affect the result, so that when you finally substitute your library process and device models, you have a much better handle on where their effects originate.

This procedure of "D-OA by simulator" is significantly enhanced when the simulator incorporates the GFT, because the results for a feedback system are exact and not impaired by the approximations and assumptions inherent in the conventional single-loop model. Moreover, it may no longer be necessary to attempt hardware measurements of loop gain, which in itself is a considerable saving of time and effort.

What Is the Conventional Approach?

The well-established method of analyzing a feedback system begins with the familiar block diagram of Figure 1, from which the feedback ratio K and the loop gain $T = AK$ are calculated. The designer's job is to set K and the forward gain A so that the final closed-loop gain H meets a specification, usually with the help of circuit-simulator software. Several iterations, often aided by hardware measurements of the loop gain, may be needed before the closed-loop gain meets the specification.

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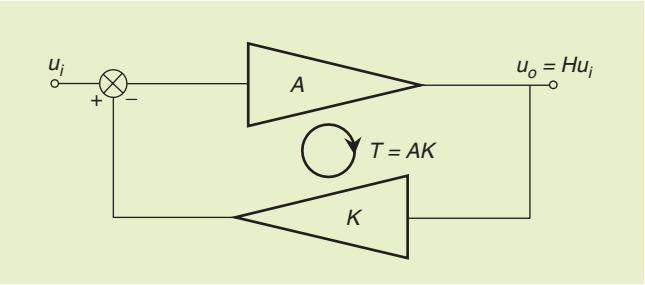

Figure 1. *The familiar single-loop block diagram of a feedback system. The arrowhead shapes imply that the signal goes only one way.*

Unfortunately, this approach can give incorrect results, stemming from the fact that the conventional block diagram of Figure 1 is an incomplete representation of the actual hardware system. Your immediate reaction to this allegation may be: "If I've noticed any discrepancies between the predicted and the actual results, they've been small enough to neglect, or I've just ignored them anyway."

Wouldn't it be better to be able to get the exact analysis results quickly and easily so that you could accurately predict the actual system performance? This desirable situation is now realized through use of the GFT.

Let's start by reviewing in more detail the conventional approach based on Figure 1, for which the closed-loop gain H (the "answer") is given by

$$H = \frac{A}{1+AK} = \frac{A}{1+T}. \tag{1}$$

A "better" form is

$$H = \frac{1}{K}\frac{AK}{1+AK} = H_\infty \frac{T}{1+T} = H_\infty \frac{1}{1+\frac{1}{T}} = H_\infty D, \tag{2}$$

where

$$H_\infty \equiv \frac{1}{K} \equiv \text{ideal closed-loop gain} \tag{3}$$

$$T \equiv AK \equiv \text{loop gain.} \tag{4}$$

It is convenient to define a discrepancy factor D as a unique function of T

$$D \equiv \frac{T}{1+T} \equiv \frac{1}{1+\frac{1}{T}} \equiv \text{discrepancy factor,} \tag{5}$$

so that the closed-loop gain H can be expressed concisely as

$$H = H_\infty D. \tag{6}$$

Form (2) is "better" because H_∞ represents the specification and is the only known quantity at the outset. So, $K = 1/H_\infty$ is designed to meet the specification, and the only hard part is designing the loop gain T so that the actual closed-loop gain H meets the specification within the required tolerances. That is, the discrepancy factor D must be close enough to one over the specified bandwidth.

One of the principles of D-OA is embodied in (2) and (6), namely "Get the quantities you want in the answer into the statement of the problem as early as possible." In this case, H_∞ is the desired gain, and D is the discrepancy between H_∞ and the actual answer you're going to get. Equally important, A is banished from the answer, because it contributes only via T, and its own value is of no interest.

It is clear from (5) that D is a unique function of T, which has several useful consequences. First, when T is large, $D \approx 1$, which leads to the desired result that $H \approx H_\infty$. Second, when T is small, $D \approx T$ and is small also, leading to a significant discrepancy between H_∞ and T.

Third, *where* the magnitude of T falls to one, the crossover frequency, marks the end of the frequency range over which T performs its useful function. *How* T crosses over determines the degree of peaking exhibited by D during its transition between one when T is large to T when T is small. According to (5), peaking in D is related to the phase margin of T, and translates by (6) directly to the closed-loop response H.

Thus, (5) and (6) expose the well-known unique relationship between loop gain phase margin and both the frequency and time domain responses of the closed-loop gain.

What's Wrong with the Conventional Approach?

The model of Figure 1 is incomplete because it does not account for bidirectional signal transmission in the boxes. In fact, the boxes are drawn as arrowheads on purpose to emphasize that reverse transmission is excluded. If both boxes have reverse transmission, there is also a nonzero reverse-loop gain, and it is convenient to lump together all the properties omitted from this block diagram under the label *nonidealities*. Consequently, all analysis based on this model also ignores the nonidealities.

In most textbooks and handbooks you can find whole sections that postulate a model in which each box of Figure 1 is replaced by a two-port model, thus retaining the bidirectionality of a real circuit. However, there are several disadvantages to this approach:

1) Four different sets of two-port models are required to represent the four possible feedback configurations: shunt-shunt, series-shunt, etc., and in three of the four, the model itself is still inaccurate because common-mode gain is ignored.
2) Even though the nonidealities are incorporated in the model, how do you account for their effects upon the loop gain and the closed-loop response?
3) Because the circuit elements are buried inside the two-port parameters, which are themselves buried in expressions for the loop gain and closed-loop gain, the results are high entropy expressions and are essentially useless for design.

The Dissection Theorem Is a Completely General Property of a Linear System Model

The GFT sweeps away all the a priori assumptions and approximations inherent in the previously described conventional approach and produces low entropy results directly in terms of the circuit elements. This is accomplished because the GFT does not start from a block diagram model but is developed from a very basic property of a linear system, the dissection theorem.

The dissection theorem says that any "first level" transfer function (TF) H of a linear system can be dissected into a combination of three "second level" TFs $TF1$, $TF2$, and $TF3$ according to

$$H = TF1\frac{1+\frac{1}{TF3}}{1+\frac{1}{TF2}}. \tag{7}$$

These TF symbols are intentionally anonymous so that different physical significances can be assigned later.

The second-level TFs are calculated in terms of an injected test signal u_z, as shown in Figure 2. The injected test signal sets up u_x going "forward" towards the output u_o, and u_y going "backward" towards the input u_i, such that $u_x + u_y = u_z$, in which u_x, u_y, u_z may be all voltages or all currents, and u_i and u_o can independently be a voltage or a current.

The second level TFs are defined by

$$TF1 \equiv \left.\frac{u_o}{u_i}\right|_{u_y=0} \quad TF2 \equiv \left.\frac{u_y}{u_x}\right|_{u_i=0} \quad TF3 \equiv \left.\frac{u_y}{u_x}\right|_{u_o=0}, \tag{8}$$

and the first-level TF H is simply the output divided by the input (the "gain") in the absence of the test signal:

$$H \equiv \left.\frac{u_o}{u_i}\right|_{u_z=0}. \tag{9}$$

In (8), $TF2$ is the ratio of the signal going backward to the signal going forward from the test signal injection point, under the condition that the original input signal is zero. This is a "single injection" (si) calculation, the familiar method by which any TF is calculated.

$TF1$ is the ratio of the output to the input when u_y is nulled, a condition that is established by adjustment of the test signal u_z so that its contribution to u_y is exactly equal and opposite that from u_i. This is a less familiar "null double injection" (ndi) calculation. Note that, while H and $TF1$ are both ratios of output to input, their values are different because, even if the input u_i is the same, the u_o for $TF1$ contains a component due to u_z that is absent in the u_o for H.

An ndi *calculation* is made after an ndi *condition* has been established and is always *easier and simpler* than an si calculation. This is not an accident: any element in the system that supports a null signal might as well not be there and does not appear in the calculation or in the result. Also, you don't have to know what the relation between the two injected signals is; all you have to know is the equivalent information that the null exists. To emphasize this, consider the way to make the null self-adjusting shown in Figure 3: the imaginary infinite gain amplifier automatically nulls u_y, and to calculate $TF1$ from (8), you simply use the fact that u_y is nulled, and you don't have to know what u_z is. The method of Figure 3 can be implemented in a circuit simulator, since the "nulling amplifier" bandwidth is infinite, even if its gain is not.

The $TF3$ in (8) is also an ndi calculation, and no further explanation is necessary. The (different) ndi condition can be established by connecting the nulling amplifier input to u_o instead of to u_y.

If you're not familiar with the dissection theorem, you can easily verify (7) by setting up a set of equations that represent the properties of a linear system containing two independent sources u_i and u_z:

$$u_x = \mathcal{A}u_o + \mathcal{B}u_z \tag{10}$$

$$u_y = \mathcal{C}u_i + \mathcal{D}u_z \tag{11}$$

$$u_z = u_x + u_y. \tag{12}$$

You can evaluate the TFs of (8) and (9) in terms of the $\mathcal{A}$, $\mathcal{B}$, $\mathcal{C}$, $\mathcal{D}$ coefficients. For example, to find $TF1$, set $u_y = 0$ in (11) and solve for the ratio $u_z/u_i = -\mathcal{C}/\mathcal{D}$ that nulls u_y. In (10), $u_x = u_z$ by virtue of $u_y = 0$ in (12). Thus, $u_o = (1-\mathcal{B})u_z/\mathcal{A}$. Finally, substitute $u_z/u_i = -\mathcal{C}/\mathcal{D}$ to get $TF1 = (\mathcal{B}-1)\mathcal{C}/\mathcal{A}\mathcal{D}$. Likewise, find $TF2$ and $TF3$, and insert all three TFs into (7) to confirm that the result for H is the same as that obtained directly from (10)–(12) by setting $u_z = 0$, which makes $u_x = -u_y$ and $H = -\mathcal{C}/\mathcal{A}$.

What Is the Dissection Theorem Good for?

The dissection theorem is completely general, the only constraint being that it applies to linear systems. As with most theorems, the important thing is what is it good for, and how do you use it?

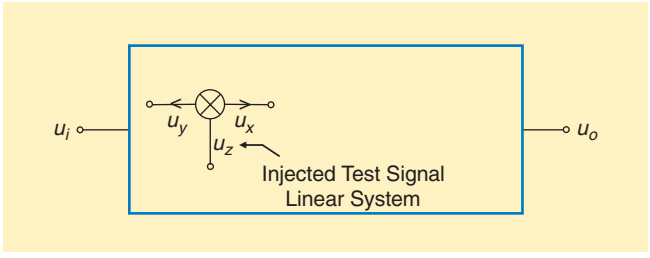

Figure 2. *General model of a linear system with input u_i and output u_o and an injected test signal u_z.*

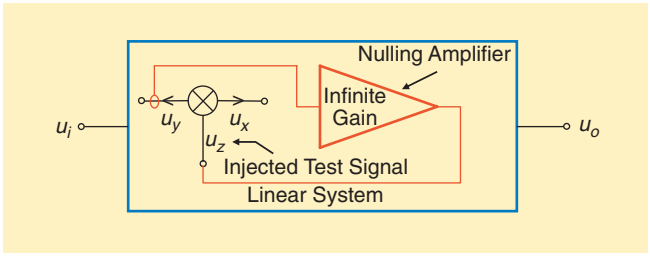

Figure 3. *How to set up an ndi condition: u_y is automatically nulled.*

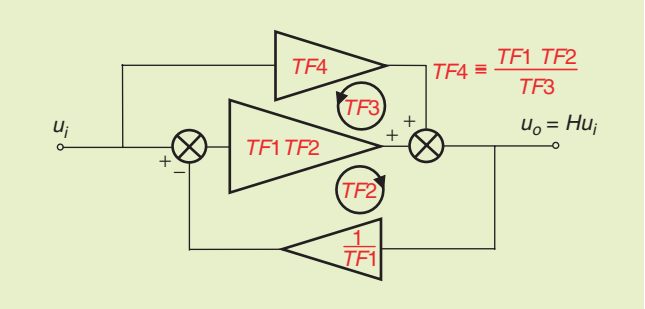

Figure 4. *This augmented block diagram with anonymous TFs represents the dissection theorem (7).*

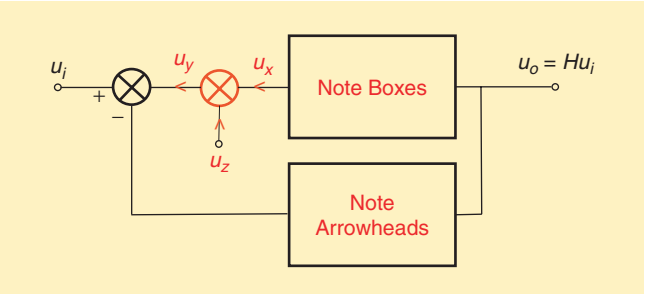

Figure 5. *When the test signal is injected inside the loop at the error-summing point, the dissection theorem of (7) becomes the GFT (15).*

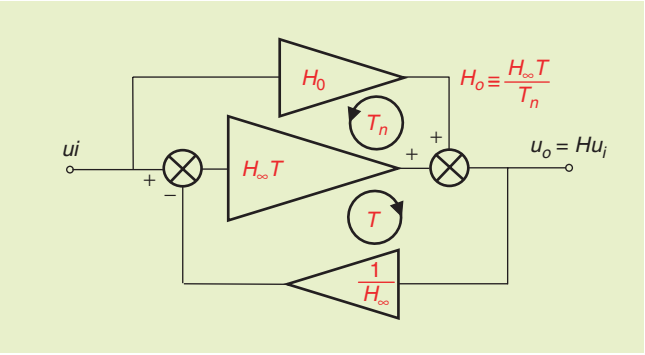

Figure 6. *This block diagram for the GFT is a morphed version of Figure 4, in which T_n (or H_0) represents the main effects of the nonidealities.*

At first sight, you might think that replacing one calculation by three is a step in the wrong direction. On the contrary, since (7) is itself a low entropy expression, the influences of $TF2$ and $TF3$ in modifying $TF1$ are exposed, which is helpful design-oriented information. Moreover, since two of the three second-level definitions of (8) are ndi calculations, the dissection theorem replaces a single complicated calculation by three potentially simpler calculations, thus implementing another of the principles of D-OA: "divide and conquer."

Nevertheless, these are minimum benefits, and much greater benefits accrue if the second-level TFs have useful physical interpretations. Thus, the second level TFs (8) themselves contain the useful design-oriented information, and you may never need to actually substitute them into (7). For example, if $TF2$, $TF3 \gg 1$, $H \approx TF1$.

How do we determine the physical interpretations of (8)? In the above discussion based on Figure 2, nothing was said about *where* in the system model the test signal is injected. Different test-signal injection points define different sets of coefficients $\mathcal{A}, \mathcal{B}, \mathcal{C}, \mathcal{D}$ and, hence, different sets of second level TFs. However, when a mutually consistent set is substituted into (7), the *same* H results:

$$H = TF1a\frac{1+\frac{1}{TF3a}}{1+\frac{1}{TF2a}} = TF1b\frac{1+\frac{1}{TF3b}}{1+\frac{1}{TF2b}} = \ldots . \tag{13}$$

Therefore, the *key decision* in applying the dissection theorem is choosing a test signal injection point so that at least one of the second level TFs has the physical interpretation you want it to have.

The Dissection Theorem Can Morph into the Extra Element Theorem

For example, if the injection point is chosen so that u_y goes into (voltage across, or current into) a single impedance $\boldsymbol{Z}$, (7) becomes

$$H = H|_{Z=\infty}\frac{1+\frac{Z_n}{Z}}{1+\frac{Z_d}{Z}}, \tag{14}$$

in which Z_d, Z_n are respectively the driving-point impedance and the null driving-point impedance seen by $\boldsymbol{Z}$, and $H|_{Z=\infty}$ is the value of H when $\boldsymbol{Z}$ is infinite. In this form, the dissection theorem becomes the extra element theorem (EET), of which a useful special case is when $\boldsymbol{Z}$ is the only capacitance in an otherwise resistive circuit. Then, $H|_{Z=\infty}$ is the first level TF (the "gain") when the capacitance C is absent (zero), and the pole and zero are exposed directly as $1/CR_d$ and $1/CR_n$.

The EET will not be further discussed here, because the spotlight is on another example of the choice of injection point.

The Dissection Theorem Can Morph into the GFT

It is easy to see that the block diagram of Figure 4 represents (7) and is immediately recognizable as an augmented version of the conventional feedback block diagram of Figure 1, which represents (2). So, where does the test signal have to be injected so that $TF1$ has the physical interpretation of H_∞?

The answer is obvious: since H_∞ is H when the error signal vanishes (infinite loop gain), and $TF1$ is H when u_y is nulled, then u_z must be injected at the error summing point so that u_y represents the error signal.

At the same time, this makes $TF2$ have the physical interpretation of the loop gain T, since the test signal injection point is inside the loop.

Finally $TF3$, which does not have a corresponding appearance in Figure 1, is a new TF that can be designated T_n, since by (8) it is defined as a loop gain with u_o nulled.

Following the above procedure, (7) becomes

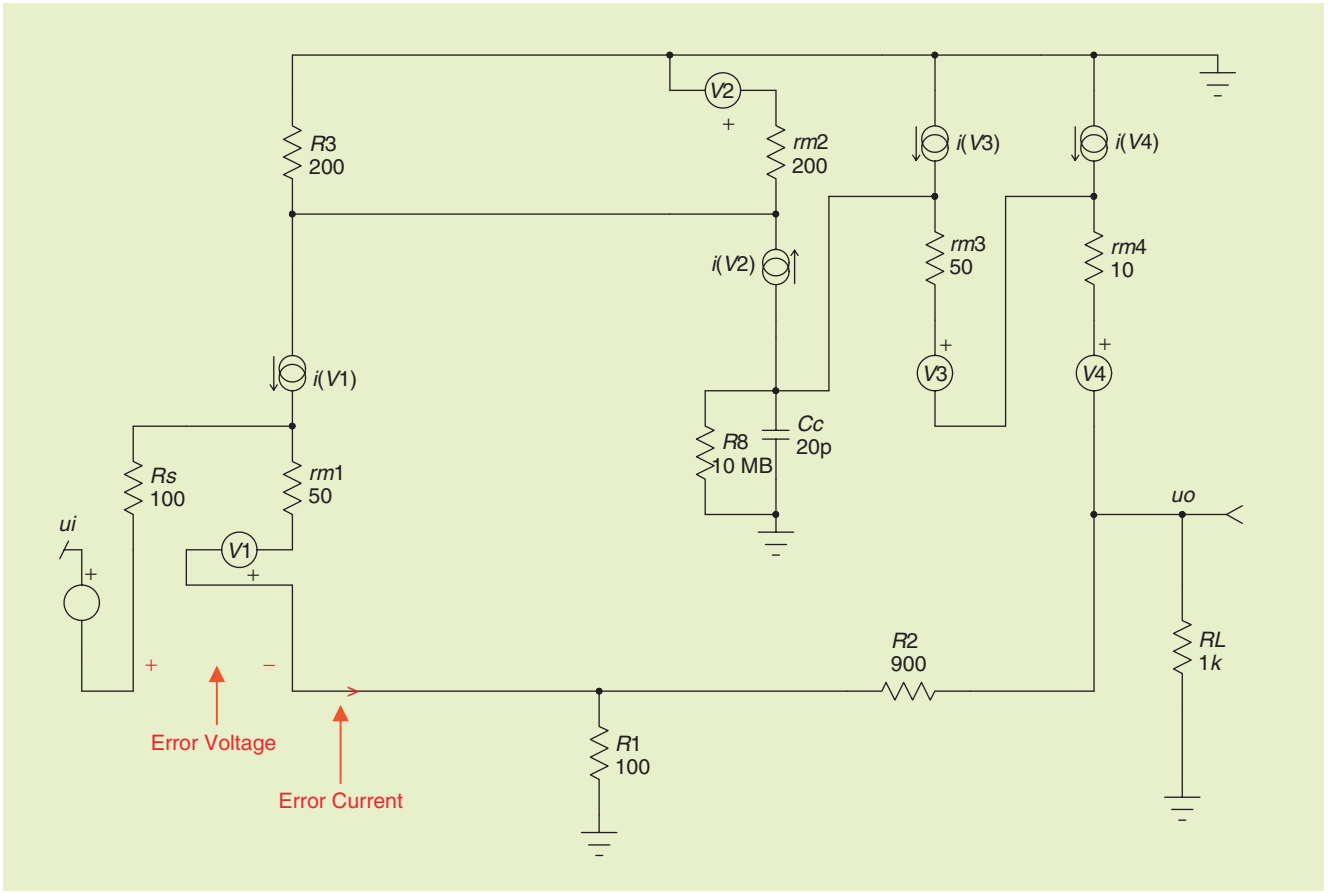

Figure 7. *A simple feedback amplifier model with the error voltage and the error current identified.*

$$H = H_\infty \frac{1 + \frac{1}{T_n}}{1 + \frac{1}{T}}, \tag{15}$$

and, in this form, the dissection theorem becomes the GFT. For the second-level TFs to have the desired physical interpretations $TF1 = H_\infty$, $TF2 = T$, $TF3 = T_n$, the test signal u_z must be inside the loop and at the error summing point, as illustrated in Figure 5. Then, (8) becomes

$$H_\infty \equiv \left.\frac{u_o}{u_i}\right|_{u_y=0} \quad T \equiv \left.\frac{u_y}{u_x}\right|_{u_i=0} \quad T_n \equiv \left.\frac{u_y}{u_x}\right|_{u_o=0}. \tag{16}$$

With H_∞, T, and T_n calculated from (16), the result (15) is represented by the "augmented" block diagram of Figure 6.

Because, superficially, Figure 6 differs from Figure 1 only in the presence of an additional block that contains the nonidealities, it is important to emphasize the fundamental difference between the conventional approach and that based on the GFT.

In the conventional approach, the block diagram of Figure 1 is the *starting point*, in which reverse transmission in both boxes is ignored, and the result (2) is developed from Figure 1.

In the GFT approach, Figure 5 is the *starting point*, and the result (15) is developed from (16) directly from the complete circuit *without any assumptions or approximations.* Since (15) is represented by Figure 6, the block diagram of Figure 6 is *part of the result*. The boxes in Figure 6 are unidirectional and *do not necessarily correspond to any separately identifiable parts of the circuit*. The values of these boxes, expressed in terms of the second level TFs H_∞, T, and T_n, *automatically incorporate* any nonidealities that may be present in the actual circuit.

Although the augmented block diagram exhibits a "loop," it represents any linear system even if there is not a physically discernible loop. An example is a Darlington follower, for which the GFT affords a means of investigating the well-known potential instability.

It is apparent that the null loop gain T_n contains the first-order effects of nonidealities, although there may also be second-order effects upon the loop gain T. Thus, the T in (2) may not be the same as *the correct* T in (15).

Since it was convenient in (5) to introduce the discrepancy factor D as a unique function of T, it is likewise useful to introduce the null discrepancy factor D_n as a unique function of T_n, according to

$$D_n \equiv \frac{1 + T_n}{T_n} \equiv 1 + \frac{1}{T_n} \equiv \text{null discrepancy factor} \tag{17}$$

so that the final result for the first level TF T can be written

$$H = H_\infty D D_n. \tag{18}$$

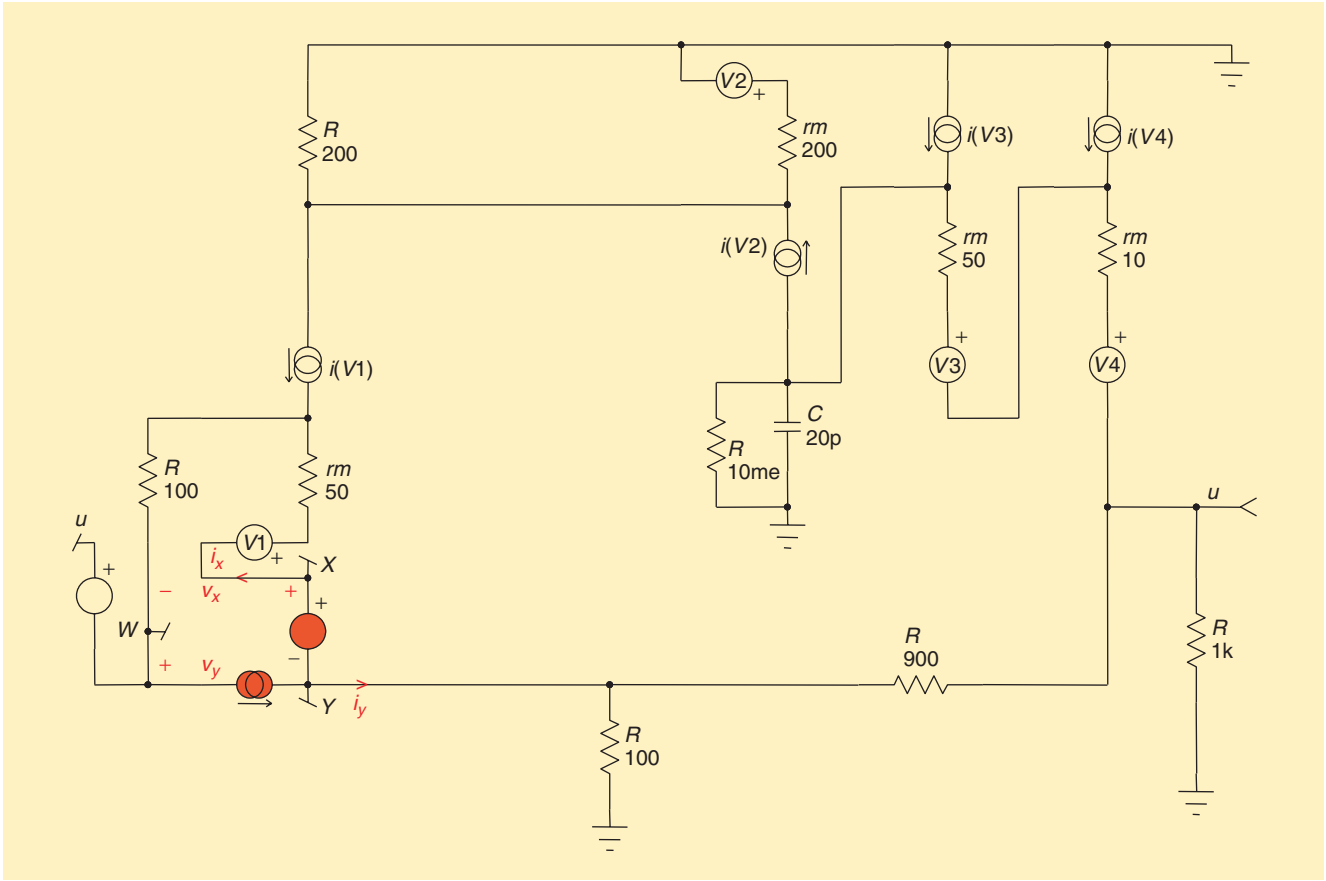

Figure 8. *The crucial step: choose the test signal injection point inside the loop so that v_y is the error voltage and i_y is the error current.*

The importance of this result is that the familiar tenet must be modified: *the closed-loop frequency domain and time domain responses are no longer uniquely determined by the loop gain T and its phase margin.* Instead, these responses are modified by a noninfinite value of the null loop gain T_n via a nonunity value of the null discrepancy factor D_n.

Calculation of the second level TFs H_∞, T, and T_n can be done symbolically, or numerically by use of a circuit simulator. The Intusoft ICAP/4 simulator incorporates GFT templates that apply a voltage or current test signal, set up the appropriate si and ndi conditions, and perform the required calculations. As a user, all you have to do is choose the proper test-signal injection point, which is inside the loop at the error-summing point.

However, before proceeding to a circuit example, it is necessary to make an extension of the dissection theorem.

The GFT for Two Injected Test Signals Is the "Final Solution"

From Figure 2, the Dissection Theorem was developed in terms of a single injected test signal u_z, but a general version can be developed in terms of any number of test signals injected at different points. The EET interpretation in terms of N test signals becomes the NEET, and, although this is "NEET," it won't be discussed further here.

For the GFT interpretation, the most useful version employs two injected test signals, a voltage e_z and a current j_z, both injected at the error-summing point. This is because, to make H_∞ equal to $1/K$, the ideal closed-loop gain, both the error voltage v_y and the error current i_y have to be nulled simultaneously.

For dual voltage and current injected test signals at the error-summing point, the GFT of (7) *remains exactly the same*, except that the *definitions* of the TFs are extended. In particular,

$$H_\infty \equiv \left.\frac{u_o}{u_i}\right|_{v_y, i_y = 0}, \tag{19}$$

which says that H_∞ is established by the double-null triple-injection (dnti) condition that e_z and j_z are mutually adjusted with respect to u_i so that v_y and i_y are both nulled. The definitions of T and T_n are each extended to a combination of voltage and current loop gains established by ndi conditions for T and by dnti conditions for T_n. These definitions are not displayed here because the circuit examples will be treated by use of the Intusoft ICAP/4 GFT templates, in which all the calculations needed for dual test signal injection are included and are, therefore, transparent to the user.

Are dnti calculations even easier than ndi calculations? Absolutely: the more signals are nulled, the more circuit elements do not appear in the answer. This constitutes another round of the "divide and conquer" approach: you make a *greater* number of *less* complicated calculations.

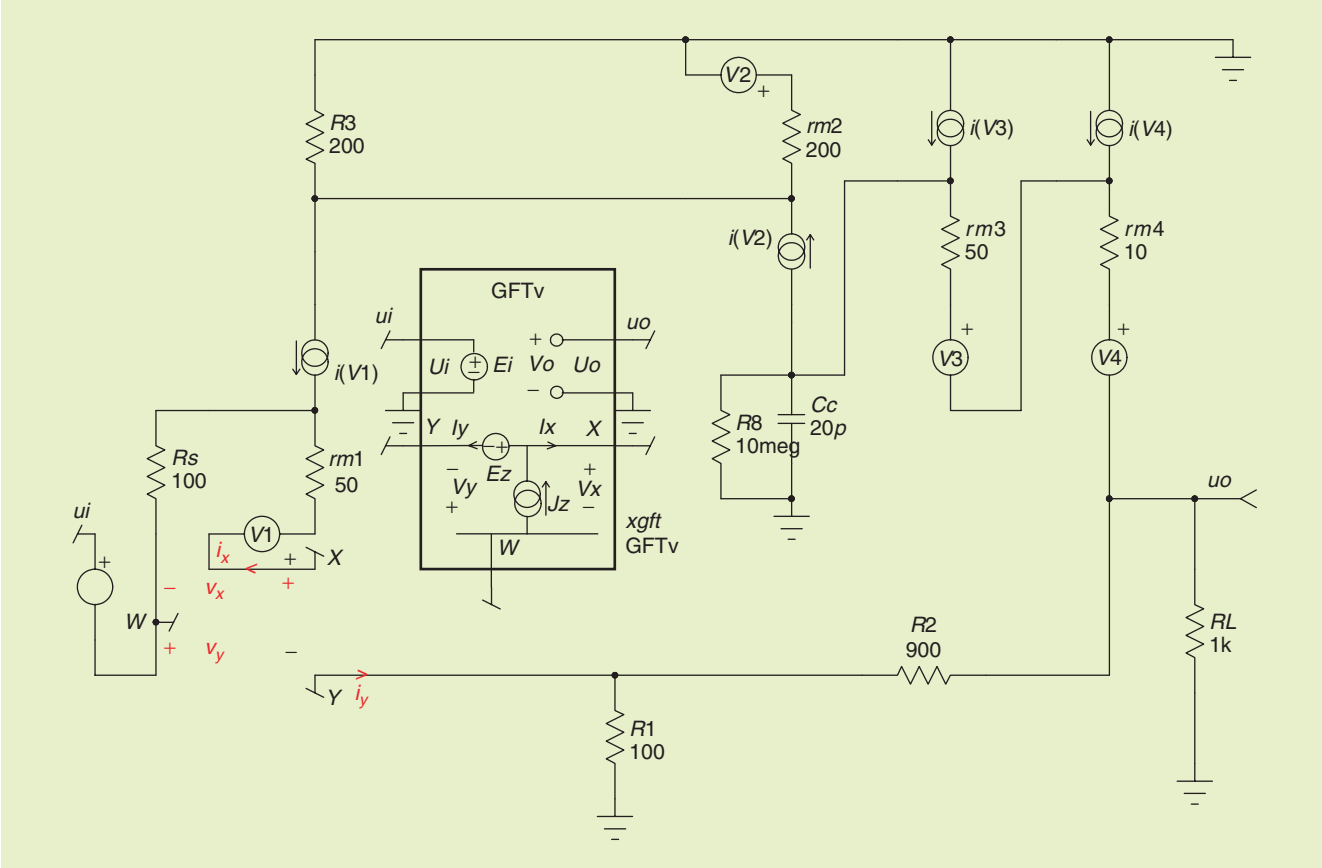

Figure 9. *An Intusoft ICAP/4 GFT template provides the injected test signals e_z and j_z, and performs the simulations and postprocessing required to obtain H_∞, T, and T_n, and hence H, for the GFT of (15).*

How to Use a Circuit Simulator Incorporating GFT Templates

In any case, if you're going to use a circuit simulator rather than doing symbolic analysis, all you need to do is choose an injection point inside the loop at the error-summing point, plus select the appropriate GFT template according to whether single or dual test signal injection is required to null simultaneously the voltage and current error signals. The template does simulation runs to calculate the second-level TFs H_∞, T, and T_n in (15) and does post-simulation calculations to produce the discrepancy factors D and D_n in (18).

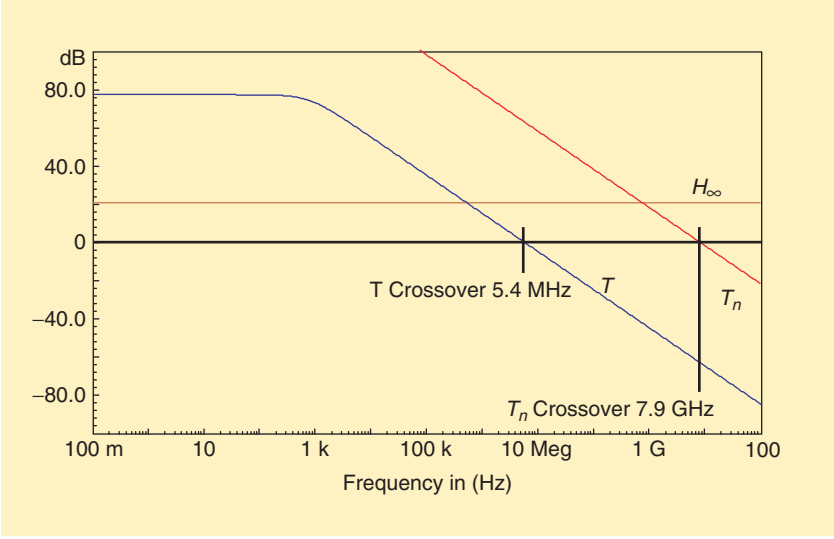

Figure 10. *The expectations are borne out: H_∞ is flat at 20 dB, and T has a single pole. The null loop gain T_n is not infinite because of nonzero reverse transmission through the feedback path (a feedforward path).*

A Simple Feedback Amplifier Example

A series-shunt feedback amplifier circuit model is shown in Figure 7. The forward path is a simplified model of a typical integrated circuit (IC) in which voltage gain is achieved in the first two stages, which may be differential, and current gain is achieved in the final Darlington follower stage. In this first example, the frequency response is determined by the sole capacitance C_c. Each active device is represented by a simple bipolar junction transistor (BJT) T-model, which has the advantage of also representing a field-effect transistor (FET) by setting the drain current equal to the source current, as is done in this example.

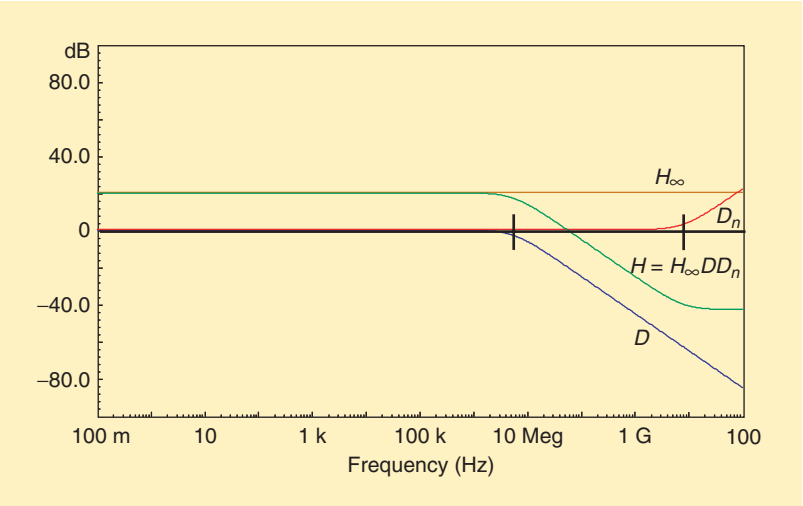

Figure 11. *T and T_n replaced by their corresponding discrepancy factors $D = T/(1 + T)$ and $D_n = (1 + T_n)/T_n$. The normal closed-loop gain $H = H_\infty DD_n$ differs from H_∞ not only because of D, but also because of D_n, although this effect is small.*

To apply the GFT, the crucial first step is to choose the test signal injection point that makes H_∞, T, and T_n have the desired interpretations of ideal closed-loop gain, loop gain, and null loop gain.

The error voltage is the voltage between the input and the fed back voltage at the feedback divider tap point, labeled v_y in Figure 7. The error current is the current drawn from the feedback divider tap point, labeled i_y in Figure 7. The test signals e_z and j_z are to be injected inside the loop so that v_x and i_x are the driving signals for the forward path, as shown in Figure 8. Thus, the test signal configuration meets the two conditions that injection occurs at the error-summing point, and is inside the loop, implementing the general model of Figure 5.

To invoke the GFT template, the appropriate dual-injection icon is selected and connected to provide the test signals e_z and j_z, as in Figure 9. The icon also provides the system input signal e_i and observes the output signal v_o, because it has to adjust the test signals relative to the input to establish various nulls, one of which is the output signal.

Another principle of D-OA is "figure out as much as you can about the answer before you plunge into the analysis."

In this case, we expect H_∞ to be $1/K$, the reciprocal of the feedback ratio that was initially chosen to meet the system specification, because the injection configuration was specifically set up to achieve this. Here, $1/K = (R_1 + R_{2)}/R_1 = 10 \Rightarrow 20$ dB, flat at all frequencies.

We expect T to be large at low frequencies and to have a single pole determined by C_c. Consequently, D will be flat at essentially 0 dB at low frequencies, with a pole at the crossover frequency of T, beyond which D will be the same as T.

We expect T_n to be noninfinite and, consequently, D_n to be not 0 dB, because there is nonzero reverse transmission through

the feedback path. That is, if the forward path through the active devices dies, the input signal e_i can still reach the output v_o by going through the feedback path in the "wrong" direction. The principal benefit of the GFT is to permit calculation of this effect, which is not accounted for in the conventional model, in order to determine whether or not it is significant.

The GFT results for the three second-level TFs for the model of Figure 9 are shown in Figure 10, and the expectations are indeed borne out. The results are repeated in Figure 11 with the loop gains replaced by their corresponding discrepancy factors, both of which are essentially 0 dB at low frequencies. Also shown is the final result for the first level TF H, the closed-loop gain, which from (18) is the direct superposition of the H_∞, D, and D_n graphs.

This final result shows that the bandwidth of H is determined by the T crossover frequency, as in the conventional approach, and that reverse transmission ("wrong way") through the feedback path does not have any significant effect until the much higher null loop gain crossover frequency.

A More Realistic Feedback Amplifier Model

The more interesting model of Figure 12 includes two added capacitances for each active device. This is a much more realistic model, and, of course, library device models can be substituted. What are our expectations for the results in comparison with those for Figure 9?

Since all the extra elements are capacitances, we expect the low-frequency properties to remain the same, but the dominant pole, and, hence, the loop gain crossover frequency would be lowered. Therefore, to enable a more meaningful comparison between the two circuits, C_c in Figure 12 has been reduced sufficiently to preserve the same loop gain crossover frequency. Nevertheless, the extra capacitances create more poles and zeros, so the high-frequency loop gain is expected to be more complicated.

The major consequence of the presence of the extra capacitances is that there is now a second feedforward path (through a string of capacitances), in addition to that through the feedback path in the "wrong" direction, through which the input signal can reach the output. Also, there is now nonzero reverse transmission through the forward path, which in turn creates a nonzero reverse loop gain. It is not necessary to separate these nonidealities, because they are all automatically accounted for in the calculation of the loop gain (usually little effect) and in the null loop gain (the major effect).

The quantitative results of the GFT template simulations for Figure 12 shown in Figures 13 and 14 bear out the expectations. The null loop gain crossover frequency is drastically lowered, and even though the magnitude of the null discrepancy factor

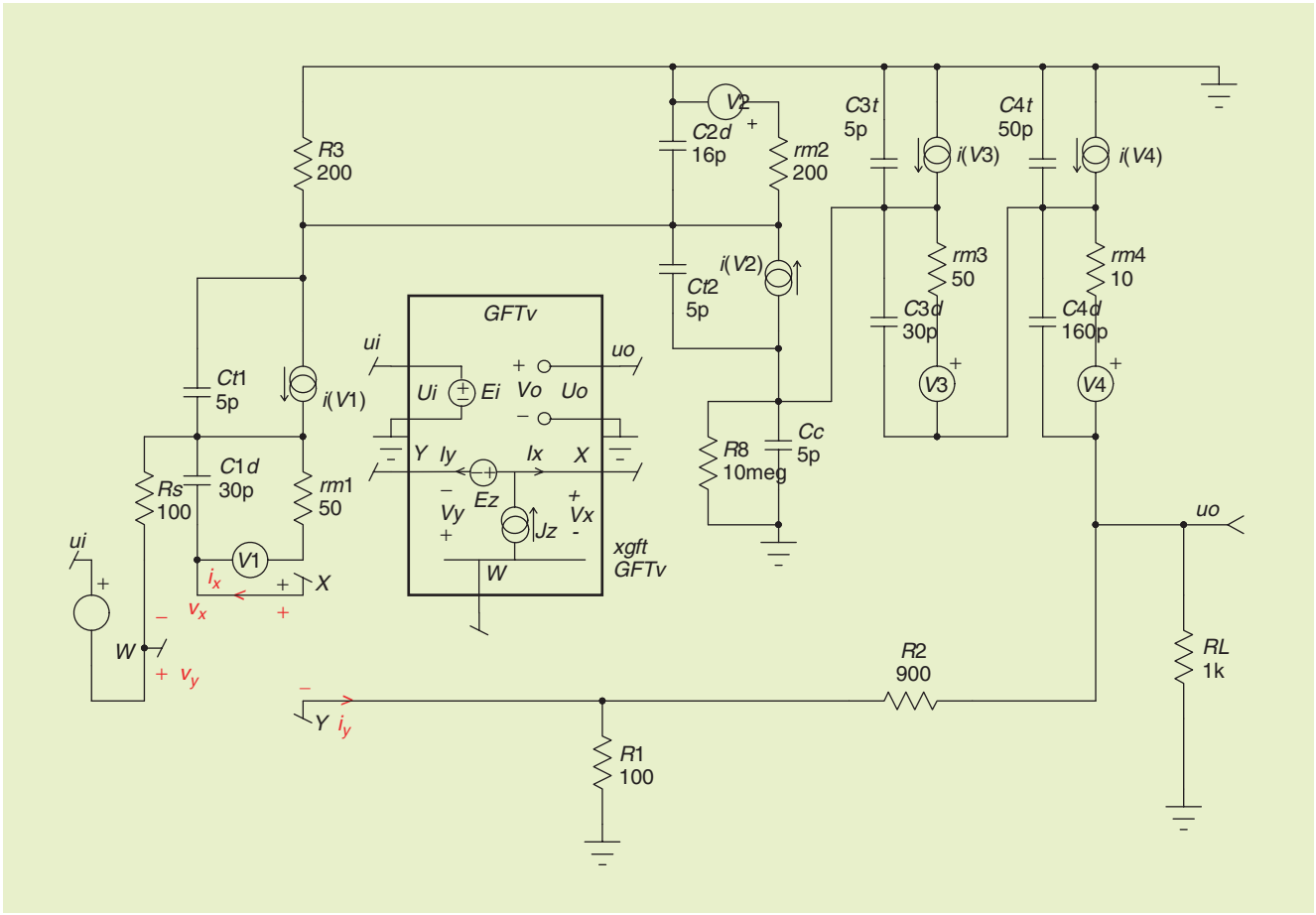

Figure 12. *A more realistic model than Figure 7, with two capacitances added per active device (library models, of course, could be substituted).*

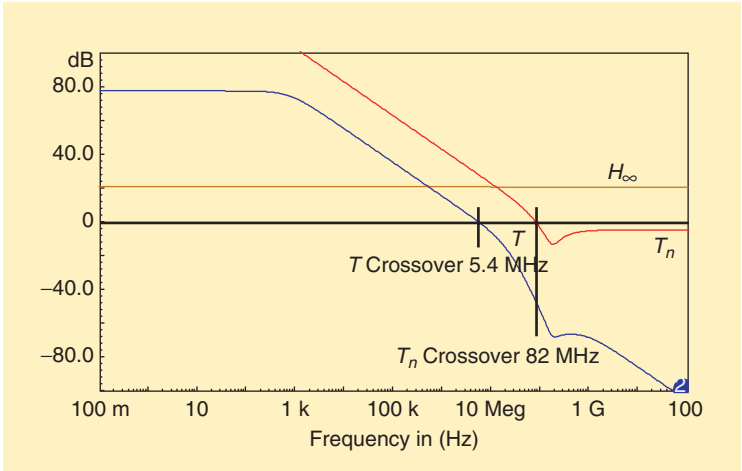

Figure 13. *There is now an additional feedforward path, nonzero reverse transmission through the forward path, and nonzero reverse loop gain, causing the null loop gain crossover frequency to be much lower.*

D_n is 0 dB at both ends of the frequency range, its phase undergoes a huge lag that is transferred directly into a correspondingly huge phase lag in the final closed-loop gain H.

Although the magnitude of H at high frequencies may not be of much interest in the frequency domain, its corresponding phase has a controlling effect in the time domain. The step responses of the circuits of Figures 9 and 12 are shown in Figure 15. The huge phase lag of H at high frequencies for the circuit of Figure 12 causes the expected delay in the step response; however, the ensuing rise time is *shorter* than for Figure 9, with the perhaps unexpected beneficial result that the final value is achieved *sooner* for Figure 12 than for Figure 9.

The bottom line is that the GFT of (28), whose principal difference from (6) of the conventional approach is the presence of the null discrepancy factor D_n, predicts a substantial modification of the closed-loop performance H. The nonidealities represented by T_n or D_n are *always present* in a realistic model of an electronic feedback system, and in at least some respects, can actually *improve* rather than degrade the performance. This rare exception to Murphy's law provides added incentive to utilize the GFT.

A method of finding loop gain from a voltage loop gain T_v and a current loop gain T_i calculated successively from single voltage and current injected test signals has been quite widely adopted since it was proposed in 1975. The formula is

$$\frac{1}{1+T} = \frac{1}{1+T_v} + \frac{1}{1+T_i} \text{ or } T = \frac{T_v T_i - 1}{2 + T_v + T_i}. \quad (20)$$

However, this formula was based on the conventional block diagram of Figure 1 and does not account for nonzero reverse loop gain.

You No Longer Need to Measure Loop Gain Directly

In the conventional approach, efforts are often made to measure loop gain on the actual hardware to check that the phase margin is adequate, although little or no thought is given to whether or not the measurement is consistent with the actual closed-loop gain. It is very awkward to inject even a single test signal into an IC, and dual or triple injection to set up ndi or dnti conditions is so burdensome that it is rarely attempted.

Fortunately, *it is no longer necessary to measure loop gain directly.* The GFT of (18) is exact with respect to the simulated model, and all you have to do is measure the final closed-loop TF H, which you would do anyway to check whether it meets the specification. If the simulated H differs from the measured H, you have to adjust the model until the two are the same. When this is achieved, you know the model is correct, and then the simulation tells you what T and T_n are individually. This is the culmination of the D-OA process.

More Useful Techniques for Analog Engineers

The GFT is completely general, the only requirement being that it applies to a linear system model. The symbol H has been used here for the first level TF purposely to avoid the connotation of "gain," because it could equally well represent input or output impedance, power supply rejection, or indeed *any* TF of interest.

It was mentioned earlier that the EET interpretation of the dissection theorem can be extended to any number of injected test signals, leading to the NEET theorem. The GFT interpretation could, likewise, be extended, in particular to two pairs of injected voltage and current test signals, which would open the door to analysis of feedback amplifiers containing both differential and common mode loops.

Analog, mixed-signal, and power supply design engineers are not the only ones to benefit from an ability to apply the powerful methods of D-OA. Those who review and verify designs of others also need to know how design-oriented results of analysis should be presented.

Therefore, managers, system integration engineers, and reliability engineers who evaluate the products of other companies as well as their own, also can significantly increase their effectiveness by applying the methods of D-OA.

Then, if you hold any of the above job titles, you can contribute meaningfully to design review discussions, instead of just saying to the presenting designer "Well, it looks as though it's coming along all right; carry on!" In fact, you can improve the effectiveness of the whole project by requiring that design engineers present their results according to the principles of D-OA.

For further information on the GFT, EET, and D-OA in general, see http://www.rdmiddlebrook.com.

For further information on the Intusoft ICAP/4 Circuit Simulator, including a GFT Template User's Manual, see http://www.intusoft.com.

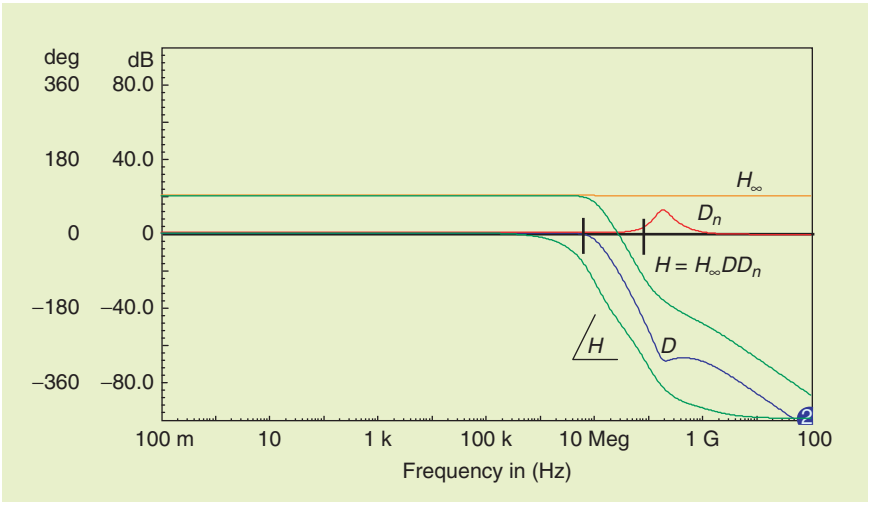

Figure 14. *The extra capacitances cause the null discrepancy factor D_n to be drastically different, resulting in a huge phase lag of* 450° *in the normal closed-loop gain H.*

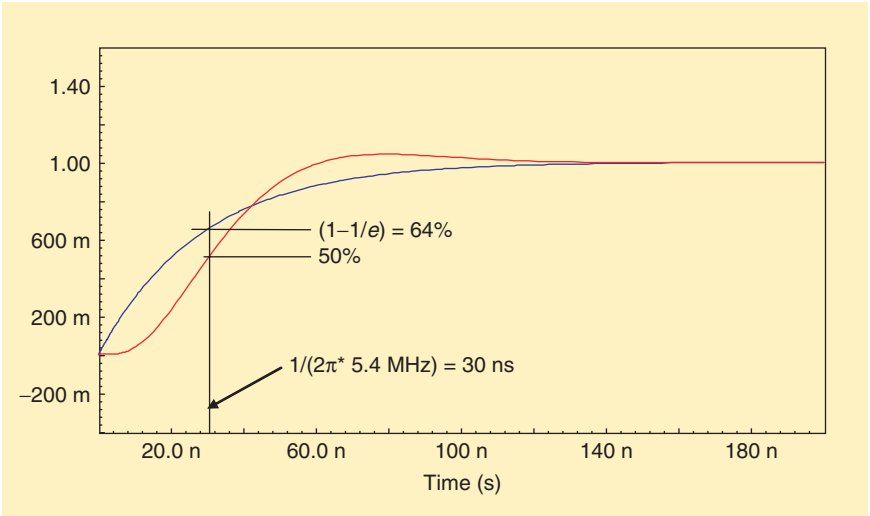

Figure 15. *For the circuit of Figure 12, the huge phase lag of H causes the expected delay in the step response; however, the ensuing rise time is* shorter, *with the perhaps unexpected beneficial result that the final value is achieved* sooner. *At least in some respects, nonidealities can actually* improve *performance!*