A Wideband Injection-Locking Scheme and Quadrature Phase Generation in 65-nm CMOS

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***Abstract*—A novel technique for wideband injection locking in an *LC* oscillator is proposed. Phased-lock-loop and injection-locking elements are combined symbiotically to achieve wide locking range while retaining the simplicity of the latter. This method does not require a phase frequency detector or a loop filter to achieve phase lock. A mathematical analysis of the system is presented and the expression for new locking range is derived. A locking range of 13.4–17.2 GHz and an average jitter tracking bandwidth of up to 400 MHz were measured in a high-*Q* *LC* oscillator. This architecture is used to generate quadrature phases from a single clock without any frequency division. It also provides high-frequency jitter filtering while retaining the low-frequency correlated jitter essential for forwarded clock receivers.**

***Index Terms*—Adler's equation, injection-locked oscillator (ILO), injection-locked (IL) phase-locked loop (PLL), jitter transfer function, locking range, quadrature, voltage-controlled oscillator (VCO).**

I. Introduction

INJECTION-LOCKED oscillators (ILOs) have been used in many wireline receivers because of their simple implementation and instantaneous locking characteristics. However, their application is hindered by their limited locking range compared with alternative techniques such as phase-locked loops (PLLs). Recent standards [1] require operation with data rates that span more than 10% of the nominal frequency. Therefore, transceivers must operate reliably over this range. A large locking range is also desirable to counter the inevitable PVT variations in modern scaled technologies.

Injection range of an *LC* ILO is inversely proportional to *Q* of the tank [2]. Thus, low-*Q* tanks have been used [3] to increase the locking range in an *LC* ILO, but this comes at the expense of higher power consumption, as shown in Fig. 1. Intricate frequency-tracking mechanism such as a reference PLL has also been used to set the oscillator's natural frequency so that it is within the injection range of the reference clock [4]. This adds additional design complexity and an area/power penalty to the otherwise simple circuit, thus offsetting the merits of the injection-locked (IL)-based system.

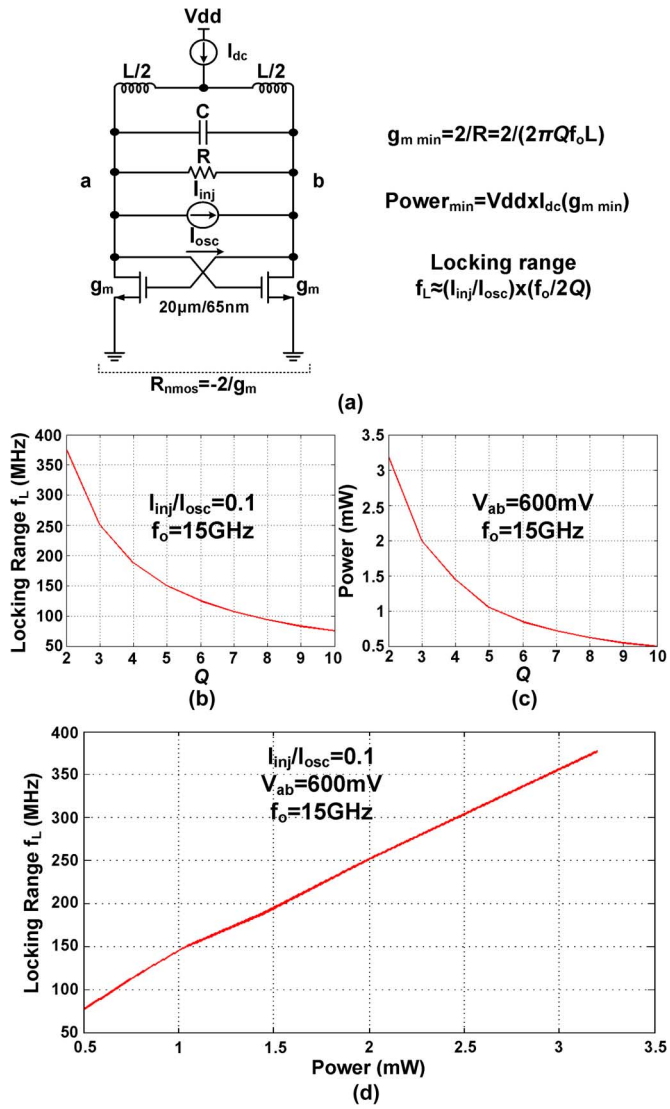

Fig. 1. (a) *LC* oscillator with injection. (b) Variation of locking range with *Q* for a constant injection strength of 0.1. (b) Variation of power consumption with *Q* for a constant oscillation amplitude of 600 mV. (d) Improvement in locking range versus power consumption for a constant injection strength and oscillation amplitude (simulation).

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Another important requirement of wireline receivers that employ half- and quarter-rate architectures is generation of accurate quadrature phases. Injection-locked *LC* dividers have been frequently used for generating quadrature phases [5], but they require complementary clocks at twice the desired frequency, which tends to be power inefficient. Quadrature phase generation from a single phase of clock without any frequency division

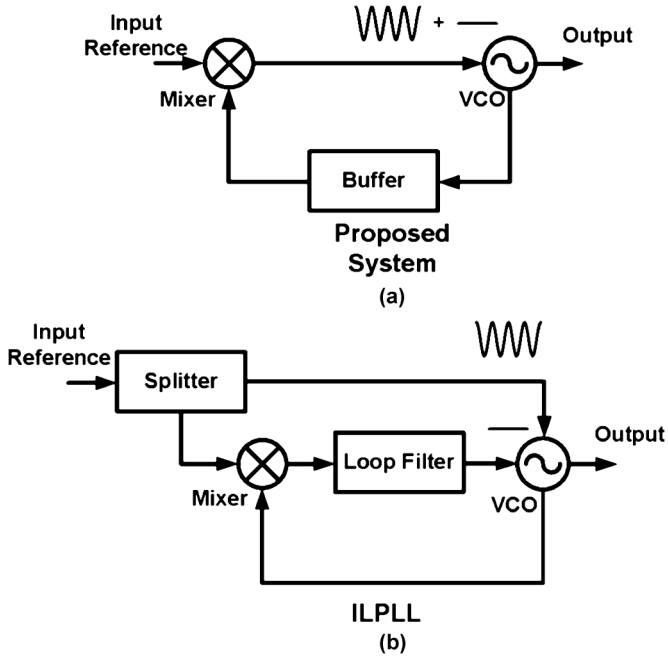

Fig. 2. Block diagram of: (a) proposed system and (b) ILPLL.

is highly desirable for half- and quarter-rate clock and data recovery (CDR) architectures.

In this paper, we propose a method for wideband injection locking in an *LC* oscillator that maintains the simplicity of an IL system. We also describe an extension of this method to produce quadrature phases from a single reference clock without any frequency division. The system has a wide jitter tracking bandwidth (JTB), which makes it useful for forwarded clock receivers [6].

This paper is organized as follows. Section II describes the system architecture. Section III presents a mathematical analysis describing the dynamics of the system. Measurement results are presented in Section IV. Finally, Section V summarizes our work by presenting conclusions.

II. System Architecture

Fig. 2(a) shows the simplified block diagram of the proposed system. It consists of three basic elements, namely, a voltage-controlled oscillator (VCO), mixer, and buffer. The buffered VCO output is mixed with the input reference and the resultant signal is fed back to the VCO to complete the feedback architecture.

A. Comparison With Injection-Locked Phased-Locked Loop (ILPLL)

In the locked state, an ILO can be modeled as a first-order PLL [7]. A first-order PLL is comprised of a VCO, mixer, and low-pass filter. In this work, we propose to eliminate the loop filter altogether. The resultant high-frequency component of the mixer is used to perform injection locking. This is different from an ILPLL structure [see Fig. 2(b)], which consists of a full PLL with additional injection in the VCO to improve its phase-noise characteristics. Additionally, unlike the ILPLL, both IL and PLL actions are performed at the same node using common-mode injection in the varactors.

B. Common-Mode Injection

In most *LC* oscillators, the control voltage of the varactor is used to set the frequency of oscillation, f_o. In such architectures, the instantaneous voltage oscillation at the output node results in transient changes in the capacitance (Fig. 3). Due to this effect, the voltage of the common-node A has an extra frequency component at $2f_o$ [8]. Similarly, if we inject a $2f_o$ component at the varactors' common node, then the mixing action of the varactors will inject a current at f_o into the tank. However, such a circuit will constitute a frequency divider, which is not desirable in many applications. We will describe the basic principles of the proposed architecture that avoids such division and provides a very wide locking range.

C. Implementation Details

Fig. 3 shows the basic schematic of the proposed wideband injection-locking system. A complementary transmission gate is used as a single balanced passive mixer. The output of the *LC* oscillator is buffered by the current mode logic (CML) to CMOS stage. The transmission gate is driven by the outputs of the buffer and the reference clock is used as the input. The output of the transmission gate is directly fed to the varactors in the *LC* oscillator thereby completing the loop.

D. System Analysis in Locked State

In the locked state, the output of the transmission gate contains a high-frequency $2f$ component and a dc component. The value of the dc component is determined by the phase difference between the reference and the buffer output (α) is proportional to $\cos(\alpha)$ [see Fig. 4(d)]. The phase difference between the oscillator output and the injected clock (θ) is given by [2]

$$\sin(\theta) = \frac{(\omega_o - \omega_{\rm inj})}{\omega_L}. \tag{1}$$

Assuming a constant delay Δ_o through the CML to CMOS buffer, the phase difference between the clock and buffer output α is given by

$$\alpha = \theta + \Delta_o \times (2\pi f_{\rm inj}). \tag{2}$$

Thus, the dc component of the switch output is dependent on θ. In the unlocked state, the dc component brings the f_o close to $f_{\rm inj}$ (PLL action) and the $2f_{\rm inj}$ component performs the injection lock. Thus, the phase difference θ becomes dependent on reference frequency, which enables wideband locking. Fig. 4(e) shows the simulated varactor control voltages under locked condition for two frequencies (14 and 16.5 GHz). The dc levels are different and are overridden by the corresponding $2f_{\rm inj}$ components.

Fig. 4(a) shows the simulated oscillator output phase difference (θ) versus input frequency. θ is smaller at lower frequencies and it increases as frequency increases. This is in accordance with the dc characteristic of the transmission gate [see Fig. 4(d)] and phase difference between the CML to CMOS output and the reference clock (α). The fact that CML to CMOS

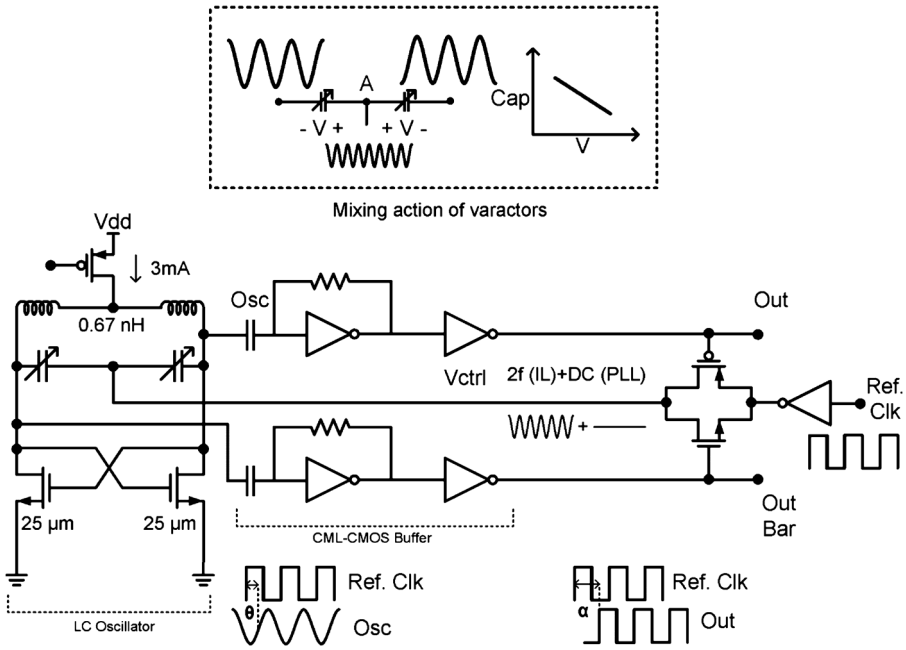

Fig. 3. Schematic of the proposed system. The input to the common mode of the varactors contains $2f$ and dc components. The dc component brings the natural frequency close to the frequency of the reference clock and the $2f$ component does the injection lock.

buffers add a constant delay across all frequencies helps increase the injection range as it amplifies the phase shift when frequency increases (2). This helps the switch output to cover the entire voltage range (0-Vdd), as shown in Fig. 4(d).

It is important to clarify that the proposed work achieves wider locking range due to the PLL like loop, which brings the center frequency of the oscillator within the injection range automatically. The inherent properties of a VCO-only system like injection range and JTB remain intact and are still a function of the Q of the oscillator. Our unique methodology alleviates the need of using a loop filter so that system can have a high JTB.

E. Quadrature Phase Generation

For quadrature phase generation, a secondary matched *LC* oscillator is coupled to the primary in a quadrature VCO (QVCO) configuration. Fig. 5 shows the schematic of quadrature phase generation circuit. Antiphase coupling is achieved using pMOS differential pairs. The strength of the coupling is controlled by varying the tail current of the pMOS differential pair. A coupling factor of above 25% was used to provide sufficient oscillation reliability [9].

The control voltage of the secondary is generated from the output of the transmission gate after sending it through a passive low-pass filter, consisting of two *RC* sections in series with $R = 1$ kΩ and $C = 80$ fF. A passive filter is chosen to reduce power consumption and values of *RC* are chosen to have a 3-dB bandwidth of 1 GHz, which provides more than 50 dB of attenuation to the $2f$ component and allows the dc component to pass through. This has two effects. Firstly, it allows both oscillators to have the same f_o, and secondly, it ensures that there is no coupling between them through the varactors' common mode. A two-stage *RC* section is chosen for more efficient isolation as it provides sharper (-40 dB/dec) attenuation without slowing down the feedback loop as the 3-dB bandwidth does not need to be too small. This isolation is important for generating accurate quadrature phases as it ensures that coupling between primary and secondary oscillators is solely antiphase through the pMOS differential pairs and there is no in-phase coupling through the varactors. If not attenuated, in-phase coupling would force the phases of the oscillators to be aligned.

ILOs have been frequently used for clock de-skewing applications [3]. Equation (1) suggests that the phase of the output clock can be varied by changing the f_o of the oscillator. In our architecture, the phase of the replica oscillator can be adjusted by changing the bias of secondary varactors VarA and VarB, which are chosen to be more than seven times smaller than the main varactors (Fig. 5). Secondary varactors are controlled externally and are not a part of the loop. Thus, sizing of the secondary varactors present a tradeoff between the de-skew range and locking range. Sizes of the secondary varactors were kept much smaller than primary varactors so that the locking range is minimally altered. To provide sufficient de-skew, the control voltages of VarA and VarB were altered in the opposite direction. This phase controllability is also imperative for clock receiver application where exact quadrature phases may not be required due to polarized-mode dispersion effects [10].

III. Mathematical Analysis

In this section, we propose a mathematical model of our system and derive the new effective locking range. To simplify the analysis, we delink IL and PLL aspects of our design. Fig. 6 shows both IL and PLL characteristics. Injection is modeled as an additive input. The output tracks the input (ω_{inj}), except for a phase difference θ, which may be time varying. The PLL part of the system consists of a mixer with a gain of γ and a constant delay of Δ_o. The mixer has inputs from the reference clock and the delayed version of the *LC* oscillator output. The output of the mixer goes to the common mode of the varactors, which,

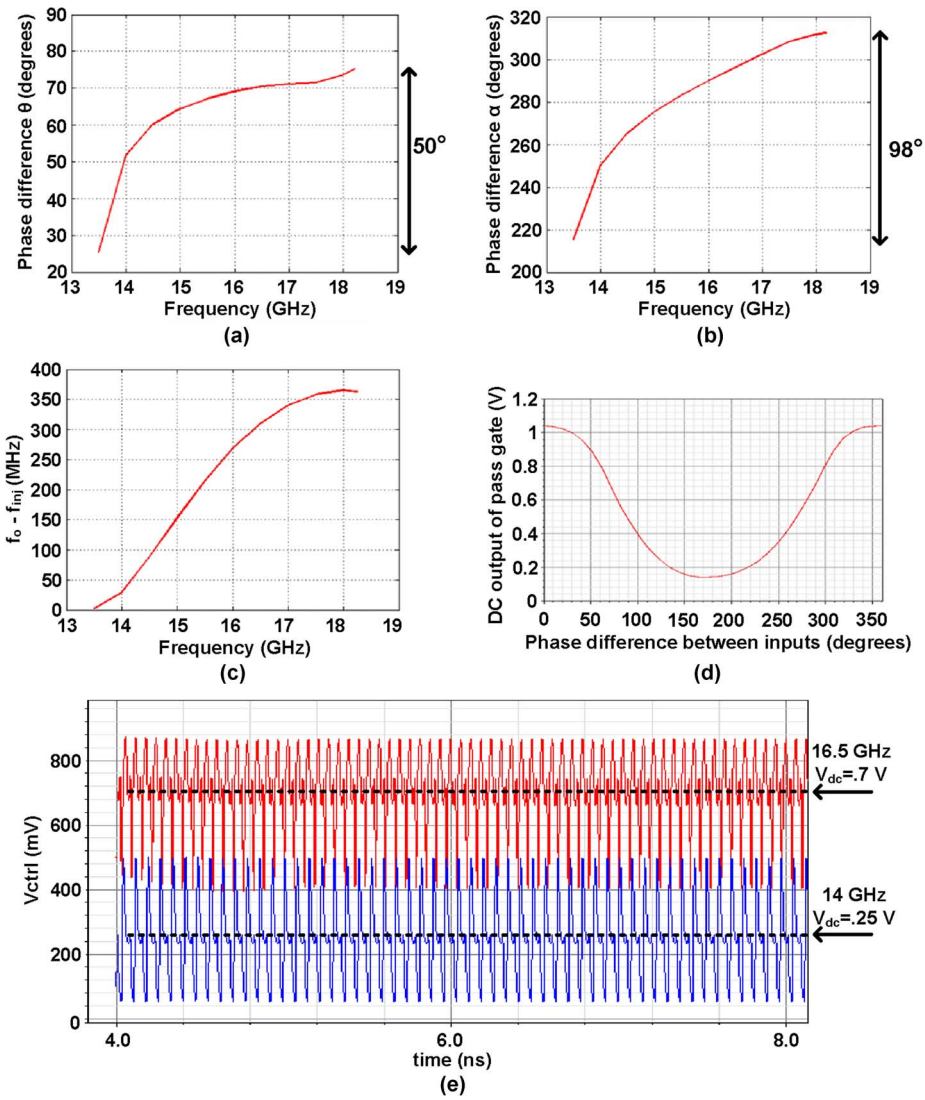

Fig. 4. Simulation results. (a) θ versus ref. frequency. (b) α versus ref. frequency. (c) $f_o - f_{\rm inj}$ versus ref. frequency, (d) DC characteristic of the transmission gate. (e) Vctrl at 14- and 16.5-GHz clock reference.

through its mixing action, converts it to equivalent injection at $\omega_{\rm inj}$.

The injection-locking dynamics for weak injection $V_{\rm osc} \gg V_{\rm inj}$ is governed by the famous Adler's equation [11]

$$\frac{d\theta}{dt} = \omega_o - \omega_{\rm inj} - \omega_L \sin(\theta). \tag{3}$$

Here, ω_L is the locking range defined as

$$\omega_L = \frac{\omega_o}{2Q} \times \frac{V_{\rm inj}}{V_{\rm osc}}. \tag{4}$$

To take into account the PLL action, we replace ω_o by $\omega_o + K_{\rm vco} * {\rm V}_{\rm ctrl}$

$$\frac{d\theta}{dt} = \omega_o + K_{\rm vco} V_{\rm ctrl} - \omega_{\rm inj} - \omega_L \sin(\theta) \tag{5}$$

where

$$V_{\rm ctrl} = \gamma V \cos(\alpha) + \gamma V \cos(2\omega_{\rm inj} t + \alpha). \tag{6}$$

However, we have already taken the $2\omega_{\rm inj}$ component into account in the form of injection so we are left with

$$\frac{d\theta}{dt} = \omega_o + K_{{\rm vco}\gamma} \cos(\theta + \omega_{\rm inj}\Delta_o) - \omega_{\rm inj} - \omega_L \sin(\theta). \tag{7}$$

To make (7) comparable to the Adler's equation, we modify it to have only a single sinusoid

$$\frac{d\theta}{dt} = \omega_o - \omega_{\rm inj} - [\{\omega_L + K_{{\rm vco}\gamma} \sin(\omega_{\rm inj}\Delta_o)\} \sin(\theta) - K_{{\rm vco}\gamma} \cos(\theta) \cos(\omega_{\rm inj}\Delta_o)] \tag{8}$$

where

$$K_{{\rm vco}\gamma} = K_{\rm vco}\gamma V \text{ and } \alpha = \theta + \omega_{\rm inj}\Delta_o. \tag{9}$$

We therefore have

$$\begin{aligned}\frac{d\theta}{dt} &= \omega_o - \omega_{\rm inj} - \omega_{L{\rm new}} \{\sin(\theta)\cos(\varnothing) - \sin(\varnothing)\cos(\theta)\} \\ &= \omega_o - \omega_{\rm inj} - \omega_{L{\rm new}} (\sin(\theta - \varnothing)).\end{aligned} \tag{10}$$

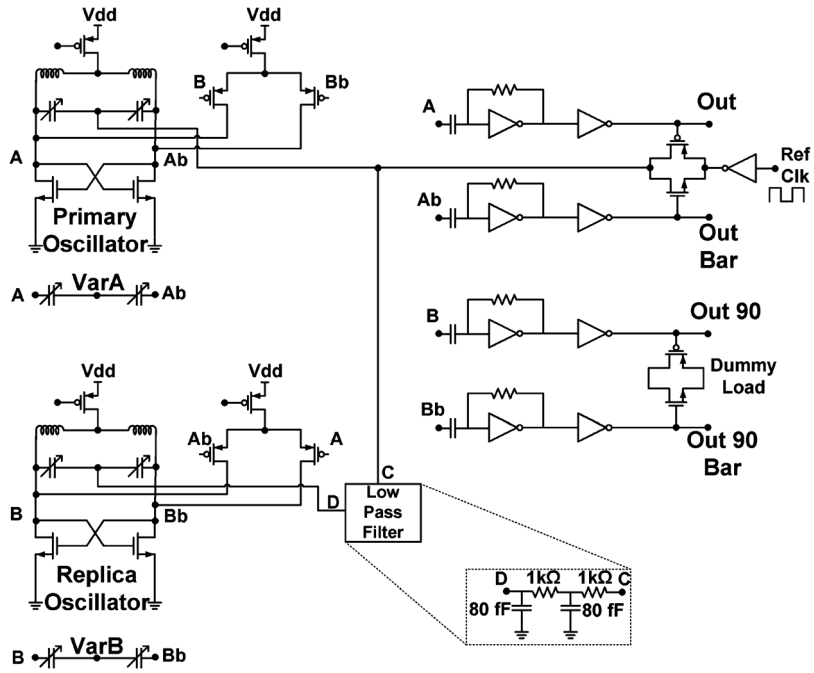

Fig. 5. Schematic of the proposed system for quadrature phase generation.

Defining

$$\tan(\varnothing) = \frac{K_{\text{vco}\gamma}\cos(\omega_{\text{inj}}\Delta_o)}{\omega_L + K_{\text{vco}\gamma}\sin(\omega_{\text{inj}}\Delta_o)} \tag{11}$$

$$\omega_{L\text{new}} = \sqrt{K_{\text{vco}\gamma}^2 + \omega_L^2 + 2\omega_L K_{\text{vco}\gamma}\sin(\omega_{\text{inj}}\Delta_o)}. \tag{12}$$

In the locked state $(d\theta/dt) = 0$, thus for a real solution,

$$\left|\frac{\omega_o - \omega_{\text{inj}}}{\omega_{L\text{new}}}\right| = |\sin(\theta - \varnothing)| \leq 1 \tag{13}$$

$$|\omega_o - \omega_{\text{inj}}| \leq |\omega_{L\text{new}}|. \tag{14}$$

Thus, the new effective locking range is $\omega_{L\text{new}}$. It can be inferred from (12) that for all values of Δ_o such that

$$\Delta_o < \frac{\pi}{\omega_{\text{inj}}}. \tag{15}$$

$\omega_{L\text{new}}$ will be greater than ω_L, and hence, the improvement in the locking range. For a maximum reference frequency of 18 GHz, the upper limit of Δ_o is 27.7 ps.

Fig. 7(a) shows a plot of the new locking range $f_{L\text{new}}$ and the regular locking range f_L based on (12) and (4), respectively. It predicts an average new locking range of 1.8 GHz, which is a $9\times$ improvement over that of a regular injection-locked LC oscillator. To further examine the system, a simulink-based behavioral model was designed. Using the same, transient solutions to (3) and (7) were calculated for the case when the oscillator natural frequency (f_o) was 13 GHz and injected frequency (f_{inj}) was 14.8 GHz. Fig. 7(b) clearly shows that our proposed system locks to the injected frequency because of its extended locking range whereas the regular ILO fails to do so as the injected frequency is well beyond its locking range.

Spectre-based simulations reveal a single-sided locking range $(f_{L\text{new}})$ of 1.7, 1.8, and 2.1 GHz for the reference frequencies 13, 15, and 17 GHz, respectively. Comparing the simulation results with the predictions of our mathematical model [see Fig. 7(a)] reveals a locking range mismatch of -0.1, 0, and 0.3 GHz at 13, 15, and 17 GHz, respectively. Mismatch can be attributed to the fact that the simple mathematical model does not take into account the variation of parameters like K_{vco} and Q with frequency.

Fig. 8 shows the behavior of $f_{L\text{new}}$ with variation in Δ_o. Initially $f_{L\text{new}}$ increases as Δ_o increases, but as Δ_o increases to 30 ps, $f_{L\text{new}}$ starts decreasing. This clearly shows that there is an optimum Δ_o for maximum locking range. We choose Δ_o to be 20 ps to maximize the locking range.

Equation (10) suggests the dynamics of the proposed system is similar to that of the injection locked of a VCO only system, as described by the Adler's equation (3). JTB of a simple ILO is proportional to its locking range (ω_L), as derived in [3],

$$\text{BW} = \omega_L \frac{K + \cos(\theta)}{(1 + K\cos(\theta))^2} \tag{16}$$

where K is the injection strength.

Thus, the proposed system has a similar jitter transfer function as that of the usual ILO, i.e., a first-order PLL [7]. However, due to its larger locking range $(\omega_{L\text{new}})$, it has a higher tracking bandwidth than a conventional ILO for a given Q and injection strength (16). The jitter from the incident signal is filtered by the low-pass characteristic of the noise transfer function, and the output signal tracks the phase variations of the incident signal within the loop bandwidth. Measured results for jitter transfer show a first-order behavior with -20-dB/dec attenuation [see Fig. 11(a)].

The phase of the oscillator is fixed for a given frequency, as shown in Fig. 4(a). However, phase of the replica oscillator can be changed by controlling bias of the secondary varactors VarA and VarB. The replica oscillator is not a part of the feedback

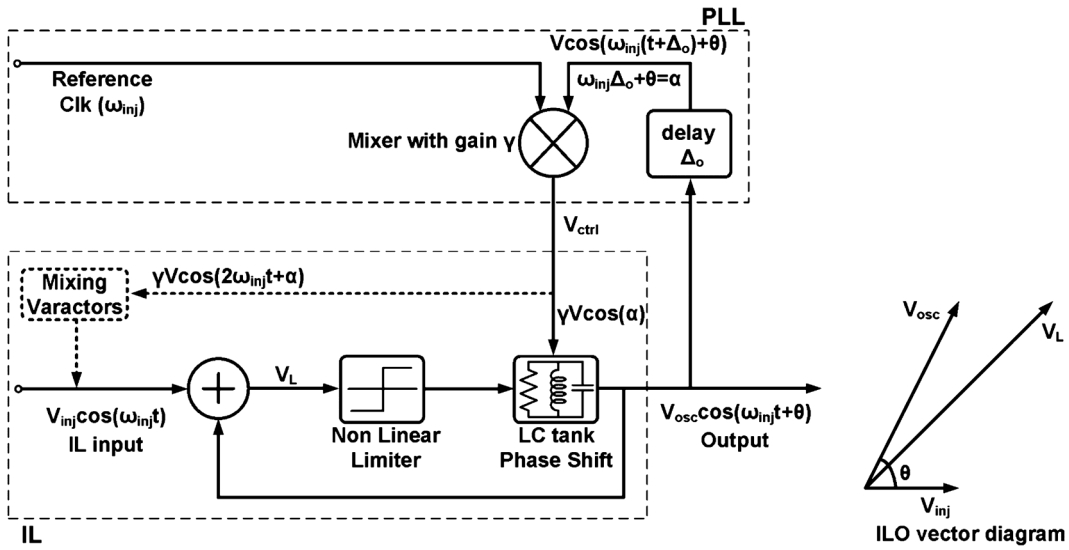

Fig. 6. System-level block diagrams showing injection and PLL feedbacks.

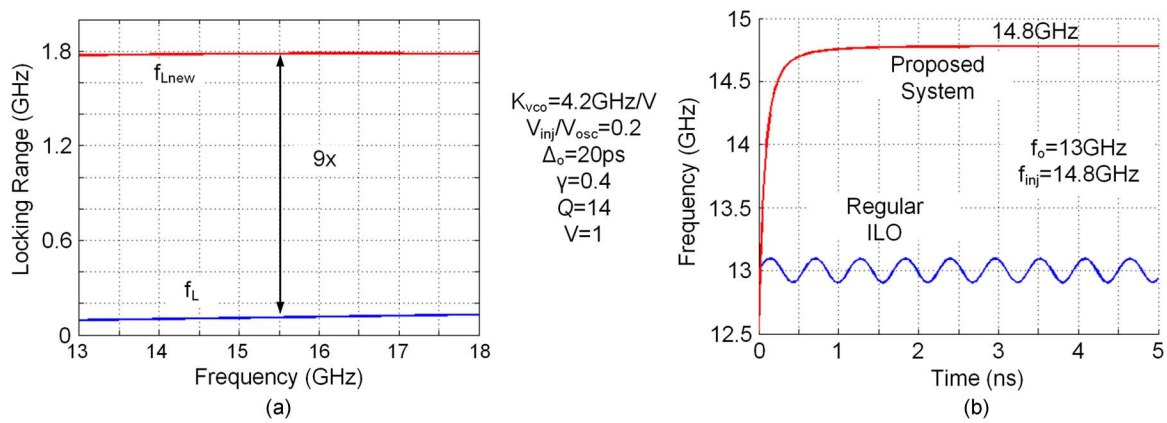

Fig. 7. (a) New locking range $f_{L\mathrm{new}}$ and regular locking range f_L. (b) Transient solutions to proposed system (7) and regular ILO (3).

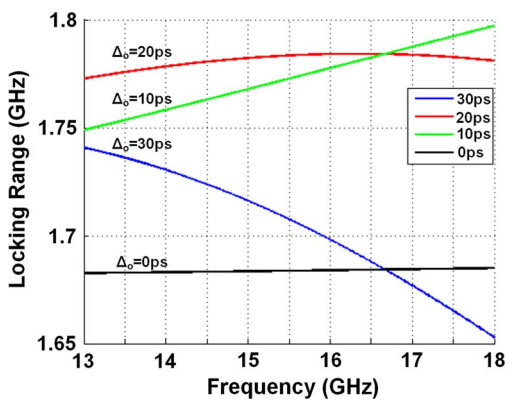

Fig. 8. Variation of $f_{L\mathrm{new}}$ with Δ_o.

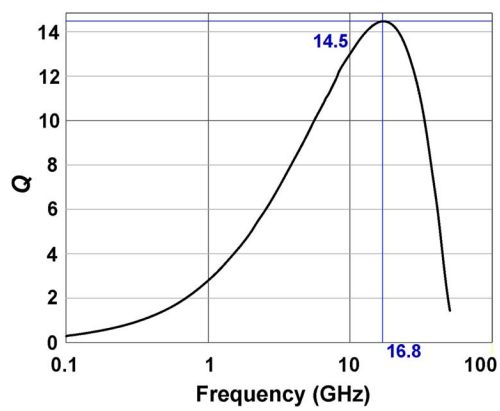

Fig. 9. Simulated frequency behavior of Q of the inductor.

loop, hence the de-skew relationship is described by (1). This would suggest a total de-skew range of 180°. However, measured results show an average de-skew range of 140° (Fig. 14). This is due to the size of the secondary varactors, which are not large enough to change the natural frequency of the oscillator for a full 180° phase shift.

IV. Measurement Results

A prototype has been designed and fabricated in 65-nm CMOS technology with a 1-V supply voltage. nMOS transistors in accumulation mode were used to implement the varactors with control voltage applied to the drain/source.

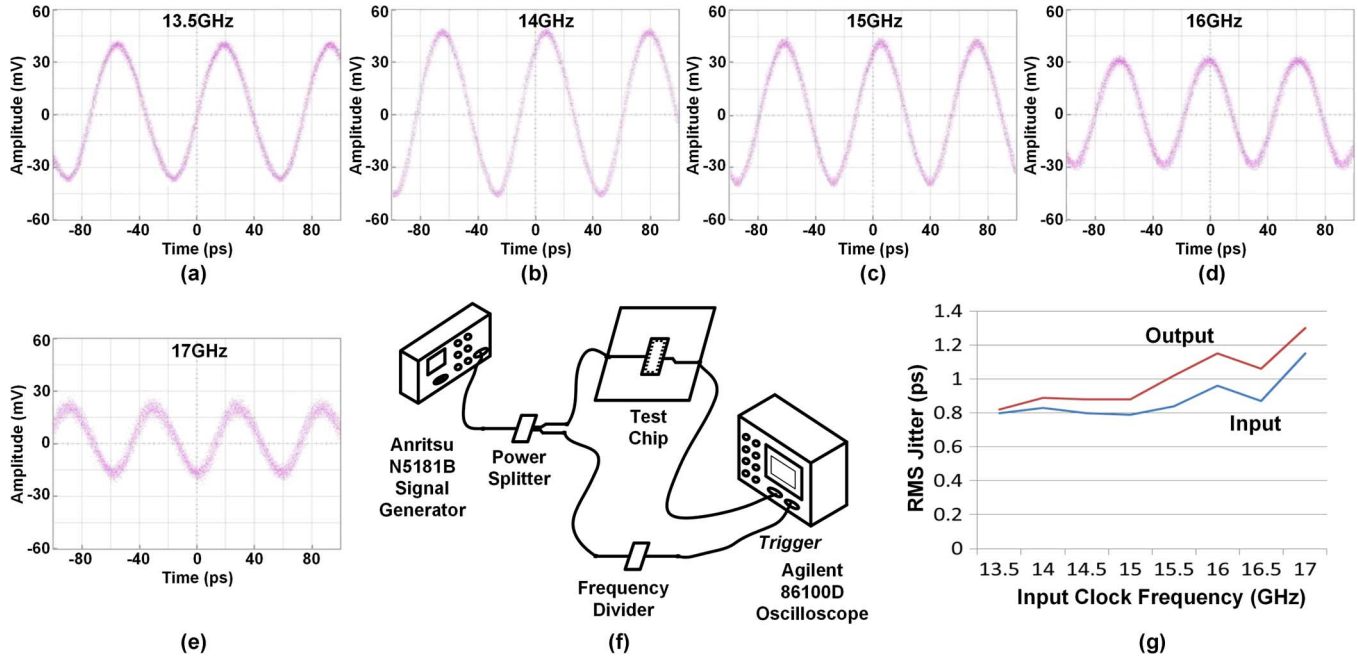

Fig. 10. (a)–(e) Measured locked output signals at several reference frequencies. (f) Setup for locking range and rms jitter measurement. (g) Measured input and uutput jitter at different reference frequencies.

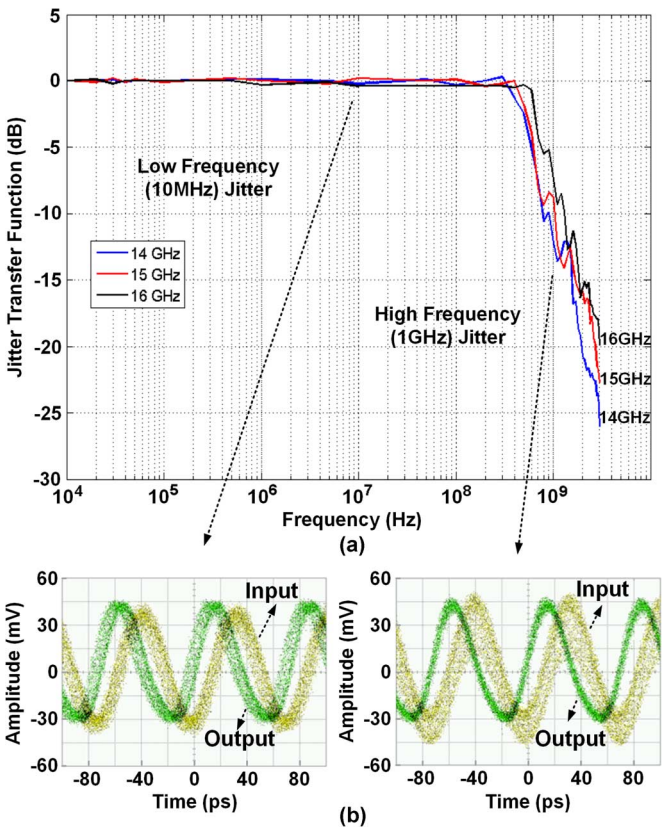

Fig. 11. (a) Measured jitter transfer function for 14-, 15-, and 16-GHz reference frequencies. (b) Response to low-frequency (10 MHz) and high-frequency (1 GHz) jitter.

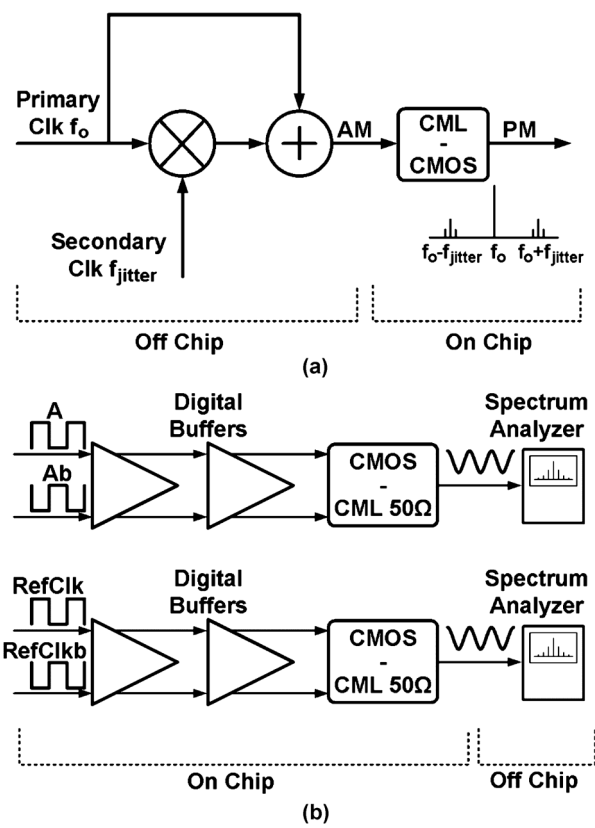

Fig. 12. (a) Measurement setup for generating PM signal reference. (b) Setup for measuring the spectrum of reference and output signals.

Spiral inductors of value 0.67 nH were designed to have simulated Q of over 14 in the frequency range of interest (Fig. 9). They were constructed using thick top two metal layers with added ground mesh for Q enhancement. The die micrograph (Fig. 15) shows their octagonal structure sized 110×110 μm^2 each. A high-Q design was chosen to substantiate the efficacy

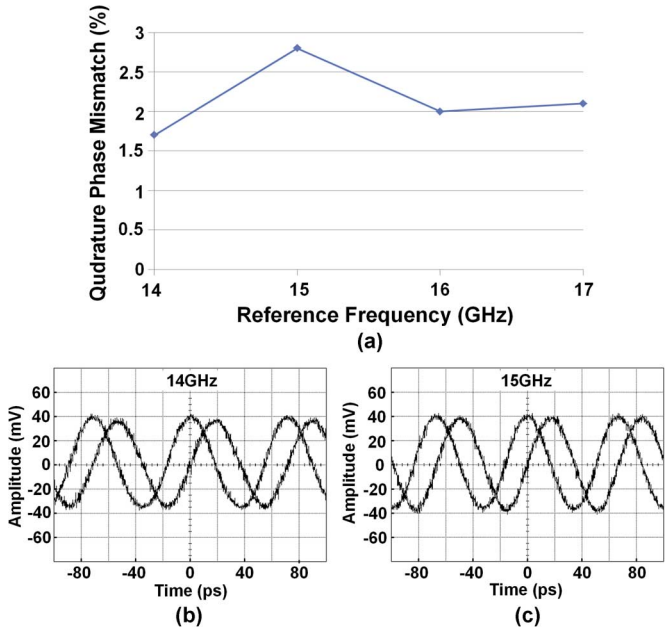

Fig. 13. (a) Measured percentage quadrature phase error versus reference frequency. (b) Measured quadrature phase waveforms at 14 GHz. (c) Measured quadrature phase waveforms at 15 GHz.

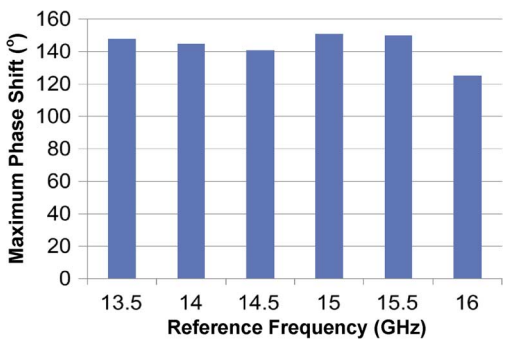

Fig. 14. Measured maximum phase shift of the replica oscillator at different reference frequencies.

of the proposed locking range extension technique as the injection-locking range is inversely proportional to Q in standard ILOs [2].

The key ILO parameters based on design methodology and simulation results are described in Fig. 7.

A. Locking Range and Root Mean Square (rms) Jitter

In our measurement setup [see Fig. 10(f)], an external signal generator is used to provide the reference clock used for injection. The frequency of the reference clock was varied and output waveforms were observed on a sampling oscilloscope [see Fig. 10(a)–(e)]. A locking range of 13.4–17.2 GHz was measured, which translates to 24.8% around the center frequency. The achieved locking range is limited by the varactor tuning range. The power consumption depends on the frequency of operation and varied between 8.5–9.5 mW going from low to high frequencies. For comparison, a previous design [3] uses a low-Q (2.5) inductor to achieve a maximum locking range of 12% with strong injection while consuming 13.1 mW for a single injection-locked LC oscillator.

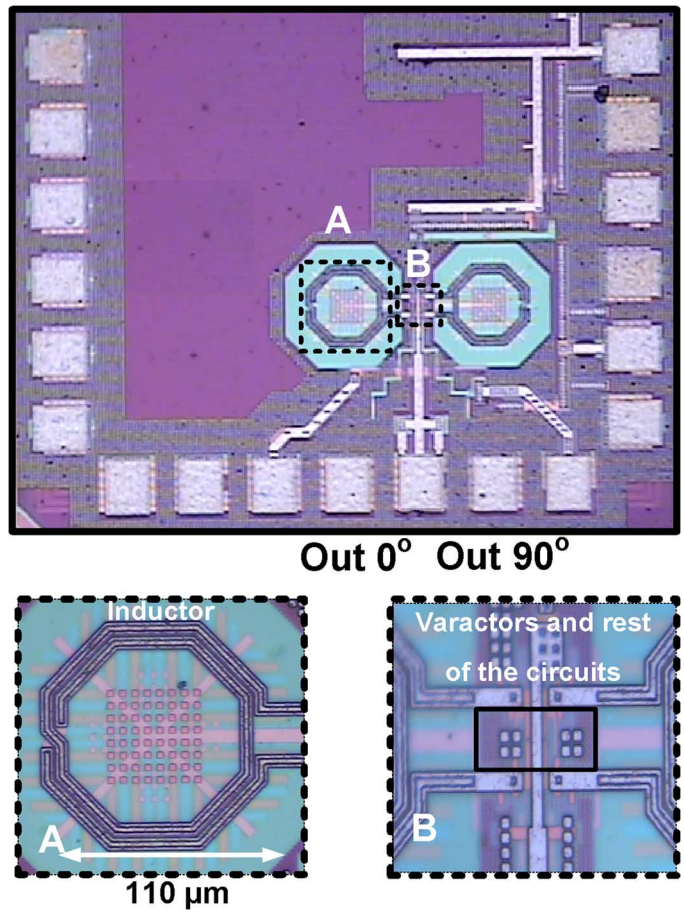

Fig. 15. Die micrograph. A: Details of the high-Q inductor. B: Placement of the varactors.

The rms jitter of the reference and the output waveforms were also measured across several frequencies in the locking range and are plotted in Fig. 10(g). A maximum rms jitter addition of 0.15 ps is observed at 17 GHz, which is expected considering that the system output goes through several buffers to drive the output stage.

B. Jitter Transfer Function

The jitter transfer function was measured using the test setup shown in Fig. 12. In this setup, a secondary clock $(f_{\rm jitter})$ was mixed with the primary clock (f_o) to generate an amplitude-modulated (AM) signal. This signal was transformed to a phase-modulated (PM) signal by on-chip CML-CMOS converters. The PM signal was used as the new reference clock. The secondary clock frequency $(f_{\rm jiiter})$ was varied from 10 MHz to 2 GHz for each f_o and the spectrum components of the output and the reference were measured at the carrier (f_o) and sideband $(f_{\rm jitter})$ frequencies [see Fig. 12(b)] using a spectrum analyzer.

Measurements were made [see Fig. 11(a)] for three reference frequencies (14, 15, and 16 GHz), and an average JTB of 400 MHz was recorded. High JTB helps in retaining the low-frequency jitter while eliminating high-frequency jitter, as depicted in Fig. 11(b). It is important to retain the low-frequency jitter in forwarded clock receivers as low-frequency jitter is correlated with the data [6].

TABLE I
PERFORMANCE COMPARISON

	This work	[3]	[5]	[6]	[14]
Injection architecture	PLL aided ILO	ILO	IL Divider	MILO-ILO	PILO
Oscillator architecture	LC	LC	LC	CMOS Ring	LC
Process technology	65nm CMOS	45nm CMOS	90nm CMOS	65nm CMOS	130nm CMOS
Injection range	24.8% (13.4GHz - 17.2GHz)	12% (12.6GHz - 14.3GHz)	18.1 %	—	—
RMS jitter	0.82 ps (at 13.5 GHz)	1.4 ps (at 13.5 GHz)	—	1.4 ps (at 3.2 GHz)	0.13 ps (at 3.2 GHz)
Average jitter tracking BW	400 MHz	200 – 700MHz	—	25 – 300MHz	—
Active area	0.3 x 0.11 mm^2	0.15 mm^2	0.33 x 0.08mm^2	0.03 mm^2	0.4 mm^2
Supply voltage	1 V	1.1 V	1.2 V	1 V	—
Average power consumption	9 mW (LC oscillators 65 % and buffers 35 %)	13.1 mW (for a single LC osc.)	6.4 mW	6.8 mW (for entire transmitter)	28.6 mW (single LC oscillator)
Average de-skew	140°	160°	NA	400°	—
Quadrature phase error	2.8% from 90° at 15GHz	NA	90° ± 1.8°	—	NA

C. Quadrature Accuracy and De-Skew

Quadrature phase accuracy was confirmed by measuring the phase difference between the outputs of the two oscillators after careful calibration of the measurement setup. A maximum offset of 2.8% (from 90°) is observed between the two phases at 15 GHz [see Fig. 13(a)]. Bias to VarA and VarB (Fig. 5) were fixed while making quadrature accuracy measurements. They were then varied from 0-Vdd to measure the maximum phase shift of the replica oscillator (Fig. 14).

Table I compares the performance of the proposed system with similar works.

V. CONCLUSION

A new locking scheme for extended injection range in an *LC* oscillator was introduced and analyzed. The dynamics of the system were derived and the new locking range was proven to be better than that of a conventional ILO. The system requires only a single clock phase for operation. Quadrature phase generation was demonstrated by adding a secondary coupled oscillator to the system. This wide locking range of the proposed system eliminates the need for center-frequency adjustment.

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