How tunneling currents *reduce* plasma-induced charging

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As semiconductor manufacturing moves towards smaller logic devices and thinner gate oxides, there is serious concern that pattern-dependent charging during plasma etching will impede progress by distorting etch profiles and by causing oxide breakdown. Simulations of the final overetch predict that the use of ultrathin oxides ($\leqslant 5$ nm), combined with a low substrate potential, will actually eliminate notching by enabling electron tunneling from the substrate to decrease surface charging potentials at the bottom of high aspect ratio trenches. Comparison with published experimental results validates the simulations. © *1997 American Institute of Physics.* [S0003-6951(97)03246-4]

Plasma-induced charging damage represents one of the most formidable issues to challenge plasma etching in the quest for smaller logic devices. It manifests itself in two forms: (a) the ''notching'' effect,[1] which appears as a wedge-like sidewall profile irregularity (Fig. 1), and (b) the ''electron shading'' effect,[2] which describes the electrical degradation of gate oxides by tunneling currents that flow during etching. Conflicting reports on when and how charging damage occurs abound in the literature,[3] hampering the empirical approach to solving the problem. Understanding the physics of charging is crucial for developing the predictive capabilities required to alleviate charging damage.

Notching is a result of differential microstructure charging brought about by the directionality difference between ions (anisotropic) and electrons (isotropic) at the wafer.[2,4,5] In high aspect ratio trenches, for example, the upper mask sidewalls charge up negatively, while the SiO_2 surface at the trench bottom charges up positively. The repulsive entrance potential reduces the flux of electrons to the trench bottom, thus forcing the SiO_2 surface potential to increase, until enough ions are deflected so that the ion and electron fluxes are balanced.[4,5] Since the potential of the edge gate can be maintained low by electrons arriving at its outer sidewall from the open area (Fig. 1), more deflected ions will bombard and etch its inner side, thus creating the notch. Notching is usually minimized by employing an etch chemistry that deposits a passivating layer at the sidewalls.[5] In the early work of Morimoto *et al.*,[6] it was reported that notching was significantly reduced by simply making the gate oxide thinner ($\leqslant 7$ nm). These authors speculated at the time that the reduction in notching was caused by ''the charge at the SiO_2 surface (being) discharged to the substrate.''

We present here a self-consistent treatment of pattern-dependent charging which explains the result of Morimoto *et al.*[6] and forms the basis for a new way to neutralize the surface charge by letting electrons tunnel quantum-mechanically *from the substrate*. While counter-intuitive, this idea is compatible with future devices that require oxide thickness <5 nm, for improved transistor operation and control.[7] Tunneling currents cause reliability problems and electrical failure when flowing through the oxide under a gate; however, even catastrophic currents through the oxide in cleared areas are unimportant for the electrical characteristics of the device, since the space is filled with dielectric after etching.[7] For the proposed idea to work, an electron supply to the substrate is needed. While hindered from reaching the SiO_2 surface directly through the trench entrance, plasma electrons arrive unimpeded at unpatterned surfaces; if the gate oxide extends to such open areas, the electrons could tunnel down to the conductive substrate, as illustrated in Fig. 1. The ''double-tunneling'' approach bears promise for eliminating both forms of charging damage: lower charging potentials will deflect fewer ions, thereby reducing notching, gate charging, and the concomitant (damaging) tunneling current under the gate.

Our Monte Carlo simulations of microstructure charging account explicitly for electron tunneling. Two mechanisms are considered, with well-established analytic expressions:[8] (a) Fowler-Nordheim tunneling (FNT) of electrons from the Fermi level of the n^+-polycrystalline Si (poly-Si) gate to the SiO_2 conduction band; and (b) direct tunneling (DT) of electrons from the n^+-poly-Si to the Si(100) conduction band (substrate). Tunneling from SiO_2 surface states is assumed to proceed likewise. The treatment of charging includes calculating the oxide field and the induced tunneling current to and from the substrate, for every SiO_2 surface segment. The substrate potential responds instantaneously to the net charge variation. Local electric fields are modified self-consistently as more charge accumulates, until steady state is reached. Surface currents and secondary electron emission are both neglected.

Typical high-density plasma conditions are assumed: low pressure (<10 mTorr), uniform Cl_2 plasma of density 1×10^{12} cm^{-3}, dissociated to a degree that renders etching

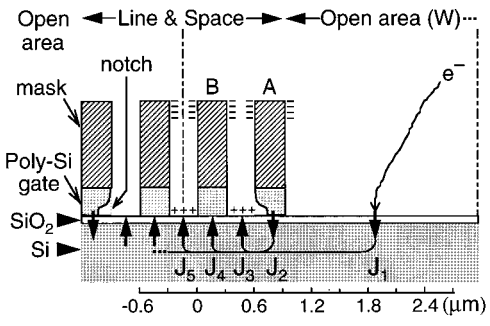

FIG. 1. Schematic of the line-and-space structure considered in the simulation. Note the location of the notch. The dashed-dotted lines indicate mirror axes defining the simulation domain. The arrows (J_i) indicate the direction of *electron* flow through the gate oxide at various surface segments.

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ion-limited. An rf bias of 60 V (peak-to-peak) is applied at 0.4 MHz. The ion and electron temperatures are assumed to be 0.5 and 4.0 V, respectively. A dc sheath bias of 7 V has been measured[4] to develop under these conditions. The simulated structure consists of four isolated 0.3 μm lines separated by 0.3 μm spaces (trenches). Identical patterns are separated by open areas with a width of 4 μm. At the onset of overetching, each feature consists of a 0.9 μm photoresist mask (insulating) onto 0.3 μm n^+-poly-Si gates, formed on top of a uniform layer of SiO_2, whose thickness is a control variable, critical for electron tunneling.

The steady-state charging potential distribution in the ''edge'' trench reveals the perturbation in the local ion dynamics occurring as a result of surface charging (Fig. 2). Gradients on this potential surface are a measure of the electric field that influences ion motion. As previously shown,[5] an asymmetric potential distribution, with a pronounced peak near the inner sidewall foot of the edge line, is critical for notch formation. Such a potential surface is obtained for $t_{ox}=50$ nm [Fig. 2(a)], where electron tunneling from the substrate is negligible. As the oxide thickness is decreased, FNT currents increase rapidly; substrate electrons tunnel through to the exposed SiO_2 surface, thereby changing profoundly the potential distribution at the trench bottom. Electron tunneling through the open area oxide also decreases the substrate potential. At $t_{ox}=20$ nm, the potential distribution peak disappears and the tilt of the potential surface towards the edge line is reduced (not shown). Thinning the oxide even more, completely flattens the potential surface, as shown in Fig. 2(b) for $t_{ox}=5$ nm. The dramatic changes in the potential distribution with t_{ox} forecast the reduction and elimination of notching.

To better understand how these changes occur, consider the tunneling current density through various surface segments [Fig. 3(a)]. Insignificant electron tunneling occurs for $t_{ox}>50$ nm. As t_{ox} decreases, FNT currents increase abruptly;[8] electrons tunnel down from the open area surface to the conductive substrate and then up to the trench bottom surfaces, reducing their charging potentials. The currents through the uncovered oxide areas saturate for ultrathin oxides. Surprisingly, the current through the oxide under the edge gate (J_2) goes through a minimum at $t_{ox}=7$ nm. Since oxide degradation under the gate is detrimental for device operation, the latter observation points to a strategy for reducing charging damage. For $t_{ox}<7$ nm, tunneling under the edge line and under the neighboring line increases rapidly as the DT mechanism becomes dominant. Remarkably, even for long (>5 min) overetching, the time-integrated oxide current (<0.1 C/cm^2 even for the highest values of J_4) is smaller than that capable of causing significant degradation (≈ 10 C/cm^2).[7] This observation suggests that charging damage must be occurring during earlier stages of etching.[9]

The variation in the tunneling current under each gate can be understood by examining their potentials as a function of t_{ox} [Fig. 3(b)]. As explained earlier, the equipotential of the edge gate is significantly lower than that of the neighboring gate. The potentials of both gates decrease with decreasing t_{ox}; the drop is larger for the neighboring line. In contrast, the substrate potential increases abruptly between $t_{ox}=100$ and 50 nm, and then decreases gradually for thinner

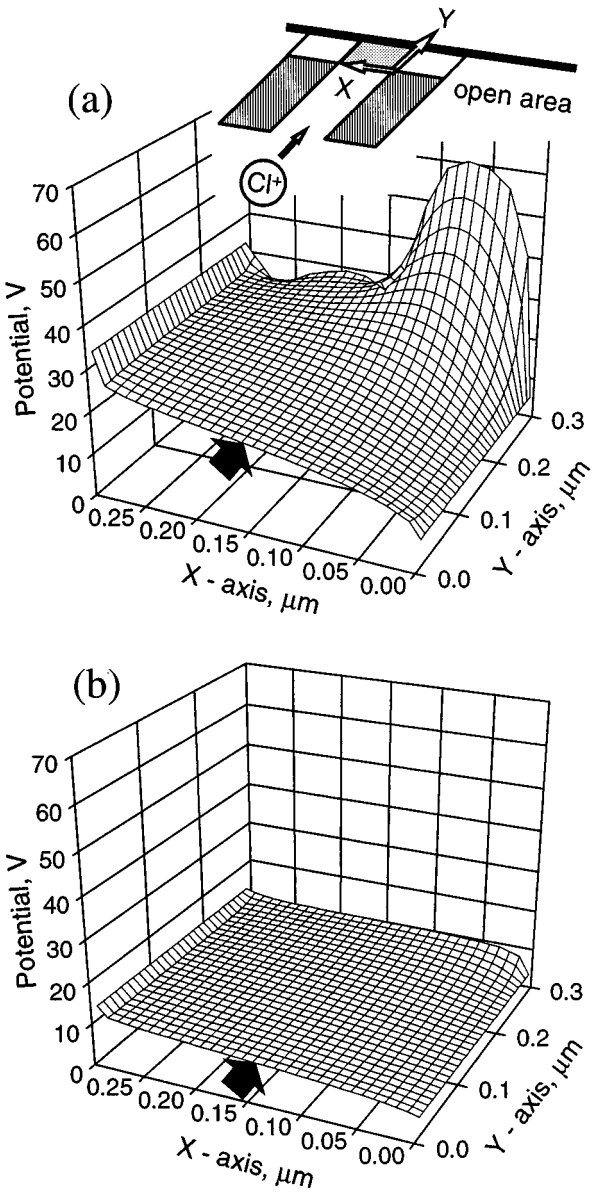

FIG. 2. Three-dimensional charging potential distributions in the ''edge'' trench for structures with an SiO_2 thickness of: (a) 50 nm and (b) 5 nm. The inset in (a) illustrates the area of interest and defines the origin for the potential surface. The microstructure has been rotated so that the direction of ions as they approach the potential surface corresponds to the direction of ions as they enter the trench (arrows).

oxides. The difference between the gate and substrate potentials (V_{ox}) determines the oxide field (V_{ox}/t_{ox}) and fully explains the tunneling current behavior seen in Fig. 3(a). In particular, the tunneling current (J_2) extrema correspond to oxide field extrema. Note that the potentials of the neighboring gate and the substrate drop at the same rate.

The reduction of the positive charge buildup at the bottom of the trench decreases both the flux and average energy of ions bombarding the inner sidewall of the edge gate. The ion current to the trench bottom increases since fewer ions get deflected; in contrast, the corresponding electron current from the plasma to the same surface decreases.[10] The current balance at steady state is achieved by tunneling electrons through the substrate. For $t_{ox}=3$ nm, the electron current J_3 is *four times* that arriving through the trench entrance.

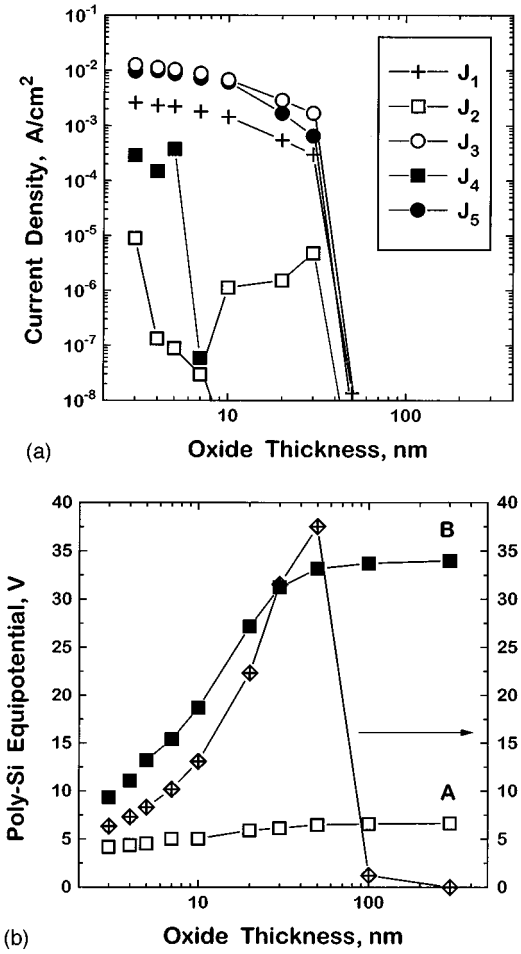

FIG. 3. (a) Total electron tunneling currents to various surface segments, as a function of oxide thickness; the individual currents J_i are defined in Fig. 1. (b) The steady-state equipotentials of the poly-Si edge gate (A) and its neighboring gate (B), as a function of oxide thickness. The substrate potential is shown by the crossed diamonds.

Profile evolution simulations have been performed for various t_{ox}, as described in detail elsewhere.[5] The notch depth (for fixed overetching time) at the edge gate decreases precipitously as soon as tunneling becomes possible ($t_{ox}<50$ nm), as shown in Fig. 4. Notching becomes imperceptible for $t_{ox}\leqslant 7$ nm. This result is even more remarkable, considering that less overetching is required for thinner oxides—since more ions impinge at the trench bottom. Although the plasma and rf bias conditions used by Morimoto *et al.*[6] were not reported, which makes a comparison of notching results appear somewhat ambiguous, it is still instructive to replot our results in terms of the ''re-entrant'' angle, defined as the angle between the notched sidewall and the wafer normal, together with the experimental points of Morimoto *et al.* (Fig. 5). The exact location of the abrupt transition from significant notching ($\approx 31°$) to no notching ($\approx 5°$) is captured. The good agreement is more than fortuitous, since the transition is controlled by t_{ox} alone.[11]

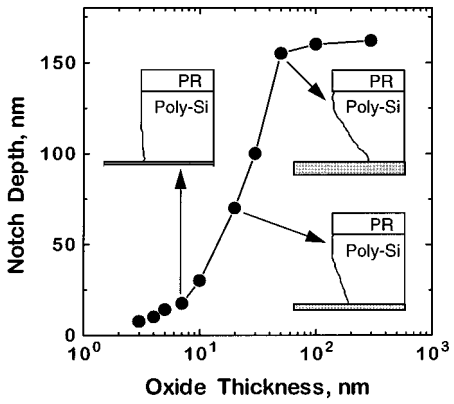

FIG. 4. Dependence of the notch depth at the edge gate on oxide thickness for fixed overetching time. Representative profiles are shown as insets. The mask (PR) has been truncated to save space. The poly-Si aspect ratio has been preserved. The outer sidewall evolution is not simulated.

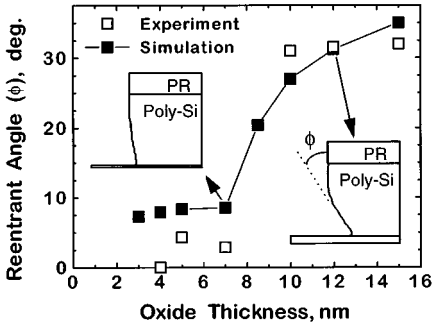

FIG. 5. Comparison between experiment and simulations in terms of the re-entrant angle, ϕ, at the notched area as a function of oxide thickness for longer overetching time than that of Fig. 4. The experimental points are reproduced from Morimoto *et al.* (Ref. 6).

In conclusion, a self-consistent theory of charging phenomena during overetching in plasmas suggests that electron tunneling could help reduce notching. The calculations also reveal that small steady-state tunneling currents flow during overetching, capable of generating cumulative charging damage only after long overetches.[9] Necessary conditions for these effects include thin (<7 nm) gate oxides—required by the industry anyway for smaller and faster devices—combined with a low substrate potential (<5 V), so that neutralization of surface potentials can be achieved by electron tunneling from the substrate through the ultrathin oxide.

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[10] Since fewer deflected ions reach the upper photoresist sidewalls as t_{ox} decreases, the entrance potential becomes more negative, thus preventing more plasma electrons from entering the trench.
[11] Variation of the plasma conditions and rf bias in the typical regime for high-density plasmas does not change the location of the transition. The same is true for a slightly higher energy threshold to reaction, to account for the use of oxygen in the experiment.