Design Issues in CMOS Differential *LC* Oscillators

Ali Hajimiri and Thomas H. Lee

***Abstract*— An analysis of phase noise in differential cross-coupled inductance–capacitance *(LC)* oscillators is presented. The effect of tail current and tank power dissipation on the voltage amplitude is shown. Various noise sources in the complementary cross-coupled pair are identified, and their effect on phase noise is analyzed. The predictions are in good agreement with measurements over a large range of tail currents and supply voltages. A 1.8-GHz *LC* oscillator with a phase noise of −121 dBc/Hz at 600 kHz is demonstrated, dissipating 6 mW of power using on-chip spiral inductors.**

***Index Terms*—Design methodology, noise measurement, oscillator noise, oscillator stability, phase jitter, phase-locked loops, phase noise, voltage-controlled oscillators.**

I. Introduction

DUE to their relatively good phase noise, ease of implementation, and differential operation, cross-coupled inductance–capacitance *(LC)* oscillators play an important role in high-frequency circuit design [1]–[6]. In this paper, the time-variant phase-noise model of [7] will be applied to analyze these oscillators. A simple expression for the tank amplitude is first obtained. The effect of different noise sources in such oscillators is then investigated, and methods for exploiting the cyclostationary properties of noise are shown. New design implications arising from this approach and experimental results are given. A differential *LC* oscillator using spiral inductors is demonstrated that dissipates 6 mW of power while running at 1.8 GHz, with a phase noise of −121 dBc/Hz at 600-kHz offset.

The dependence of tank amplitude on the tail current and supply voltage is calculated in Section II. The effect of noise sources in both active and resistive tank loss is analyzed in Section III. Section IV investigates the effect of tail-current noise. Last, design insights and experimental results are presented in Section V.

II. Tank Amplitude

Tank voltage amplitude has an important effect on the phase noise, as emphasized by the presence of $q_{\max}$ in the denominator of the expression for the single-sideband phase noise [7]

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log_{10}\left(\frac{\overline{i_n^2}/\Delta f}{q_{\max}^2} \cdot \frac{\Gamma_{\rm rms}^2}{2\Delta\omega^2}\right) \qquad (1)$$

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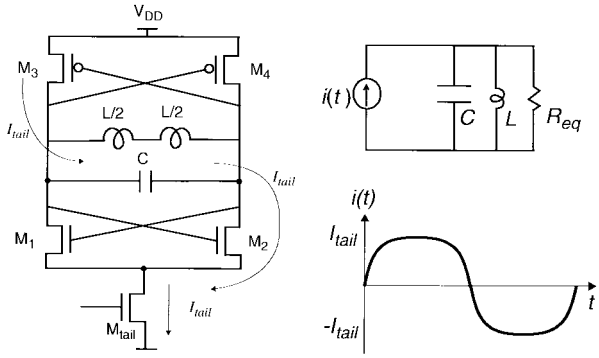

Fig. 1. (a) Current flow when the stage is switched to one side. (b) Differential equivalent circuit.

where $\overline{i_n^2}/\Delta f$ is the power spectral density of the parallel current noise, $\Gamma_{\rm rms}$ is the rms value of the impulse sensitivity function (ISF) associated with that noise source, $q_{\max}$ is the maximum signal charge swing, and $\Delta\omega$ is the offset frequency from the carrier.

A simple expression for the tank amplitude can be obtained assuming that the current in the differential stage switches quickly from one side to another. Fig. 1(a) shows the current flowing in the complementary cross-coupled differential *LC* oscillator [3] when it is completely switched to one side. As the tank voltage changes, the direction of the current flow through the tank reverses. The differential pair thus can be modeled as a current source switching between $I_{\rm tail}$ and $-I_{\rm tail}$ in parallel with a resistance–inductance–capacitance *(RLC)* tank, as shown in Fig. 1(b). $R_{\rm eq}$ is the equivalent parallel resistance of the tank.

At the frequency of resonance, the admittances of the L and C cancel, leaving $R_{\rm eq}$. Harmonics of the input current are strongly attenuated by the *LC* tank, leaving the fundamental of the input current to induce a differential voltage swing of amplitude $(4/\pi)I_{\rm tail}R_{\rm eq}$ across the tank if one assumes a rectangular current waveform. At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain. In such cases, the tank amplitude can be better approximated as

$$V_{\rm tank} \approx I_{\rm tail}R_{\rm eq}. \qquad (2)$$

This mode of operation is referred to as the *current-limited* regime of operation since, in this regime, the tank amplitude is solely determined by the tail-current source and the tank equivalent resistance. Fig. 2 shows the simulated node voltages as well as the drain currents of the NMOS transistors, M_1 and M_2, in this regime of operation. The values of L and C are such that the circuit oscillates at 1 GHz.

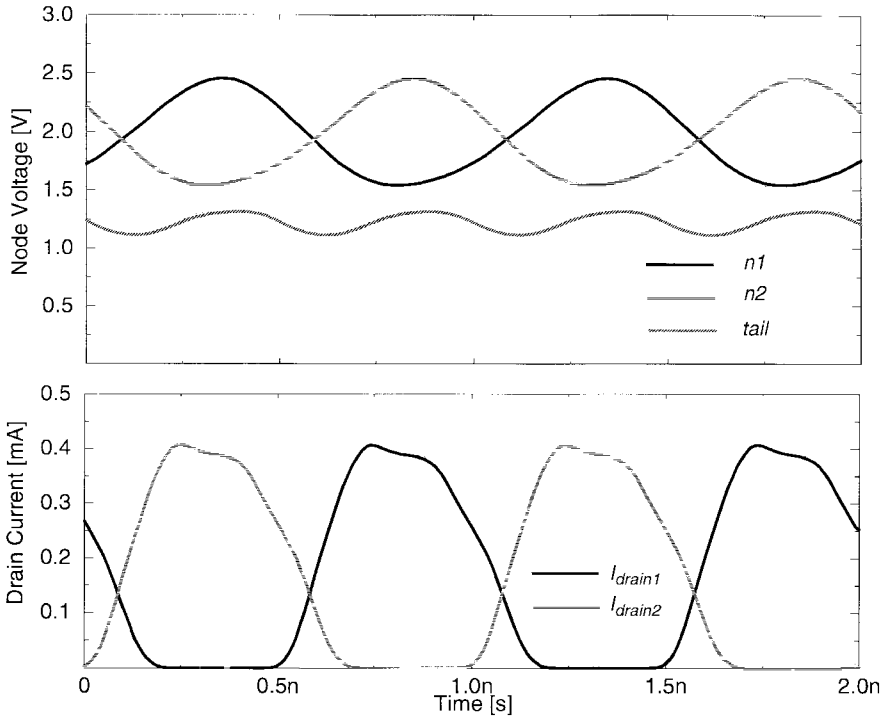

Fig. 2. Simulated voltages and currents in the current-limited regime.

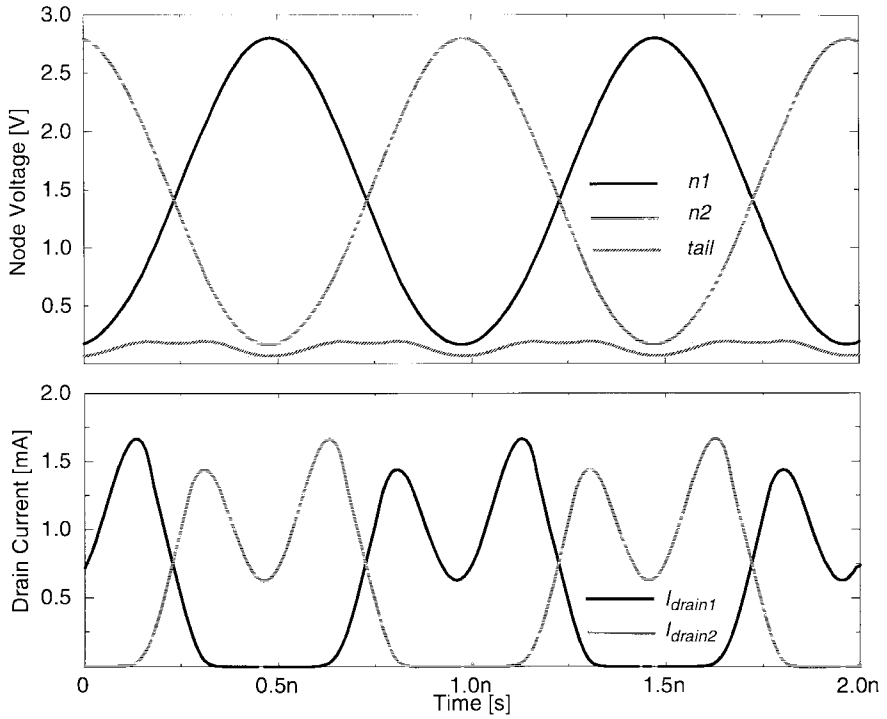

Fig. 3. Simulated voltages and currents in the voltage-limited regime.

Note that (2) loses its validity as the amplitude approaches the supply voltage because both NMOS and PMOS pairs will enter the triode region at the peaks of the voltage. Also the tail NMOS transistor may spend most (or even all) of its time in the linear region. This behavior can be seen in the simulated voltages and currents shown in Fig. 3. The tank voltage will be clipped at $V_{\rm DD}$ by the PMOS transistors and at ground by the NMOS transistors. Therefore, for the oscillator of Fig. 1(a), the tank voltage amplitude does not significantly exceed $V_{\rm DD}$. Note that since the tail transistor is in the triode region, the tail current does not stay constant. Thus, the drain-source voltage of the differential NMOS transistors can drop significantly,

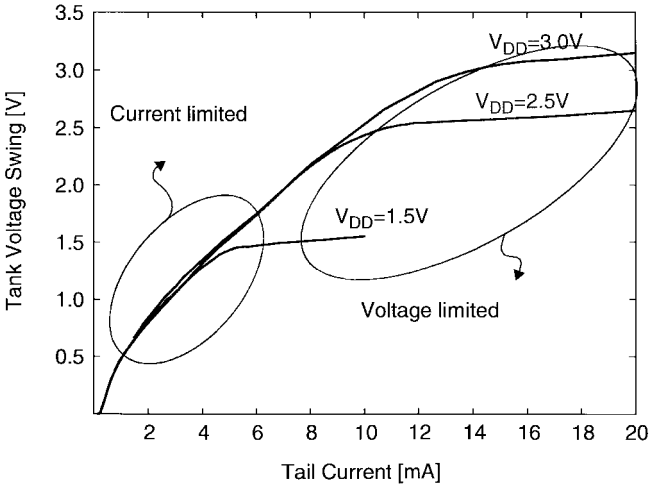

Fig. 4. Simulated tank voltage amplitude versus tail-current source for the 1.8-GHz complementary differential oscillator.

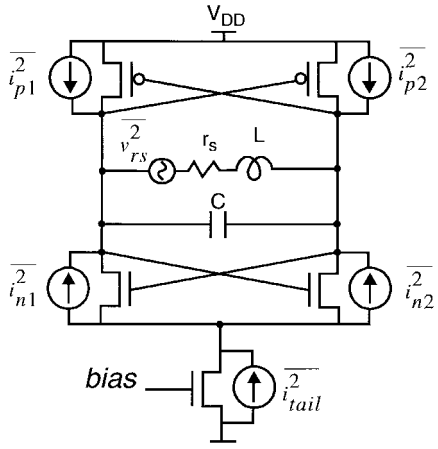

Fig. 5. Complementary *LC* oscillator with noise sources.

resulting in a large drop in their drain current, as shown in Fig. 3. This region of operation is known as the *voltage-limited* regime.

Fig. 4 shows the simulated tank voltage amplitude as a function of tail current for three different values of $V_{\rm DD}$. As can be seen, the tank amplitude is proportional to the tail current in the current-limited region, while it is limited by $V_{\rm DD}$ in the voltage-limited regime.

III. Noise Sources

Fig. 5 depicts the noise sources in the oscillator. The noise power densities for these sources are required to calculate the phase noise using (1). In general, these noise sources are cyclostationary because of the periodic changes in currents and voltages of the active devices. In this section, we first introduce a simplified stationary model for the noise sources and then examine subtleties arising from their cyclostationary behavior.

A. Stationary Noise Sources

In a simplified stationary approach, the power densities of the noise sources can be evaluated at the most sensitive time (i.e., the zero crossing of the differential tank voltage) to estimate the effect of these sources [7]. Fig. 6(a) shows a simplified model of the sources in this balanced case. Converting the current sources to their Thevenin equivalent and writing Kirchoff's voltage law, one obtains the equivalent differential circuit shown in Fig. 6(b). Note that the equivalent parallel resistance is canceled by the negative resistance provided by the positive feedback. Therefore, the total differential noise power due to the four cross-coupled transistors is

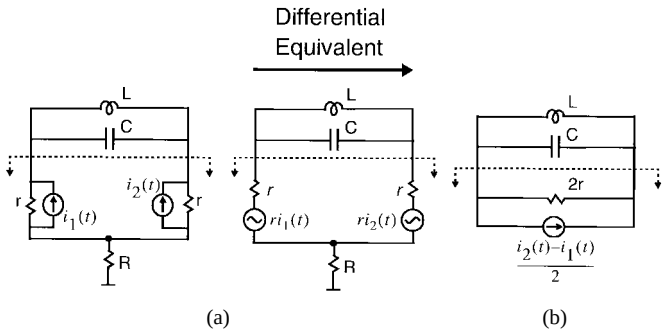

Fig. 6. (a) Simplified model for transistor noise sources. (b) Differential equivalent circuit.

$$\overline{i_{\rm cc}^2} = \tfrac{1}{4}\left(\overline{i_{n1}^2} + \overline{i_{n2}^2} + \overline{i_{p1}^2} + \overline{i_{p2}^2}\right) = \tfrac{1}{2}\left(\overline{i_n^2} + \overline{i_p^2}\right) \tag{3}$$

where $\overline{i_n^2} = \overline{i_{n1}^2} = \overline{i_{n2}^2}$ and $\overline{i_p^2} = \overline{i_{p1}^2} = \overline{i_{p2}^2}$. Noise densities $\overline{i_n^2}/\Delta f$ and $\overline{i_p^2}/\Delta f$ are given by

$$\overline{i_n^2}/\Delta f = 4kT\gamma\mu C_{\rm ox}\frac{W}{L}(V_{\rm GS} - V_T) \tag{4}$$

where μ is the mobility of the carriers in the channel, $C_{\rm ox}$ is the oxide capacitance per unit area, W and L are the width and length of the MOS transistor, respectively, $V_{\rm GS}$ is the gate-source voltage, and V_T is the threshold voltage. Equation (4) is valid for both short- and long-channel regimes of operation. γ, however, is around 2/3 for long-channel transistors while it may be between two and three in the short-channel region due to hot-electron effects [8].

In addition to these sources, the contribution of the effective series resistance of the inductor r_s caused by ohmic losses in the metal and substrate is given by

$$\overline{i_{\rm rs}^2}/\Delta f = 4kT\frac{r_s C}{L} = \frac{4kT}{R_p} \tag{5}$$

where $R_p \approx Q^2 r_s = (L\omega_0)^2/r_s$ is the equivalent parallel resistance at the frequency of oscillation.

B. The Effect of a Tail Capacitor

The foregoing analysis is based on the assumption that the sum of the currents through the differential transistors is equal to the tail current at all times. However, this assumption can break down if there is a capacitor in parallel with the tail-current source. This capacitor provides an alternative path for the tail current. If the tail capacitor is large, the differential pair transistors might carry very little current for a fraction of the cycle.

To investigate further the effect of this capacitor, the simulation of the 1-GHz complementary *LC* oscillator of Fig. 2

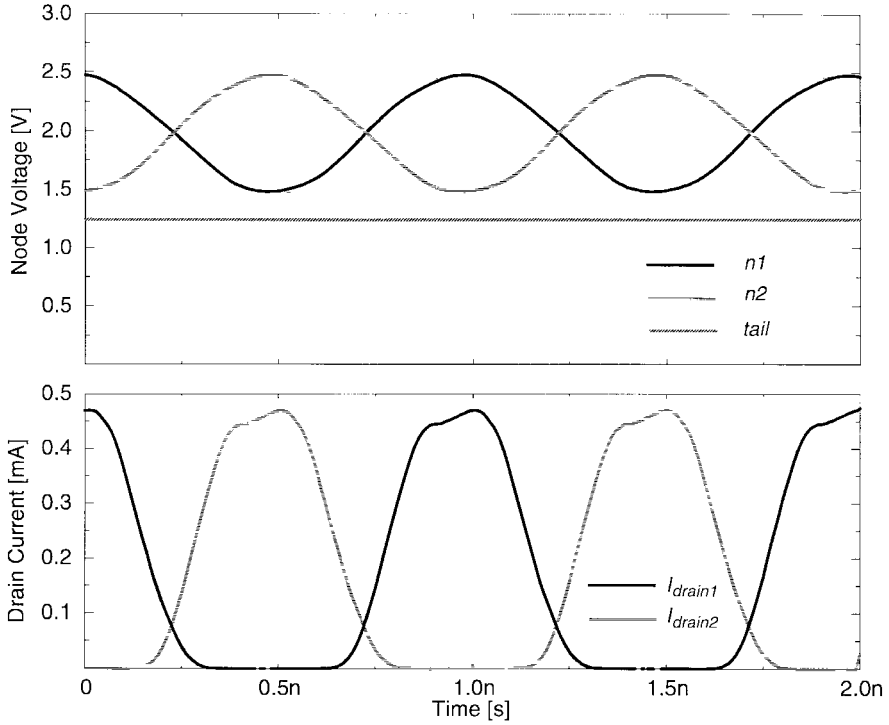

Fig. 7. Simulated voltages and currents in the current-limited regime with a 10-pF tail capacitor.

was repeated with a 10-pF tail capacitor. Fig. 7 shows the voltage of the differential and tail nodes, as well as the drain currents of M_1 and M_2 in the presence of the tail capacitor. A reduction in the duty cycle of the drain current waveform can be seen in Fig. 7 relative to that in Fig. 2. This change in the duty cycle of the waveform is particularly important, as it reduces the drain current (and the drain current noise) of the differential NMOS and PMOS transistors during the zero-crossing of the tank differential voltage. As shown in [7], this moment is when the oscillator is most sensitive to a perturbation. Therefore, the use of an extra tail capacitor can improve the phase-noise behavior of the differential *LC* oscillator.[1] The tail capacitor also shapes the effect of noise in $M_{\rm tail}$ in other important ways, as will be discussed in the next section.[2]

IV. Tail Current Noise Source

To gain further insight into the effect of the tail noise source, its ISF, as well as those for the NMOS and PMOS drain noise sources, are shown in Fig. 8. The ISF's are calculated using direct impulse injection and measuring the resultant phase shift.

As can be seen from Fig. 8, the ISF associated with the tail-current source has a fundamental frequency that is double the oscillation frequency. This is expected since the tail node is pulled up every time each one of the differential NMOS transistors turns on, and thus the tail node moves at twice the frequency of the differential voltage.

Due to this frequency doubling, the Fourier component of the ISF at ω_0 denoted by c_1 is zero, and therefore the noise of the tail-current source in the vicinity of ω_0 has no effect on the differential noise current. However, even-order coefficients such as c_0, c_2, and c_4 are significant; therefore, noise components around even harmonics of ω_0 have a significant effect on the phase noise, as shown in Fig. 9. Also, the low-frequency noise component of the tail noise source can affect phase noise through asymmetry. To verify this behavior, a sinusoidal current with an amplitude of 200 μA was injected in parallel with the tail-current source, and the induced sideband power below the carrier was measured using fast Fourier transform (FFT) analysis in HSPICE. As can be seen in Fig. 10, sinusoidal injection at low frequency (f_m) and in the vicinity of twice the oscillation frequency $(2f_0 + f_m)$ results in noticeable sidebands. However, sinusoidal injection of the same amplitude at $f_0 + f_m$ does not produce any observable sidebands.

The tail capacitor mentioned in the previous section attenuates the high-frequency noise components of the tail-current source, so one expects corresponding attenuation of phase noise due to this noise. In fact, the induced sidebands due to injection at $2f_0 + f_m$ in the presence of the 10-pF tail capacitor are very small and are below the numerical noise floor of the FFT operation.

Since upconversion of $1/f$ noise is thus the most significant remaining noise component of noisy tail current, one must properly size the tail-current transistor and satisfy the single-

[1] The tail capacitor attenuates the voltage variations on the *tail* node and therefore reduces the channel length modulation of the tail-current source. This effect results in more symmetric waveforms and smaller harmonic distortion in the output of the oscillator.

[2] One disadvantage of such a tail capacitor is that it reduces the output impedance of the tail-current source at high frequencies. This reduction increases the sensitivity of the oscillator to supply-voltage variations.

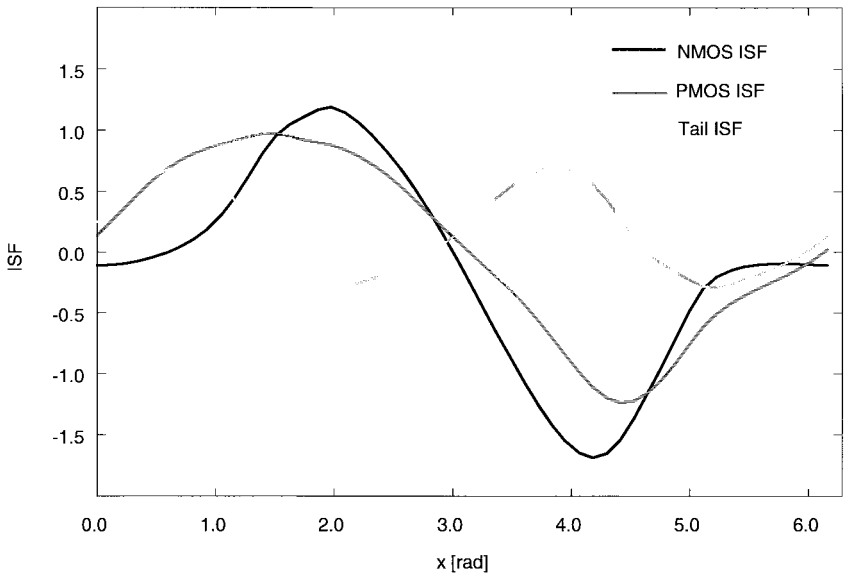

Fig. 8. The simulated ISF's of different noise sources in the 1.8-GHz complementary differential oscillator.

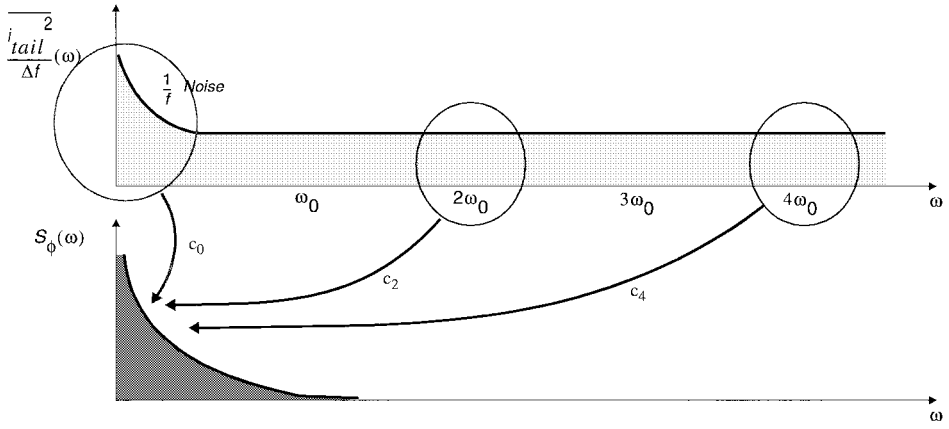

Fig. 9. Evolution of tail noise current.

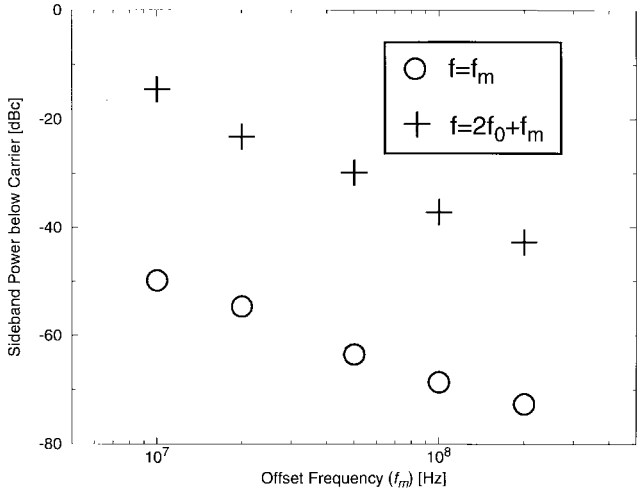

Fig. 10. Induced sidebands due to sinusoidal perturbation at $f_{\rm dev}$ and $2f_0 + f_{\rm dev}$.

ended symmetry criterion by sizing the cross-coupled NMOS and PMOS transistors properly.

V. Experimental Results and Design Insights

The complementary oscillator of Fig. 1(a) is implemented in a five-metal, 0.25-μm epi-CMOS technology. The complementary structure is used to maintain single-ended symmetry of each half circuit to mitigate the upconversion of $1/f$ noise. Fig. 11 shows the die photograph of the implemented oscillator. Two square inductors in series are laid out symmetrically in metal 3, 4, and 5. The series combination of the two constitutes the tank inductor. Each inductor is 230 μm on a side and has four turns. Vias are used to keep the three metal layers at the same potential and are interleaved to minimize the parasitic capacitance. Field-solver simulation of this inductor predicts an inductance of 2.0 nH and an effective Q of 7.5 at 1.8 GHz, which translates to an effective series resistance of $r_s = 3.0\Omega$ for each inductor. Simulated tank voltage amplitude at 1.8 GHz versus tail current is shown in Fig. 4.

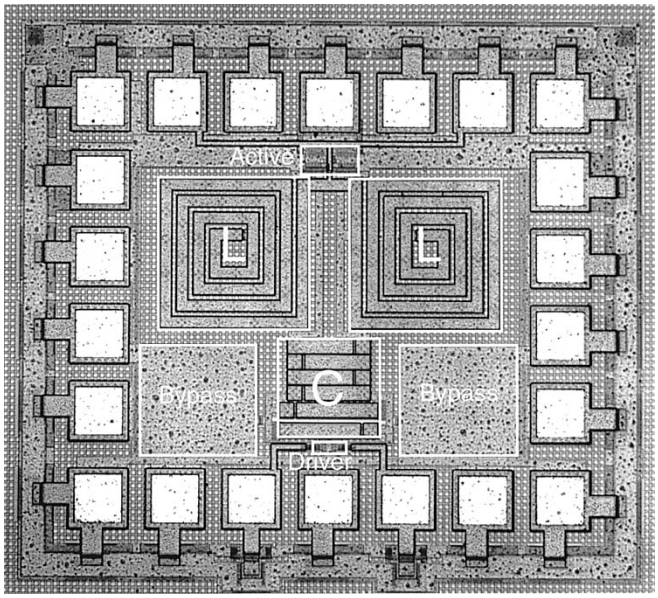

Fig. 11. Die photograph of the differential *LC* oscillator.

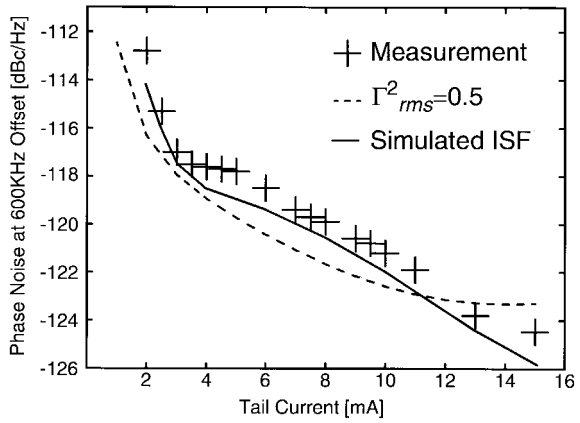

Fig. 12. Predicted and measured phase noise at 600-kHz offset versus $I_{\rm tail}$ for $f_0 = 1.8$ GHz and $V_{\rm DD} = 3$ V.

Fig. 12 shows a plot of phase noise at a 600-kHz offset versus the tail current with a 3.0-V supply. The dashed line shows the phase-noise predictions obtained using a simplified model for noise and amplitude and assuming a sinusoidal waveform so that $\Gamma_{\rm rms}^2$ equals 0.5. As can be seen, these simplifying assumptions lead to reasonable predictions. More accurate predictions can be obtained by calculating the true ISF and taking into account the effect of cyclostationarity of noise sources in (1). The solid line shows the predictions obtained using the full-blown analysis. As can be seen, good agreement between the theoretical predictions and measurements is observed for different bias points.

To gain more insight about the tradeoffs involved, the phase noise at 600-kHz offset is measured for different values of the supply voltage and tail current, as shown in Fig. 13. Each measured value is shown as a node on the three-dimensional surface. Note that bias points not achievable are shown as a flat surface. As can be seen from this graph, increasing the tail current will improve the phase noise due to the increase in oscillation amplitude. Also, as can be seen, the improvement slows down as the tank voltage amplitude approaches the supply voltage. It can also be seen that the phase noise has a weak dependence on the supply voltage, improving somewhat for lower voltages. This behavior may be attributed to smaller voltage drops across the channel on the MOS transistors, which reduce the effect of velocity saturation in the short-channel regime and hence lower γ.

The power dissipation increases as we move toward higher tail currents and supply voltage, which corresponds to moving from right to left in Fig. 13. If the goal of design is to achieve the minimum phase noise, without any concern for power dissipation, the oscillator should be operated at high supply voltage and high current to allow the maximum possible tank voltage amplitude. Point A in Fig. 13 is an example of such an operation point. It corresponds to a tail current of 16 mA and a supply voltage of 3 V, and results in a phase noise of -125.7 dBc/Hz at 600-kHz offset.

Because power consumption is usually a concern, a more practical goal is to minimize phase noise for a given power dissipation. Equation (1) suggests that it is desirable to operate at the largest tank amplitude for a given power dissipation. However, the tank amplitude cannot be increased beyond $V_{\rm DD}$ due to voltage limiting. Therefore, according to this simple model, it is desirable to operate at the edge of the voltage-limited mode of operation. As can be seen in Fig. 4, point B is at the verge of voltage limiting, which explains the good phase noise seen in Fig. 13. Under this operation point, 4 mA of dc current is drawn from a 1.5-V power supply, resulting in a phase noise of -121 dBc/Hz at 600 kHz offset from the carrier while dissipating 6 mW of power.

To investigate the effect of the PMOS transistors, an NMOS-only oscillator is compared to the complementary case. The supply voltage is provided through the middle node of the inductor, and the phase noise of this NMOS-only oscillator is measured for different supply voltages and tail currents. The result is plotted together with the data from Fig. 13 in Fig. 14. Note that the NMOS-only oscillator exhibits inferior phase noise at all the measured bias points.

There are several reasons for the superiority of the complementary structure over the all-NMOS structure. The complementary structure offers higher transconductance for a given current, which results in faster switching of the cross-coupled differential pair. It also offers better rise- and fall-time symmetry, which results in a smaller $1/f^3$ noise corner. Also, the dc voltage drop across the channel is larger for the all-NMOS structure since the dc value of the drain voltage is $V_{\rm DD}$. There is therefore stronger velocity saturation and a larger γ. As long as the oscillator operates in the current-limited regime, the tank voltage swing is the same for both oscillators.[3]

VI. Conclusion

An analysis of phase noise in differential cross-coupled *LC* oscillators was presented. The effect of tail current and equivalent tank loading on voltage amplitude was shown in

[3]If the rare case of achieving the lowest possible phase noise without any concern for power dissipation is the design objective, all-NMOS structures can offer a larger voltage swing and therefore may be the preferred topology.

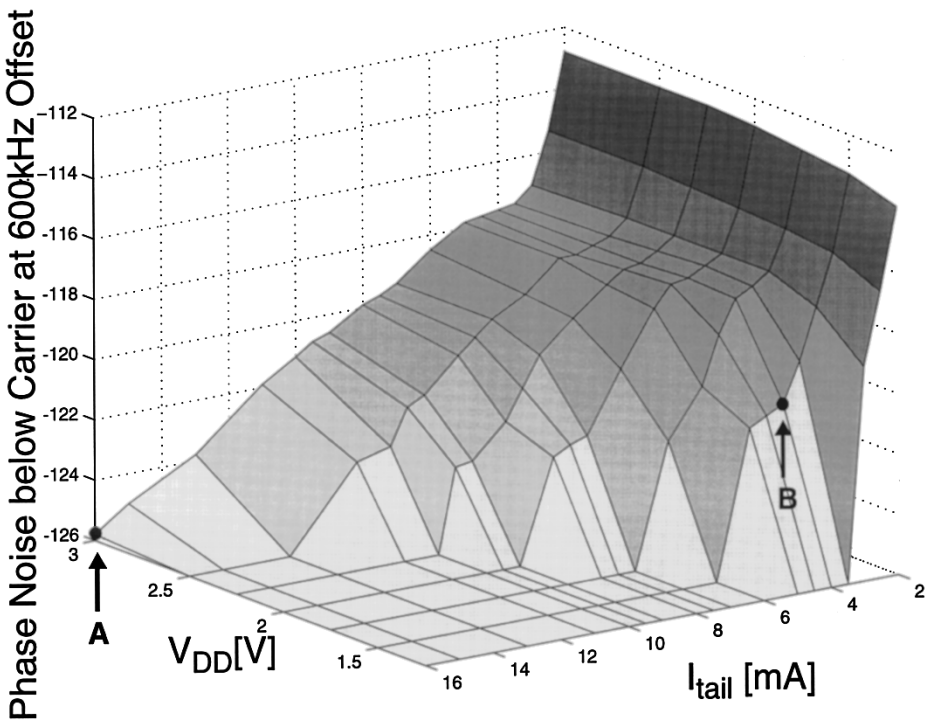

Fig. 13. The measured phase noise versus $V_{\rm DD}$ and $I_{\rm tail}$ for the complementary *LC* oscillator with $f_0 = 1.8$ GHz.

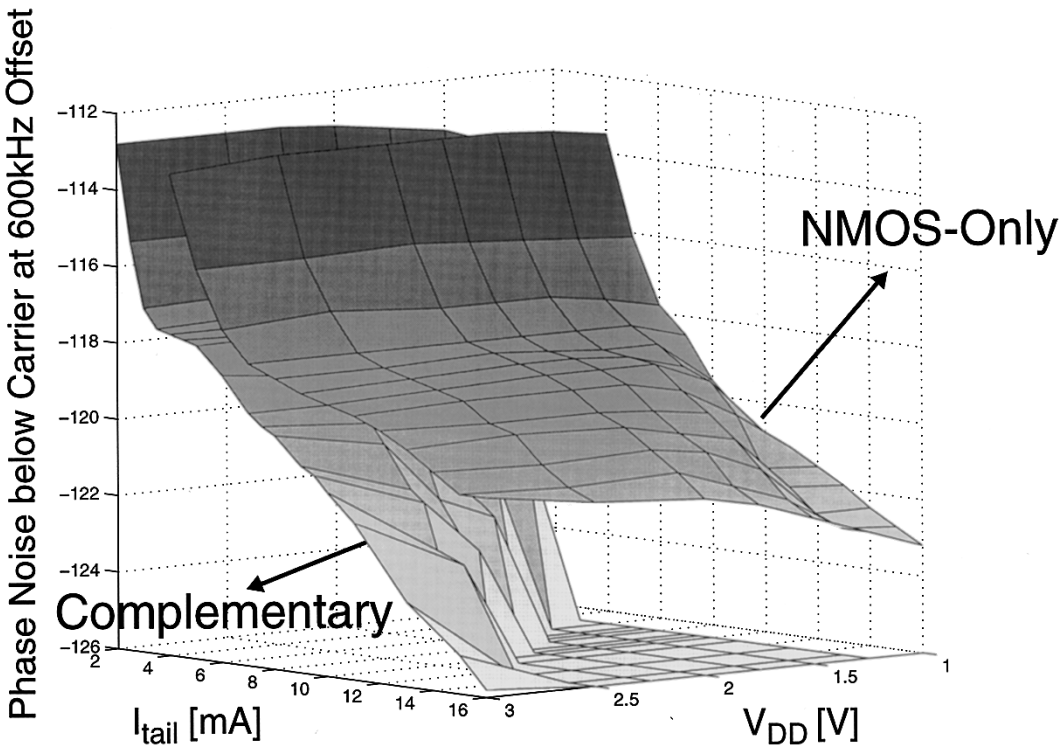

Fig. 14. Measured phase noise for complementary and NMOS-only oscillator.

both current- and voltage-limited modes of operation. The effect of various noise sources in the circuit was analyzed, and it was shown that the effective noise introduced by the transistors in the differential pair can be reduced by exploiting cyclostationary properties of the sources. The predictions made are in good agreement with the measurements for different tail currents and supply voltages. A 1.8-GHz *LC* oscillator using on-chip spiral inductors exhibits a phase noise of -121 dBc/Hz at 600 kHz while dissipating 6 mW of power.

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