Continuous-Time Adaptive Delay System

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Abstract

We have developed an adaptive delay system that adjusts the delay of a delay element so that it matches the temporal disparity between the onset of two input signals. The delay is controlled either by an external bias voltage, or by an intrinsic signal derived from an adaptive block. The operation of the adaptive delay system is similar to that of a charge-pump phase-lock loop, with an extended lock-in range of more than 5 decades. Standard CMOS transistors are used in their subthreshold region. Experimental results from circuits fabricated in $2\mu m$ CMOS technology are in agreement with the analysis.

Introduction

Conventional charge-pump phase-locked loop systems compare the output of a voltage controlled oscillator (VCO) to an incoming periodic input signal[1]. A phase comparator circuit compares the relative timing of the VCO output and the input signal and generates a lead or lag signal with a duration corresponding to the time difference between the onset of the VCO and that of the input. The lead or lag signal (error signal) is used to correct the voltage input to the VCO so that the correct VCO frequency is generated. The voltage input is stored on a capacitor and the capacitor is charged or discharged with a fixed current source during the duration of the error signal. The VCO frequency can show considerable overshoot before it settles to the correct frequency.

The adaptive delay system described here incorporates a versatile delay element that has *continuous-time adaptation.* The delay through a delay element is controlled by a bias voltage. The system computes the temporal disparity between the onset of two input signals and adapts the bias voltage so that the delay through the delay element matches the temporal disparity of the signals. The progression of the bias voltage to the final steady-state value occurs monotonically, and the gain of the system can be adjusted to control the time constant of this adaptation. A variable current source controlled by the bias voltage is used to charge or discharge the capacitor on which this voltage is stored. Their new adaptation dynamics allow the lock-in range of the adaptive system to occur over 5 decades in delay. This adaptive system is similar to the adaptation characteristics in biological systems that must handle input signals with a large dynamic range in time or other dimensions.

The circuit was fabricated in $2\mu m$ CMOS technology: experimental results from the chip are presented. The adaptive delay capability can be incorporated in any system that includes a delay element.

Architectural Model

A block diagram of the adaptive delay system is shown in Figure 1. The relative timing of the signals in this system is shown in Figure 2. The signals shown are all discrete-level, continuous-time pulses except for the bias voltage, V_D. The signal *pulse*1 is the input signal that arrives first while *pulse*2 is the input signal that arrives next. The interval t_i is the input temporal disparity between both input signals. The signal *dpulse*1 is a delayed version of *pulse*1 where the delay of the variable delay element, t_d, is controlled by V_D. Circuits using the signals, *pulse*1, *pulse*2 and *dpulse*1, are leading edge-triggered. The lead/lag discriminator in Figure 1 compares the arrival of *dpulse*1 with that of *pulse*2 and outputs an error signal, V_{lead} or V_{lag} if the signals do not arrive in synchrony. The feedback system uses V_{lead} and V_{lag}, to correct V_D in the charge pump block in Figure 1. This change in V_D is reflected as a change of t_d in the variable delay element so that t_d adapts to t_i.

Lead/Lag Discriminator

The lead/lag discriminator circuit shown in Figure 3 computes the time difference Δt between the delay through the delay element, t_d and the input temporal disparity, t_i. V_{lag} becomes active for the duration Δt when $t_i < t_d$ and $\overline{V_{lead}}$ becomes active for the duration Δt when $t_i > t_d$. The circuit on the right of Figure 3

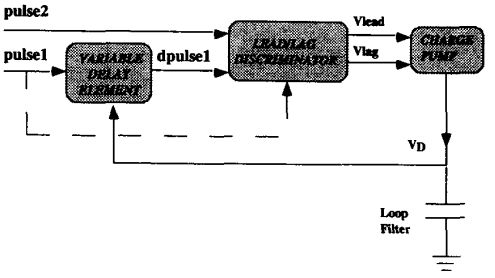

Figure 1: Block diagram of adaptive delay system. *All signals are pulses (continuous-time, discrete-level) except for the bias voltage, V_D.*

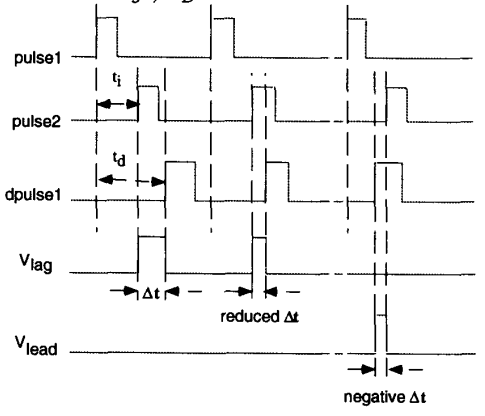

Figure 2: Relative timing of the signals shown in the block diagram in Figure 1. The input signals *pulse*1, *pulse*2 and *dpulse*1 are edge-triggered. The system adapts t_d to match t_i. V_{lead} is the output error signal when $t_d < t_i$ and V_{lag} is the output error signal when $t_d > t_i$.

computes whether $t_i < t_d$, while the circuit on the left computes whether $t_i > t_d$.

Let's first look at the circuit that creates V_{lag}. The arrival of $\overline{pulse1}$ triggers the delay element (as shown in Figure 1), and at the same time charges up node A. Node B does not go low until *pulse*2 arrives. If *dpulse*1 arrives before *pulse*2, node A is discharged to ground and prevents node B from switching. Hence V_{lag} stays low, whereas in the circuit on the left, $\overline{V_{lead}}$ becomes active. However if *pulse*2 comes first before *dpulse*1, node B goes low and V_{lag} goes high. V_{lag} is only high for the duration Δt. Q1 and Q2 are present to prevent V_{lag} and $\overline{V_{lead}}$ from being active at the same time.

The circuit on the left creates $\overline{V_{lead}}$. When $\overline{V_{lead}}$ becomes active, Q2 turns on and the current through Q1 and Q2 is mirrored in Q3. This current prevents node C from being pulled low when $\overline{pulse1}$ comes along, hence preventing V_{lag} from becoming active.

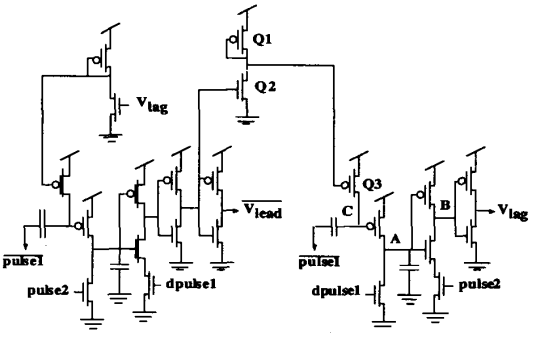

Figure 3: Lead/lag discriminator used in the adaptive delay system.

Charge Pump

The key block in the feedback system is the *charge pump* shown in Figure 4. The circuit adapts V_D so that t_d matches t_i. In traditional charge-pump phase-lock loop systems, a fixed current source is used to charge or discharge the capacitor C_b during Δt. In our system however, the adaptation of V_D depends on the *delay contrast ratio*, $\Delta t/t_i$. This ratio is important since for a given Δt error, the amount of correction of V_D should depend on the absolute temporal disparity, t_i. If Δt is a small fraction of t_i, then V_D should be corrected by a small amount. Conversely, if Δt is a large fraction of t_i, then V_D should be corrected by a larger amount. The dependence of the adaptation of V_D on the delay contrast ratio allows the system to match t_D with t_i monotonically over a wide range of t_i.

The circuit operates as follows: The current flowing in Q4 is equal to the current I_{in} in the delay element since Q4 is also biased by V_D. This current is mirrored through transistor, Q5 into Q11 and is mirrored through transistors Q6-Q7 into Q9. Q8 and Q12 act as switches in the circuit. If $\overline{V_{lead}}$ is active, V_D increases during Δt. Conversely when V_{lag} is active, V_D decreases instead.

When $\overline{V_{lead}}$ is active, the current I_D charging up the capacitor is determined by V_D. I_D is also equal to the capacitive current through the capacitor C_b. In subthreshold operation, I_D can be expressed as (V_D here is referenced to V_{dd}):

$$I_D = I_0 e^{-\frac{\kappa V_D}{U_T}} = C_b \frac{dV_D}{dt} \qquad (1)$$

where I_0 is the leakage current, κ is $\frac{C_{ox}}{C_d + C_{ox}}$, C_{ox} is the gate oxide capacitance and C_d is the depletion layer capacitance[2].

Let t_{d0} be the initial delay through the delay element.

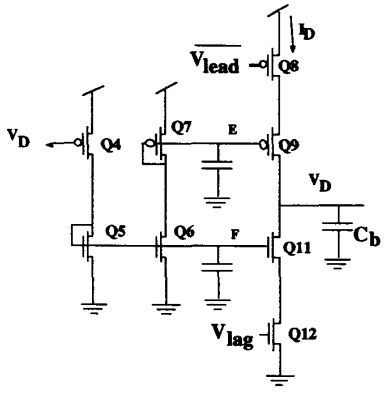

Figure 4: Charge pump used in the adaptive delay system. This circuit uses the error signals, V_{lead} or V_{lag}, to correct the bias voltage, V_D. The update of V_D depends on the duration of the error signals and on the current source controlled by V_D.

Integrating both sides of equation 1, we get

$$\int dt = \int \frac{C_b dV_D}{I_D}$$

$$\Delta t = \int \frac{C_b}{I_0 e^{-\frac{\kappa V_D}{U_T}}} dV_D \quad (2)$$

$$= \frac{C_b U_T}{\kappa}[1/I_{D1} - 1/I_{D0}] \quad (3)$$

where Δt is the duration of $\overline{V_{lead}}$, I_{D1} is the charging current in the delay element with bias voltage V_{D1} and I_{D0} is the charging current with bias voltage V_{D0}. The bias voltage, V_{D1} creates a new delay through the delay element, t_{d1}. We substitute t_{d1} and t_{d0} using the relationship derived in equation 6 in the variable delay element section into the above equation to get:

$$\Delta t = \frac{C_b U_T}{\kappa C_a V_{dd}}[t_{d1} - t_{d0}]$$

This equation allows us to express a relationship between the initial and final delays after the duration Δt.

$$t_{d1} = t_{d0} + \Delta t \frac{\kappa C_a V_{dd}}{C_b U_T} = t_{d0} + \gamma \Delta t \quad (4)$$

where $\gamma = \frac{C_a V_{dd} \kappa}{C_b U_T}$. Ideally, we should set $\gamma = 1$ for optimal response and no overshoot. The precision with which we can control γ is limited by the repeatibility of C_a, C_b, κ and U_T. Obviously if $\gamma > 1$, the system is over-corrected and we would observe overshoots in the correction of the bias voltage.

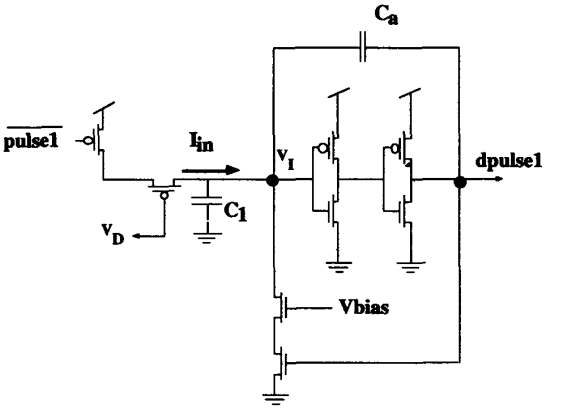

Figure 5: Variable delay element used in adaptive delay system. The delay is controlled by V_D.

Variable Delay Element

Initially, the output of the delay element, *dpulse*1, is at ground. Assume that V_I must increase by ΔV_I before the delay element fires (i.e. *dpulse*1 goes to V_{dd}). The delay, t_d, through this element, which is the time before *dpulse*1 switches from ground to V_{dd}, can be described by:

$$t_d = \frac{\Delta V_I}{dV_D/dt} \quad (5)$$

The rate at which V_I increases depend on the charging current, I_{in}, i.e, $I_{in} = C\frac{dV_I}{dt}$ where C in this case is $C_a + C_1$. The final value of ΔV_I before the delay element fires is $(C_a V_{dd})/(C_a + C_1)$. Substituting this expression back into equation 5, we get:

$$t_d = \frac{\frac{C_a V_{dd}}{C}}{\frac{I_{in}}{C}} = \frac{C_a V_{dd}}{I_{in}} \quad (6)$$

Experimental Results

When the system is operating at steady state, t_{d0} is equal to the input temporal disparity, t_{i0}. If the input temporal disparity increases from t_{i0} to t_{if}, the change in input temporal disparity, Δt_0, is equal to $t_{if} - t_{i0} = t_{if} - t_{d0}$. The error signal on the nth iteration, Δt_n, tells us the error between the new input temporal disparity and the updated delay, $t_{if} - t_{dn}$. Δt_n is a geometric decay of Δt_0 as shown below:

$$\Delta t_n = (1-\gamma)^n \Delta t_0 \quad (7)$$

t_{dn} on the nth iteration is given by:

$$t_{dn} = t_{d0}(1-\gamma)^n + t_{if}(1-(1-\gamma)^n) \quad (8)$$

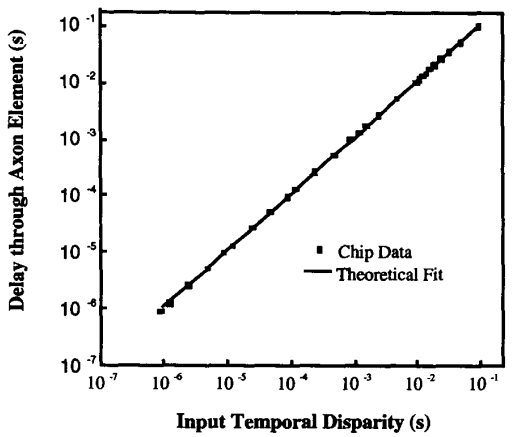

Figure 6: Measured delay through delay element as a function of input temporal disparity for system shown in Figure 1. The theoretical fit has a slope of one. The data shows a match over 5 decades.

From equation 7, we observe that the error decreases geometrically as n increases, i.e., $\lim_{n\to\infty} \Delta t_n = 0, \lim_{n\to\infty} t_{dn} = t_{if}$. From equation 8, we see that t_{dn} approaches t_{if} as the number of iterations increases. We can get the updated bias voltage, V_{Dn}, on the nth iteration by substituting the expression from equation 2 into equation 8,

$$V_{Dn} = V_{D0} + U_T \frac{\ln\left(\beta^n + e^{\kappa(V_{Df}-V_{D0})/U_T}(1-\beta^n)\right)}{\kappa} \quad (9)$$

where V_{Df} is the bias voltage corresponding to the delay, t_{if} and $\beta = (1-\gamma)$.

In the first experiment, we supplied two input signals, *pulse*1 and *pulse*2 with varying input temporal disparities to the system. For each t_i, the signals were repeated for several iterations. The interval, t_d, was measured when the system reaches steady-state. Figure 6 shows the log-log plot of t_d versus t_i. The points on the graph are the experimental data while the solid line is $t_d = t_i$. The adaptation happens over a range of 5 decades from $1\mu s$ to $0.1s$.

Next, we look at how V_D changes over time when a sudden change in t_i occurs. In this experiment, we provide 2 input clocks with a temporal disparity of $20\mu s$ between *pulse*1 and *pulse*2 and decreased t_i by 10%. Since the input signals are presented over and over again, we can monitor the temporal change of V_D. Figure 7 shows the monotonic increase in ΔV_D as V_D approaches its steady-state value. This experimental data shows that this system is stable. The smooth line in Figure 7 shows the theoretical fit through the experimental data. From this fit, γ is about 0.03 which correlates well with the value

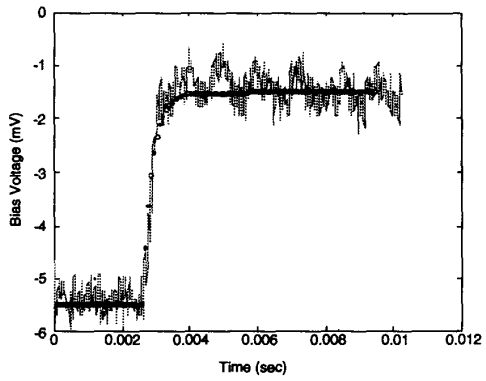

Figure 7: Change in bias voltage over time for a 10% change in delay contrast ratio.

computed from $\gamma = \frac{C_a V_{dd} \kappa}{C_b U_T}$.

Conclusion

We have developed an adaptive system that adjusts its delay through continuous-time adaptation to the temporal disparity between two input signals. The bias voltage to the delay element adapts monotonically towards the final steady-state value corresponding to the new input temporal disparity. It does not show the overshoots exhibited by conventional phase-locked loop systems. The system changes its adaptation dynamics depending on the delay contrast ratio in such a way that they are independent of the input temporal disparity itself. The new adaptation dynamics allow the system to have a lock-in range of over 5 decades in delay.

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References

[1] Gardner, Floyd M.,"Charge-Pump Phase-Lock Loops", *IEEE Transactions on Communications*, COM-32, pp.1849-1858, 1980.

[2] Mead, C., *Analog VLSI and Neural Systems*, Addison-Wesley, 1989.