Continuous-Time Adaptive Delay System

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***Abstract*—We have developed a direction-selective system that has a row of pixels with photodiodes as the front-end. The output of each photodiode is converted to a digital signal, which is then fed to an adaptive-delay block within each pixel. The adaptive block adjusts an internal delay such that the delay matches the phase offset between the rising edges of this digital signal and the corresponding digital signal from the neighboring pixel. The system does this delay matching by using a dynamic current source to adapt the bias voltage that controls the delay. The adaptive-delay block is similar to a digital charge-pump phase-lock loop (PLL). It differs from conventional PLL's however, both in its compact size and its lack of a system clock. It also has a fast pull-in time during the locking of the signal. Since our application does not require low jitter, we have not introduced a phase offset in the comparator as is typically done in PLL's. The transistors here are operated in subthreshold. A stability analysis of the feedback system leads to simple stability and convergence constraints. Experimental results from circuits fabricated in 2 μm CMOS technology show that the circuit can lock over 5 decades of frequency.**

I. Introduction

We describe a direction-selective system that has a row of pixels with photodiodes as the front-end. The photodiode at each pixel transduces the incoming input intensity into a current, which is converted to a digital signal that is fed to an adaptive-delay block within the pixel. The adaptive block adjusts an internal delay such that the delay matches the phase offset between the rising edges of the digital signal and the corresponding digital signal from the neighboring pixel. The delay matching occurs over 5 decades of frequency.

The direction-selective computation is based on a delay-and-compare model of the optomotor response of a bee [1]. In the model, the input signal from each photoreceptor is delayed through a low-pass filter. The subsequent delayed signal from each pixel location is correlated with the input signal from the neighboring photoreceptor. The direction of motion of the input signal can be extracted through this model. We can extend the dynamic range of the system by having the time constant of the low-pass filter track the speed of the signal. Since the input speeds can vary over 3 decades, the system needs to continuously adapt the time constant of the low-pass filter to the varying speed of the stimulus. The signal from the photodiode is first converted to a digital signal before it goes through the adaptive-delay block which implements the low-pass filter. In this paper, we only focus on the adaptive delay part of the system with digital signals as inputs.

The architecture of the adaptive-delay block is similar to that of a digital charge-pump PLL. The properties, applications, and analyses of phase-locked systems are well known [2]–[9]. However, the requirements for our direction-selective system are different from those of a typical PLL. First, we are constrained to use as few transistors as possible, to minimize pixel area. Second, we are interested in input frequencies in the range from hertz to kilohertz, which encompasses the range for moving objects in a natural scene. Third, since the range of input frequencies can vary over three decades, we cannot tune the system for a particular frequency. Fourth, we would like the system to continuously adapt the time constant of the low-pass filter so that we can get a large dynamic range. Fifth, we would like a fast pull-in time for the locking since the input frequencies are constantly changing. Sixth, we require the absence of a master clock since the system is a model of a biological computation. Since our application does not require low jitter and we want to keep the system compact, we have not added a phase offset in the comparator, as is done in typical PLL's.

The subunits of the adaptive delay system are similar to those in PLL's. The three components are the lead–lag discriminator, the delay element (which emulates a low-pass filter) and the charge pump. The lead–lag discriminator and the delay element are functionally equivalent to the phase detector and voltage-controlled oscillator (VCO), respectively, in a PLL. The lead–lag discriminator generates an error signal proportional to the phase offset between the rising edges of two signals. The delay through the delay element is controlled by a bias voltage on a capacitor. The charge pump charges or discharges this capacitor, depending on both the lead–lag error signal and on the bias voltage itself. The charge pump is different from that found in a typical PLL. In a charge-pump PLL, the charging or discharging of the VCO bias voltage is normally done with a fixed current source. Our system uses a dynamic current source, controlled by the bias voltage in the charge pump. The current source enables the system to adapt to input frequencies over 5 decades. The progression of the bias voltage to its final steady-state value occurs monotonically, and we can adjust the gain of the system by controlling the percentage of correction for the bias voltage in each input time period.

We fabricated the circuit in 2 μm p-well CMOS ORBIT process. Section II describes the circuitries of the lead–lag discriminator, of the delay element, and of the charge pump. Section III describes the convergence properties of the system; and the steady-state and transient responses obtained from the

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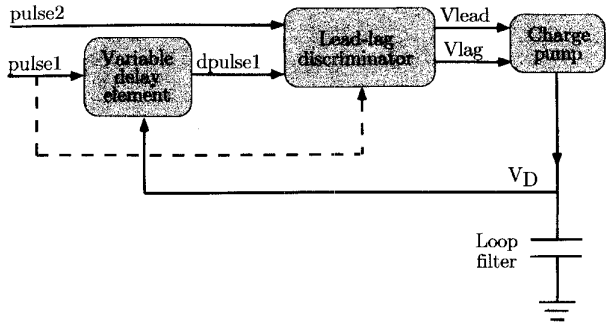

Fig. 1. Block diagram of the adaptive delay system. All signals are pulses (continuous time, discrete level) except for the bias voltage,V_D. The signal $pulse1$ is the leading input signal. $dpulse1$ is the delayed copy of $pulse1$ after going through the variable delay element. The signal $pulse2$ is the trailing input signal. The system uses the arrival of $pulse1$ to match the timing of $dpulse1$ with that of $pulse2$. If the timing is not matched, the system uses the error signals V_{lead} or V_{lag} to adjust the delay of the variable delay element.

fabricated chip. In Section IV, we show a possible application of this system in an adaptive delay line. Burt and Wallinga [12] previously described a delay line where the time constant of the line is controlled by the output of a delay element, instead of by the output of a VCO in a PLL. We show here how this delay element can be replaced by our adaptive-delay block to increase the system's dynamic range.

II. Architectural Model

A block diagram of the adaptive delay system is shown in Fig. 1. The input signals consist of the digital signal from the photodiode within the pixel and the corresponding digital signal from the neighboring pixel. The relative signal timing is shown in Fig. 2. The signals are all discrete-level, continuous-time pulses, except for the bias voltage V_D. The signal $pulse1$ is the leading input signal and $pulse2$ is the trailing input signal. The interval t_i is the input phase offset. The signal $dpulse1$ is a delayed copy of $pulse1$, where the variable delay of the element t_d (which we also call the delay phase offset) is controlled by V_D. The interval Δt is the absolute time difference between t_d and t_i.($pulse2$ and $dpulse1$ are maximally correlated when $t_d = t_i$ or when $\Delta t = 0$). Circuits using the signals $pulse1, pulse2$, and $dpulse1$ are leading-edge triggered. The lead–lag discriminator in Fig. 1 compares the arrival of $dpulse1$ with that of $pulse2$ and outputs an error signal V_{lead} or V_{lag} if the signals are not phase aligned. We use V_{lead} and V_{lag} to correct V_D in the charge pump block in Fig. 1. This change in V_D is reflected as a change in t_d of the variable delay element, so that t_d approaches t_i.

A. Lead–Lag Discriminator

The lead–lag discriminator circuit shown in Fig. 3 computes the time difference Δt between the delay through the delay element t_d and the input phase offset t_i. The signal V_{lag} becomes active for the duration Δt when $t_d > t_i$, and V_{lead} becomes active for the duration Δt when $t_d < t_i$.

First, we consider the circuit that creates V_{lag}. The initial voltage at node C is close to V_{dd} due to the leakage current flowing through Q3. The arrival of $pulse1$ triggers the delay element (as shown in Fig. 1) and, at the same time, charges node A by pulling down node C capacitively. Node B does not go low until $pulse2$ arrives. If $dpulse1$ arrives before $pulse2$, node A is discharged to ground and thus node B is prevented from switching. Hence, V_{lag} remains low. Since the circuit is symmetric, V_{lead} becomes active. However, if $pulse2$ comes before $dpulse1$, node B goes low and V_{lag} goes high. V_{lag} is high for the period Δt. When $pulse1$ goes high (i.e., $pulse1$ goes low), node C is pulled high capacitively. However if V_{lead} becomes active before $pulse1$ becomes inactive, then node C will already be at V_{dd} when $pulse1$ becomes inactive. Node C will temporarily rise above V_{dd} but the parasitic vertical bipolar transistor formed by the drain of Q3 and its well and substrate will turn on thus returning node C to V_{dd}.

Q1 and Q2 prevent V_{lag} and V_{lead} from being active at the same time. This situation might happen if $dpulse1$ did not arrive until the second occurrence of $pulse1$. To prevent both signals from being active simultaneously, if initially V_{lead} is active, Q2 turns on and the current through Q1 is mirrored in Q3. This current charges up node C, thus preventing node C from being pulled low with the second occurrence of $pulse1$.

B. Variable Delay Element

The delay element circuit is shown in Fig. 4. This circuit was described by Mead [11]. Initially, $dpulse1$ is low. When $pulse1$ becomes active, I_{in} charges C_1 by ΔV_I until $dpulse1$ triggers. The delay t_d from node V_I to $dpulse1$ can be described by

$$t_d = \frac{\Delta V_I}{dV_I/dt}. \tag{1}$$

The slew rate at node V_I depends on the charging current, $I_{\text{in}} = C(dV_I/dt)$, where $C = C_a + C_1$. The value of ΔV_I before the delay element fires can be computed from C_a/C, with $dpulse1$ acting as the voltage input to the divider. Thus, ΔV_I is $(C_a V_{dd})/C$. Substituting this expression into (1), we get

$$t_d = \frac{\frac{C_a V_{dd}}{C}}{\frac{I_{\text{in}}}{C}} = \frac{C_a V_{dd}}{I_{\text{in}}}. \tag{2}$$

This delay element is operated in the subthreshold regime [11], so I_{in} depends on V_D through the exponential relationship, $I_{\text{in}} = I_0 e^{-(\kappa(V_D - V_{dd})/U_T)}$, where I_0 is the leakage current, κ is $C_{\text{ox}}/(C_d + C_{\text{ox}})$, C_{ox} is the gate-oxide capacitance, C_d is the surface-channel depletion-layer capacitance, and U_T is the thermal voltage.

C. Charge Pump

The *charge pump* is shown in Fig. 5. Its function is to adjust V_D such that t_d approaches t_i. The circuit of Fig. 5 is functionally similar to the typical charge pumps used in digital PLL's with one important difference. In the charge pump of a typical PLL, a fixed current source is used to charge or discharge the capacitor. Here a dynamic current source controlled by V_D itself is used to update V_D.

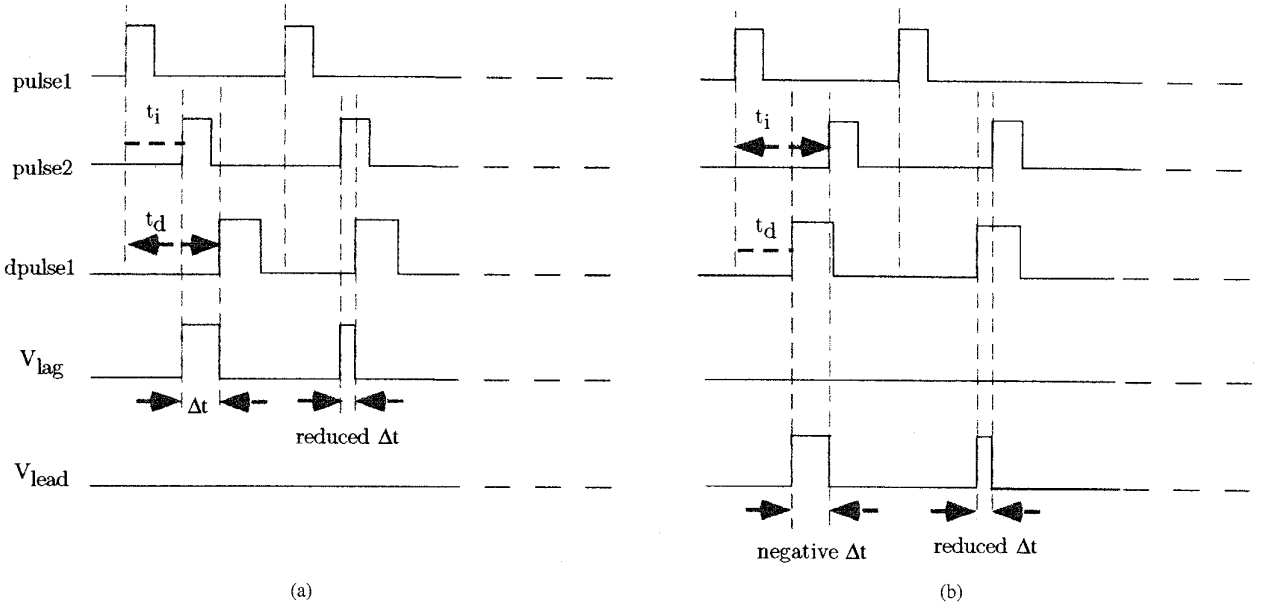

Fig. 2. Signal timing showing loop correction and overshoot across several pulses. The input signals $pulse1$, $pulse2$, and $dpulse1$ are edge triggered. The interval t_i is the input phase offset between $pulse1$ and $pulse2$. The interval t_d is the delay phase offset between $pulse1$ and $dpulse1$. The system adapts t_d to match t_i. (a) V_{lag} is the output error signal when $t_d > t_i$. (b) V_{lead} is the output error signal when $t_d < t_i$.

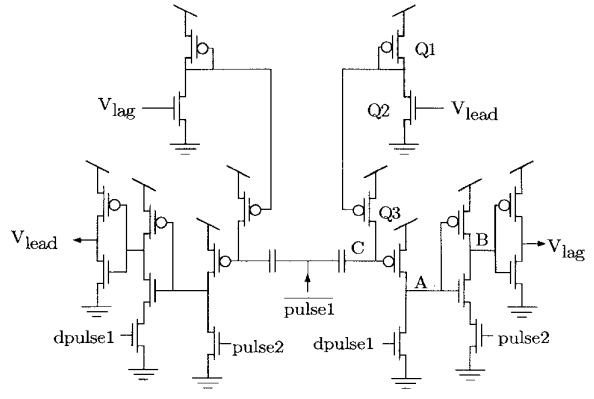

Fig. 3. Lead–lag discriminator. The circuit generates the error signals, V_{lead} and V_{lag}, which are used in the charge-pump circuit. $pulse1$ is active low whereas the other input signals in the diagram are active high.

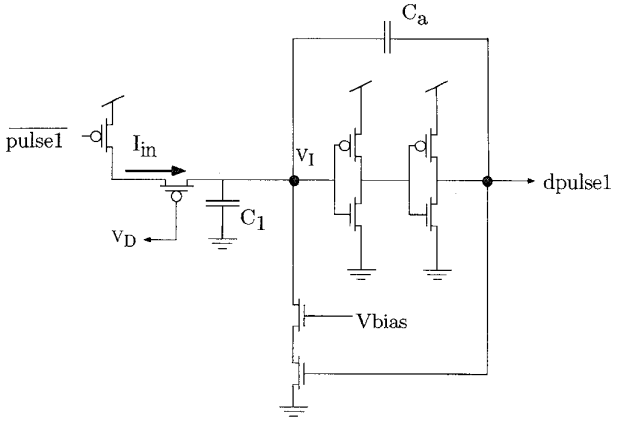

Fig. 4. Variable delay element. The delay is controlled by V_D. The output signal $dpulse1$ is a delayed version of $pulse1$. The signal $\overline{pulse1}$ is active low.

The circuit in Fig. 5 operates as follows. Q4's channel current is equal to the current I_{in} in the delay element, since both are biased by V_D (assuming no mismatches). This current is mirrored through Q5 into Q11, and then through transistors Q6 and Q7 into Q9. Q8 and Q12 act as switches. If V_{lead} is active, V_D increases during Δt. If V_{lag} is active, V_D decreases instead. Assuming that the time constant due to the parasitic capacitance at node F is much smaller than that due to the charging capacitor C_b, we can reduce the circuit in Fig. 5 to the first-order system shown in Fig. 6. There is a possibility that V_D starts off at V_{dd} after the system is reset. However during the interval when V_{lag} is active, the leakage current through transistors Q11 and Q12 will discharge V_D until the delay element is triggered.

III. Convergence Properties of the System

A. Stability Analysis

Asymmetry in the charge-pump dynamics for both a positive phase error Δt or a negative phase error is present in the circuit. In the case of a negative phase error, $dpulse1$ leads $pulse2$, and V_{lead} becomes active. The current through Q9 in Fig. 5 is equivalent to the current flowing in the delay element. As V_D increases, the currents through Q7 and Q9 decrease. The charging rate of V_D decreases as V_D increases.

During any one interval when V_{lead} is active, we can treat the circuit as a linear, time-invariant network, and can describe the network by linear difference equations. The following analysis describes the charge-pump operation during

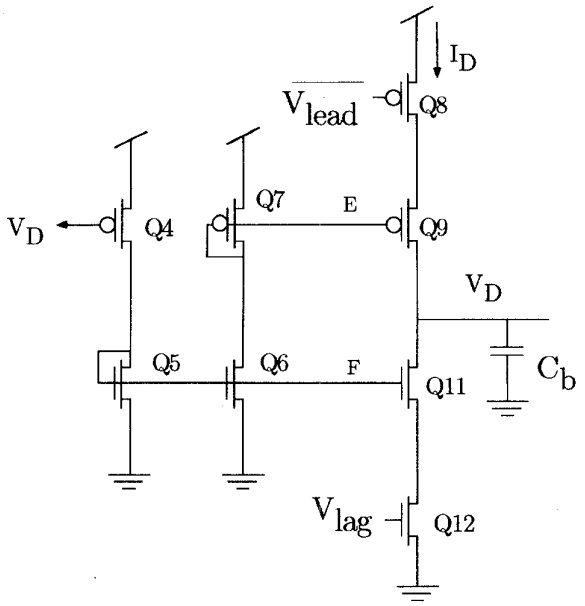

Fig. 5. Charge pump. This circuit uses the error signals $V_{\rm lead}$ or $V_{\rm lag}$ to correct the bias voltage V_D. The correction is different from typical charge-pump PLL's, which use a fixed current source to update the bias voltage. The adaptive delay system uses a dynamic current source, which depends on V_D.

this interval Δt. We assume that $t = 0$ at the time when there is a step change in the phase offset between $pulse1$ and $pulse2$. The charging current I_D is determined by V_D. Writing the KCL equation at node V_D in Fig. 6 and noting that the transistors are operated in subthreshold operation, we can express I_D as

$$I_D = I_0 e^{-(\kappa(V_D - V_{dd})/U_T)} = C_b \frac{dV_D}{dt}. \tag{3}$$

Integrating (3), we get

$$\begin{aligned}\Delta t &= \int \frac{C_b}{I_0 e^{-(\kappa(V_D - v_{dd})/U_T)}} dV_D \\ &= \frac{C_b U_T}{\kappa} [1/I_{D1} - 1/I_{D0}] \end{aligned} \tag{4}$$

where Δt is the duration of $V_{\rm lead}$, $I_D(0)$ is the charging current at $t = 0$, and $I_D(\Delta t)$ is the new charging current at $t = \Delta t$. (Recall that the system adapts V_D so that $\Delta t = 0$). Since the current charging the delay element is equal to I_D, the increase in I_D leads to a new delay through the delay element. We denote $t_d(\Delta t)$ as the delay at $t = \Delta t$, and $t_d(0)$ as the initial delay. Using (2), we substitute $t_d(\Delta t)$ and $t_d(0)$ into (4) to get

$$\Delta t = \frac{C_b U_T}{\kappa C_a V_{dd}} [t_d(\Delta t) - t_d(0)]. \tag{5}$$

This equation allows us to relate the initial and final delays to the period Δt.

$$t_d(\Delta t) = t_d(0) + \Delta t \frac{\kappa C_a V_{dd}}{C_b U_T} = t_d(0) + \gamma \Delta t \tag{6}$$

where $\gamma = C_a V_{dd} \kappa / C_b U_T$. We can rewrite (6) in terms of the new input phase error, Δt_1, after the switching interval of $V_{\rm lead}$.

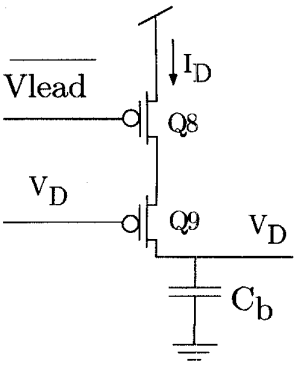

Fig. 6. Equivalent circuit model of the charge pump in Fig. 5. We use this model in deriving (6).

$$\Delta t_1 = (1 - \gamma)\Delta t(0) \tag{7}$$

Here we can see that the new phase-error offset is a fraction of the original phase offset if $\gamma < 1$. We now generalize (6) and (7) to see how the phase error changes over n switching intervals of $V_{\rm lead}$, that is, how the system adapts t_d to t_i such that $\Delta t \to 0$ over time. We define the first switching interval of $V_{\rm lead}$ after a step change in the phase-error offset as $n = 0$. Hence, $t_d[0]$ is the delay through the delay element and t_i is the new input phase offset at the start of the first interval. $\Delta t[0]$ is the phase error offset due to the change in t_i. The delay through the delay element on the nth iteration $t_d[n]$ is given by

$$t_d[n] = t_d[0](1 - \gamma)^n + t_i(1 - (1 - \gamma)^n). \tag{8}$$

The phase error offset signal $\Delta t[n]$ can be shown to be a geometric decay of $\Delta t[0]$ from (7).

$$\Delta t[n] = (1 - \gamma)^n \Delta t[0]. \tag{9}$$

The series relationship in (9) converges if $\gamma < 1$. Hence, the error decreases geometrically as n increases; that is, $\lim_{n\to\infty} \Delta t[n] = 0, \lim_{n\to\infty} t_d[n] = t_i$.

The convergence of the system can also be seen by taking the z-transform of (9)

$$\Delta t(z) = \frac{\Delta t[0](z)}{1 - (1 - \gamma)z^{-1}}.$$

The pole of this system falls at $z = 1 - \gamma$. For the system to be stable, the pole should fall within the unit circle, i.e. ($\gamma < 1$). If $\gamma > 1$, the system is under damped and we will observe overshoots and undershoots in the phase error offset correction. Another way of looking at γ is that γ sets the amount of correction of the input phase error within one interval of $V_{\rm lead}$ switching. If $\gamma = 1$, then the error is totally corrected for in one interval after the phase error is first encountered. To ensure stability of the system, we should set the ratio, C_a/C_b such that $\gamma < 1$. The precision with which we can control γ is limited by the matching of C_a, C_b, κ, and U_T. We can also control γ by adjusting the sizing of the current mirror composed of Q5 and Q6.

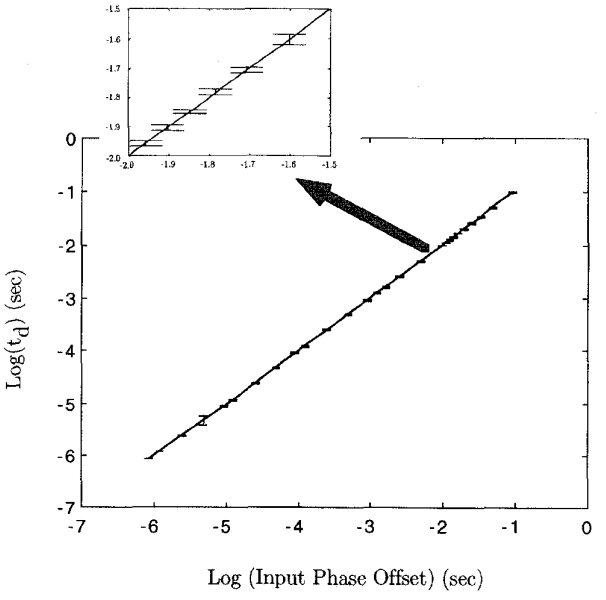

Fig. 7. Measured delay through delay element as a function of input phase offset for system shown in Fig. 1. The percentage error in t_d varies from 2 to 6.67%. The inset shows an expanded view of the error bars at the data points. The data show a match between t_d and t_i over 5 decades.

In the case of a positive phase error, $pulse2$ leads $dpulse1$, and V_{lag} becomes active. Since V_{lag} is active once $pulse2$ arrives, t_d decreases continuously until $dpulse1$ becomes active. This scenario differs from the negative phase error situation, where t_d changes only after $dpulse1$ is active. Hence, the correction on V_D is not observed until the next switching interval when V_{lead} is again active. The current through Q11 in Fig. 5 is equivalent to the charging current in the delay element. As V_D decreases, the current through Q5 and Q11 increases. The rate at which V_D discharges increases as V_D decreases.

The corresponding equations for t_d and Δt after one switching interval of V_{lag} are

$$\Delta t = t_d(\Delta t) - t_i$$
$$t_d(\Delta t) = t_d(0) - \gamma \Delta t.$$

Fig. 7 shows the steady-state data that are obtained from the fabricated circuit in Fig. 1 by allowing the system to adapt t_d to t_i. The signals $pulse1$ and $pulse2$ are both periodic signals, with $pulse2$ shifted half a period from $pulse1$. We used periodic signals so that we can track the system adaptation over several cycles. The delay, t_d, was measured when the system reached steady state for t_i varying over 5 decades. We varied t_i by changing the frequency of the periodic signals $pulse1$ and $pulse2$ over 5 decades. The percentage error in t_d varied from 2 to 6.67% The inset shows an expanded view of the error bars at the data points. The relationship between t_d and t_i is linear as shown in the derivation of (6) and (7). If we rederive those equations for above-threshold transistor operation (i.e., square-law behavior), we find that the change in t_d at each iteration is a function both of the error, Δt, and of the delay itself, t_d. This relationship does not lead to a linear dependence between t_d and t_i. The linear dependence

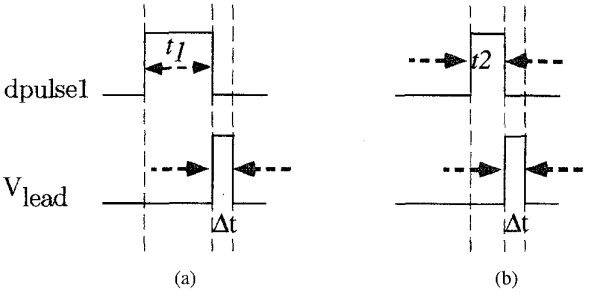

Fig. 8. Importance of the delay-contrast ratio in determining the charge pump source-current magnitude. In (a) the error signal, Δt is only a small fraction of the actual delay, t_1. In (b) Δt is a larger fraction of t_2. Hence, in (a) the current source in the charge pump circuit should be smaller in magnitude than the current source in (b).

obtained in Fig. 7 occurs in the range of low frequencies; in the hertz to megahertz range, which encompasses the range of interest for our direction-selective system. We can shift the range of frequencies higher by using bipolar transistors or stronger FET's in the system.

B. Charge-Pump Dynamics

We shall analyze how the circuit dynamics differ when we use a fixed current source in the charge pump, as is done in typical PLL's and when we use a dynamic current source that is dependent on V_D. We first look at how the change in V_D depends both on the error offset Δt and on t_d. Rewriting (2) so we can solve for V_D

$$V_D = \frac{U_T}{\kappa} \ln\left(\frac{t_d I_0}{C_a V_{dd}}\right). \tag{10}$$

From (10) we see that V_D is logarithmically dependent on t_d. Taking the differential on both sides of (10), we get

$$\Delta V_D = \frac{U_T}{\kappa} \frac{\Delta t}{t_d}. \tag{11}$$

Equation (11) shows that the change in V_D depends on the *delay–contrast ratio* $\Delta t/t_d$. This ratio is important because, for a given Δt error, the amount of correction of V_D should also depend on the existing delay, t_d. The importance of this ratio is shown in Fig. 8. If a fixed current source is used in the charge pump, then the change in V_D is dependent on only Δt. However, if Δt is a small percentage error in t_d, then we want the V_D correction to be smaller than it is when Δt is a large percentage error of t_d. The relationship in (11) comes about because of the exponential property of a transistor in subthreshold. The use of a current source which is exponentially dependent on V_D allows the system to match t_d with t_i monotonically over a wide range of t_i.

We obtain the updated bias voltage $V_D[n]$ at the start of the nth switching interval in the case of the negative-phase error offset by substituting (10) into (8)

$$V_D[n] = V_D[0] + U_T \cdot \frac{\ln((1-\gamma)^n + e^{\kappa(V_{Df} - V_D[0])/U_T}(1-(1-\gamma)^n))}{\kappa} \tag{12}$$

where V_{Df} is the bias voltage corresponding to the input phase offset t_i.

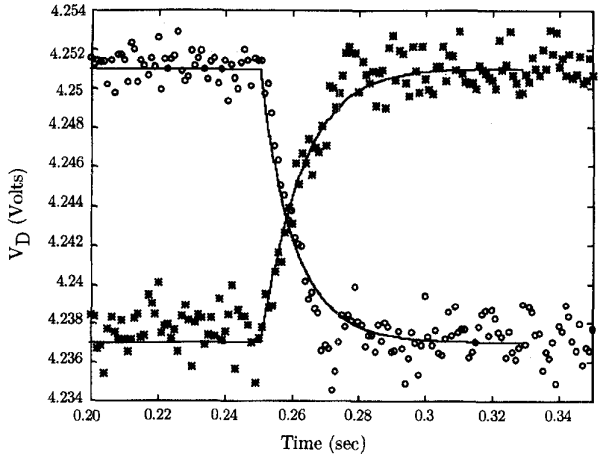

Fig. 9. Change in V_D following a 30% change in delay-contrast ratio. The curve marked with circles is the bias voltage adaptation for a step decrease in t_i; the curve marked with asterisks is the bias voltage adaptation for a step increase in t_i. The solid line is a fit to the data using (12).

The corresponding equation for a positive-phase offset error is

$$V_D[n] = V_D[0] - U_T \cdot \frac{\ln\left(\frac{1}{(1+\gamma)^n} + e^{\kappa(V_D[0]-V_{Df})/U_T}\left(1 - \frac{1}{(1+\gamma)^n}\right)\right)}{\kappa}.$$

C. Transient Response

In this section, we describe how V_D evolves over time following a step change in t_i. Fig. 9 shows the adaptation of V_D from the fabricated chip to a step increase and a step decrease in t_i. Here again, $pulse1$ and $pulse2$ consist of two square-wave periodic signals with $pulse2$ shifted by half a period. t_i is initially 97 μs. We then decrease t_i by 30%. The curve marked with circles follows the updating of V_D to this step decrease in t_i. Correspondingly, the curve marked with asterisks shows how V_D changes over time to a 30% step increase in the same initial t_i. The data show that the system is over damped. The solid lines in Fig. 9 are the theoretical fits obtained from (12). From these fits, γ is about 0.03, which correlates well with the theoretical value computed from $\gamma = (C_a V_{dd}\kappa)/(C_b U_T)$.

Next, we measured the final change in $V_D, \Delta V_D$, to different step changes in t_i. Fig. 10 shows that ΔV_D is linearly dependent on $\Delta t/t_d$. This relationship is derived in (11). Fig. 11 shows that ΔV_D is independent of t_i with a fixed delay-contrast ratio $\Delta t/t_d$.

Fig. 12 shows measured data from the chip following a 18% increase in t_i for three different t_i. We see that the final change in V_D is equal in all three cases and that the number of iterations to reach the final V_D is also the same. This response is easily inferred from (12). The solid line shows the actual data; the circles show the theoretical fit through the data. This behavior is exhibited over 5 decades of frequency.

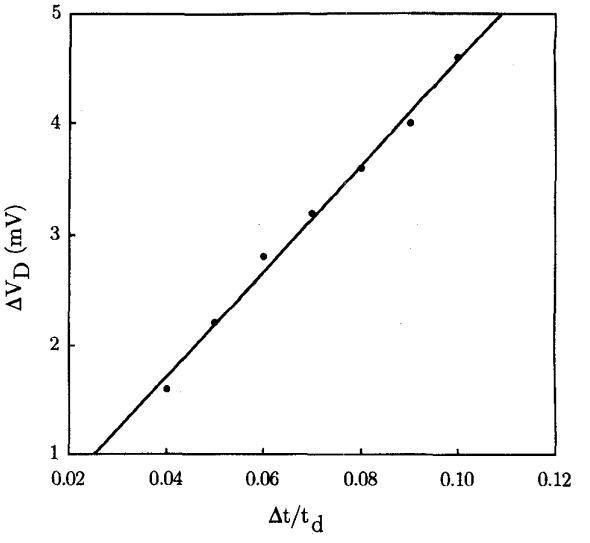

Fig. 10. Change in V_D versus delay-contrast ratio $\Delta t/t_d$ for a fixed t_i. The graph shows that the circuit adapts t_d according to the delay-contrast ratio, rather than to the offset error Δt. This feature allows the circuit to adapt monotonically to the change in the input phase offset.

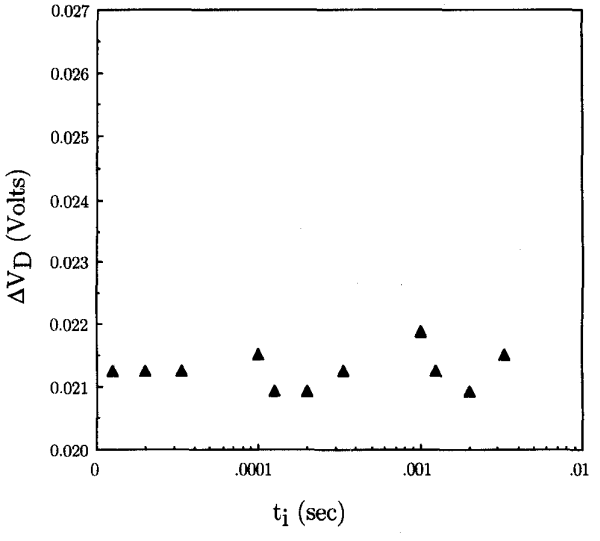

Fig. 11. Change in V_D versus t_i for a fixed delay-contrast ratio $\Delta t/t_d$. The graph shows that the change in V_D is independent of t_i for a fixed delay-contrast ratio.

IV. Discussion

Our adaptive-delay block can be used in a wide range of applications. Fig. 13 shows an example where the delay block controls the bias voltage to an analog delay line, which can be used in many signal processing applications. The time constant of the delay line is normally tuned to an external reference frequency by using a PLL. In [12], Bult and Wallinga showed how the time constant can be tuned by replacing the VCO in the PLL with a delay element. The output of the delay element is now used as the reference signal instead of the VCO output. Their adaptive delay control works over only 2 octaves in frequency since the system has the same limitations as the system dynamics in a PLL. If we replace their delay

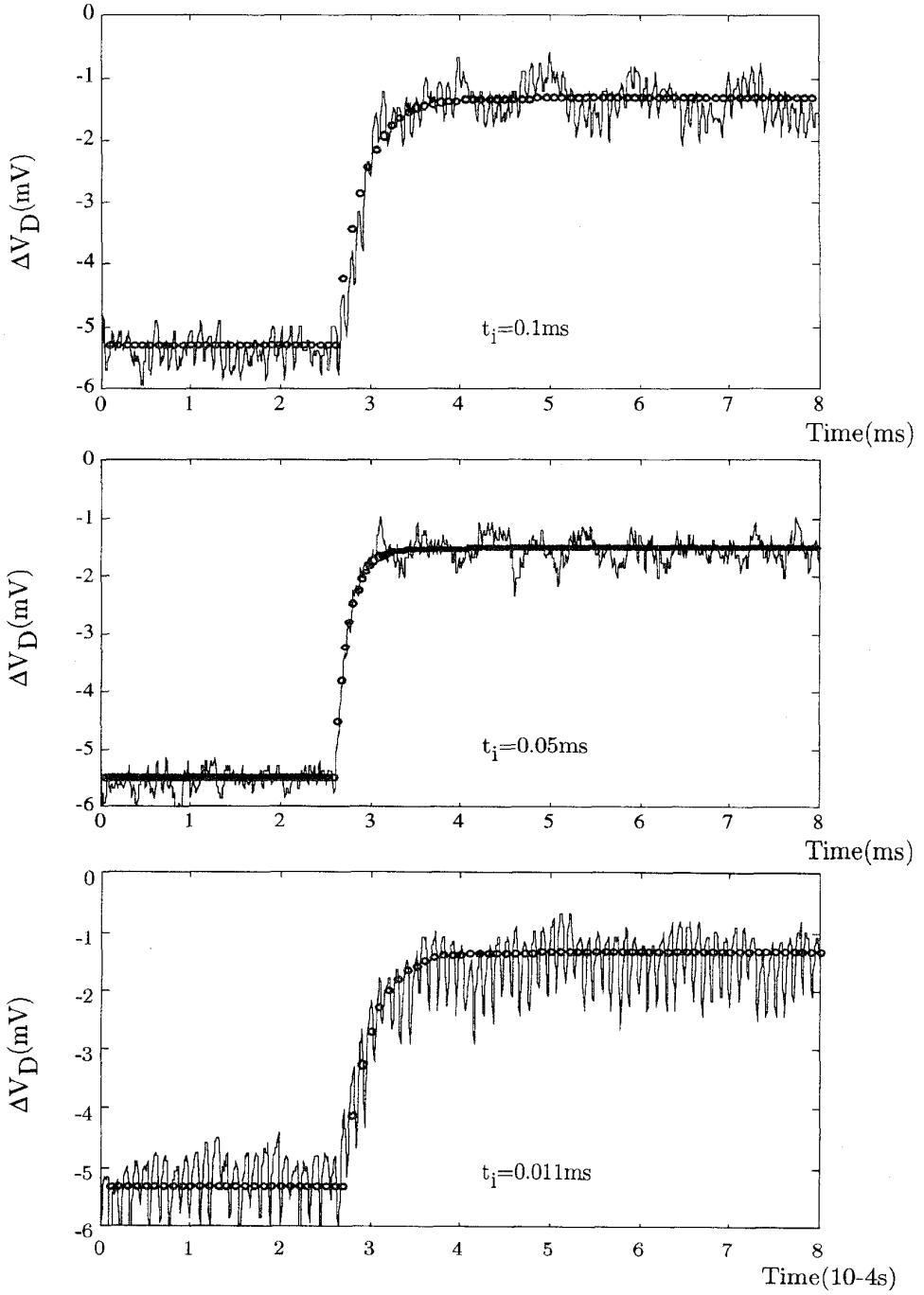

Fig. 12. Change in V_D following an 18% increase in t_i for three different values of t_i. The solid line shows measured chip data. The noise riding on top of the curve is due to clock coupling into the test setup. The circles show the theoretical fit through the data.

element with our adaptive-delay block, we can increase the adaptive control to over 5 decades in frequency.

V. Conclusion

We described an adaptive delay block which is part of the circuitry at each pixel in a direction-selective system that extracts the direction of motion of moving objects. The adaptive block adapts an internal delay to match the input phase offset between two input signals. The data matching between the internal delay and the input phase offset occurs over 5 decades of frequency. We make this extended pull-in frequency range possible by using a dynamic current source in the charge pump and using the exponential property of transistors operating in subthreshold. Since we do not require low jitter in our application, we have not included an offset

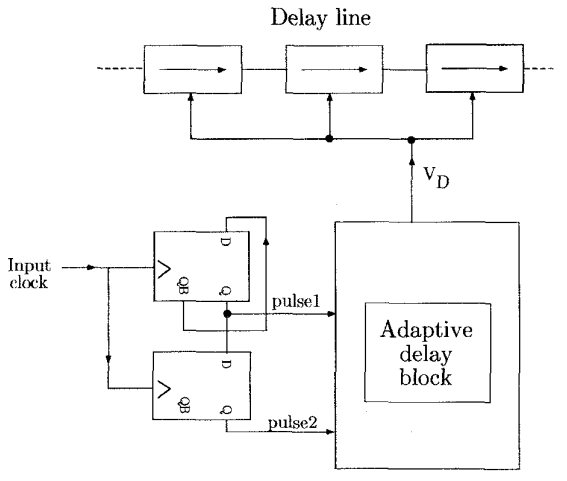

Fig. 13. Block diagram of a continuous delay line whose delay is tuned to the period of an incoming signal using the adaptive delay system. The use of a VCO is eliminated.

in the comparator circuit even though we could can easily do so. It also helps to keep our goal of keeping the system compact by excluding the circuit for low jitter. We showed that the system is stable over 5 decades of frequency without adjusting the system parameters and has a fast pull-in time during locking. The adaptive-delay block works well for our direction-selective system and has the potential for other applications.

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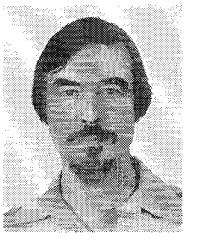

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