128-Bit Multicomparator

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Abstract—A 128-bit multicomparator was designed to perform the search-sort function on arbitrary length data strings. Devices can be cascaded for longer block lengths or paralleled for bit-parallel, word-serial applications. The circuit utilizes a 3-phase static-dynamic shift register cell for data handling and a unique gated EXCLUSIVE-NOR circuit to accomplish the compare function. The compare operation is performed bit parallel between a "data" register and a "key" register with a third "mask" register containing DON'T CARE bits that disable the comparator. The multicomparator was fabricated using p-channel silicon-gate metal-oxide-semiconductor (MOS) technology on a 107 × 150 mil chip containing 3350 devices. With transistor-transistor logic (TTL) input, data rates in excess of 2 MHz have been attained. The average power dissipation was 250 mW in the dynamic mode and 300 mW in the static mode.

INTRODUCTION

OVER the past several years, there have been significant amounts of energy devoted to the fabrication of larger and faster semiconductor memories and conventional central processing units (CPU's) in chip form. In the process, many other applications of large-scale integration (LSI) to computer architecture have been neglected [1]. LSI has removed the technological distinction between logic and memory. It is now economically feasible to decentralize the CPU of a computer by replacing much of its maintenance software with functional hardware to improve system efficiency. Presently, an inordinate amount of processing time is spent on organizing and accessing files in peripherals. Peripherals are usually controlled directly by the CPU and have little or no associated logic of their own. A great improvement in this situation can be made by developing peripheral logic units. This would allow each peripheral to accomplish its own internal processing and thus reduce CPU housekeeping duties. This paper describes a 128-bit multicomparator that is designed to perform the search-sort function.

The block diagram of the multicomparator is shown in Fig. 1. The circuit consists of three independently clocked static-dynamic shift registers with associated EXCLUSIVE-NOR gating. In operation, the device indicates a match between the data word and the unmasked bits of the key word. The multicomparator is loaded with a key word by serially shifting the word into the key register and locking the register in static mode. While the key word is being loaded, the comparator is enabled by entering zeros[1] in the appropriate locations of the mask register. Masking allows the multicomparator to search for bit strings of varying length and composition. For example, assume it is necessary to search for all words containing a specific 113-bit code. By entering the 113-bit code in the key register and masking out the rest of the comparator, the multicomparator is conformed to search for this code wherever it occurs in the data file. Once the multicomparator is loaded with "key" and "mask" words, the file being searched is serially shifted through the data register. The data words are compared in bit parallel with the unmasked bits of the key word as they pass through the data register. When a match is found, the compare output goes high.

Large multicomparators can be constructed of the 128-bit circuits. Cascaded [Fig. 2(a)], the comparator can be used to search for words longer than 128 bits. By implementing multicomparators in parallel [Fig. 2(b)], a word-serial, bit-parallel

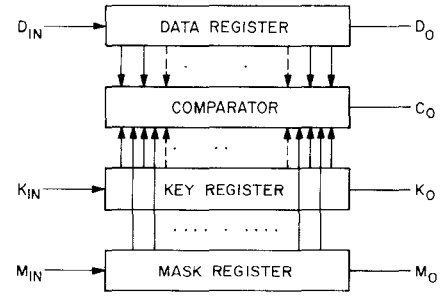

Fig. 1. Block diagram of multicomparator.

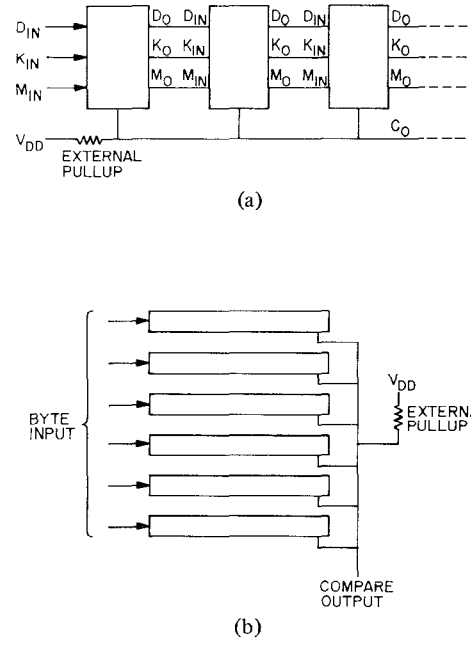

Fig. 2. Possible connections of multicomparator. (a) Cascaded. (b) Bit-parallel, word-serial.

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[1] Voltage convention: high—"1"—V_{DD}, low—"0"—V_{CC}. Note that since V_{DD} is negative for p-channel MOS and positive for n-MOS transistor-transistor logic (TTL) levels may or may not have reverse polarity depending on the processing used.

organization is achieved which is completely compatible with byte oriented machines. For example, an arbitrary length string of ASCII characters (such as one line of a source listing) can be easily searched using this technique, making the device ideal for indexing, test, etc.

There are many applications for the multicomparator in machine construction. As a result of its serial-search nature, the multicomparator is ideally suited to interface serial-access devices such as tapes or disks. For example, a "smart disk" can be constructed which has as a part of its instruction set, "find the following string." The specification of the string of course would allow DON'T CARES to mask out certain fields. For example, bin sorting could be accomplished in this manner. This capability coupled with a standard microprocessor would provide a disk capable of doing a large fraction of the string manipulation now done by CPU's. Such string manipulation capability on the word level would be useful in text processing applications. Many of the Snobol-type instructions can be directly implemented using the search chip as input to the processor.

CHIP DESIGN

The multicomparator was fabricated using p-channel silicon-gate metal-oxide-semiconductor (MOS) technology [2]. Since the circuit was designed with applications in computer peripherals in mind, an MOS clock rate of 2 MHz was adequate and MOS technology allowed a high packing density in combination with high yield. n-MOS processing can be used with the same design, with approximately $2\frac{1}{2}$ X performance advantage.

The multicomparator utilizes a 3-phase static-dynamic shift register cell [Fig. 3(a)]. The static feature is attained by adding a clocked feedback transistor to a standard 2-phase dynamic shift register cell. The clocking diagram is shown in Fig. 3(b). In dynamic operation, ϕ_1 and ϕ_2 are clocked sequentially while ϕ_3 is kept low. ϕ_3 serves as the clamping clock which holds data in the shift register. During static operation, ϕ_1 is low (isolating each cell of the shift register) and both ϕ_2 and ϕ_3 are high. ϕ_3 gates the output of an element back to the input, and hence during the transition between modes of operation, ϕ_3 must be delayed somewhat from ϕ_2 to avoid an undefined data state. In practice, one may use a delayed ϕ_2 as ϕ_3 for both static and dynamic operation.

A unique five device activated EXCLUSIVE-NOR gate was implemented to perform the compare operation [Fig. 4(a)]. The cross-coupled structure was chosen over the standard EXCLUSIVE-NOR circuit for layout simplicity. However, the operation is similar to an EXCLUSIVE-NOR gate with the addition of an activating transistor [Fig. 4(b)]. When the activating transistor is on, the comparator is operational. When off, the comparator is disabled and the compare output indicates a match irrespective of comparator inputs. Note that the match state is a logical ONE, hence when several EXCLUSIVE-NOR gates are connected in parallel to construct a comparator, only one not-compare element is necessary to pull the compare line down to the low state.

The maximum operating speed of the comparator is set by the compare line capacitance and its associated pickup device resistance. A single not-compare bit must be able to pull

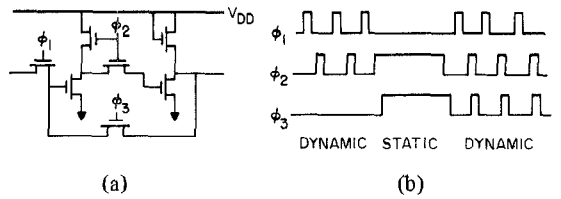

Fig. 3. Basic shift register cell. (a) Schematic. (b) Clock timing.

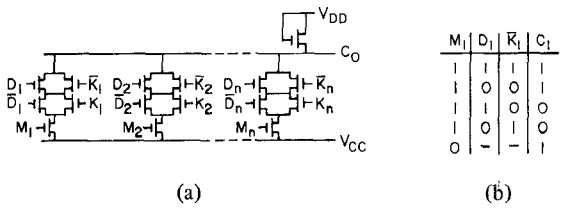

Fig. 4. Gated EXCLUSIVE-NOR gate. (a) Schematic. (b) Truth table.

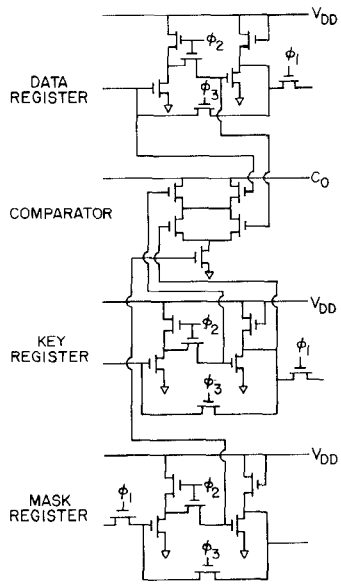

Fig. 5. Full schematic of one bit slice of the multicomparator.

the compare line down in one clock cycle. With the comparator shown, the compare line capacitance for one row of 32 cells is approximately 2 pF and the ON resistance of the 3 series comparator transistors is about 6 kΩ. Hence the time constant of a low going not-compare output from one row is approximately 12 ns. However, for a high going (compare) signal, the time constant is set by the 60 kΩ pull-up resistor at the end of the compare line. Thus the high going time constant is much larger (~120 ns). For this reason, the chip was arranged in four independent rows of 32 bits each. The four compare lines were NANDed to avoid paralleling the line capacitances and hence maintain the data rate achievable with the basic 32-bit row.

The schematic of one bit of the multicomparator is shown in Fig. 5. The circuit is composed of three static-dynamic shift registers for data handling and an EXCLUSIVE-NOR gate to accomplish the compare function. The unit cell was laid out using conservative design rules (10-μ metal lines with 10-μ

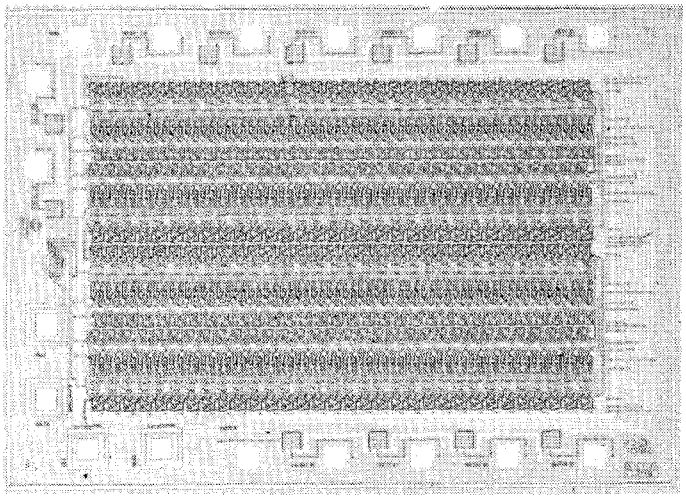

Fig. 6. Photomicrograph of multicomparator chip.

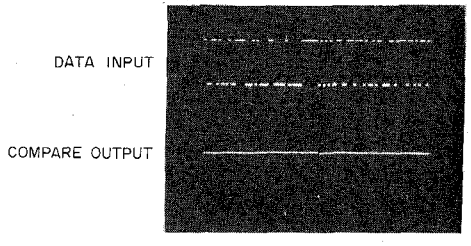

Fig. 7. Oscilloscope photo of multicomparator output with pseudorandom data input. *Note:* Compare pulse when data are aligned with internal stored-bit pattern.

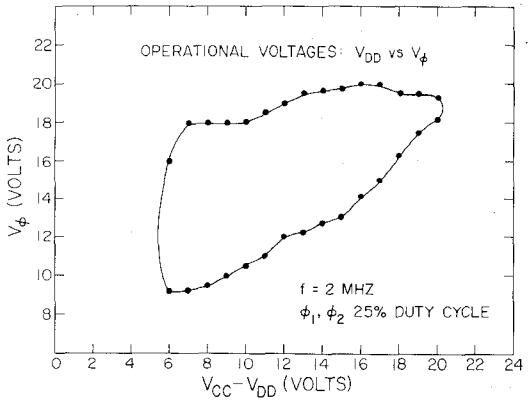

Fig. 8. Operational range of p-channel multicomparator chip.

metal-to-metal spacing). On silicon, the unit cell measures 91 X 470 μ. Photomicrographs of the 128-bit multicomparator unit cell and chip layout are shown in Fig. 6. Each shift register has independent clocks and separate output pads. The 3350 device multicomparator is 107 X 150 mils and has 18 bonding pads.

Performance Characteristics

A typical device characterization was carried out by entering a 128-bit data word composed of a pseudorandom sequence of ones and zeros in the key register. The comparator was enabled by simultaneously entering zeros in the mask register. The 128-bit data word was then cycled through the data register. Only when alignment between the cycling data word and its stored counterpart was achieved did match occur (Fig. 7). As expected, the compare pulses had a width equal to the time increment between ϕ_2 and ϕ_1 and recorded every 128 even pulses. When all ones are entered in the mask register, the comparator is disabled and the compare output is high (indicating a match) since there are no unmasked bits to disagree with the data register.

The multicomparator operates over a wide range of voltages with a TTL input. Fig. 8 shows the operational range of the multicomparator at a clock frequency of 2 MHz. The clocks had a 25 percent duty cycle and were symmetrically spaced in time. V_{cc} was set at +5 V with V_ϕ referenced to it. The minimum supply voltage is set by two MOS thresholds (approximately 2 V in the p-MOS process used). The maximum clock voltage was set by the onset of inversion under the field oxide. At high power supply voltages, the clock voltages were approximately one threshold less than $V_{cc} - V_{DD}$.

TABLE I

Parameter	Performance[a]
Clock rate	0.0001–2 MHz
Dynamic supply current	25 mA
Static supply current	30 mA
Clock leakage current (ϕ_1)	120 nA
Clock leakage current (ϕ_2)	300 nA
Clock capacitance (ϕ_1)	40 pF
Clock capacitance (ϕ_2)	60 pF
Clock capacitance (ϕ_3)	40 pF
Interclock capacitance	7 pF
Input capacitance	10 pF
Output capacitance	10 pF

[a] *Test Conditions:*

$T = 23°C$, $V_{cc} = 5$ V, $V_{DD} = -5$ V,

$V_{\phi L} = +5$ V, $V_{\phi H} = -5$ V, $V_{\text{input}} = 0.5$ V.

The multicomparator performance characteristics are summarized in Table I.

ACKNOWLEDGMENT

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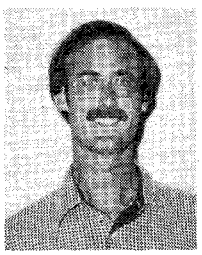

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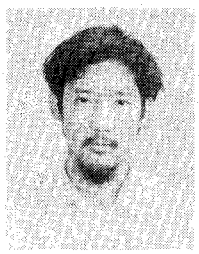

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