A MOS Cursive-Character Generator

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Abstract—Cursive characters can be made to be more readable, more attractive, and better suited to the operation of grapic CRT terminals than the usual dot-matrix type; a system using cursive-type characters achieves much higher writing rate while requiring much less bandwidth than that using dot-matrix-type characters. This paper presents an economical method of generating the x, y, and z analog signals for forming cursive characters with the deflection system of a CRT.

A circuit design embodying a complete 48-stroke character generator on a single MOS integrated circuit is described. The IC accepts 7-bit ASCII code and outputs x, y, and z analog signals to generate any one of 32 standard ASCII characters in 5 μs. Additional groups of 32 characters can be added by merely paralleling additional chips. The entire 32 character digital and analog function has been implemented on a single self-contained 16-pin silicon-gate MOS chip 125 × 165 mil in size. Character encoding on the chip is accomplished in one mask at the diffusion step, and a straightforward mask-generation procedure has been developed.

INTRODUCTION

THE increasing availability of low-cost data processing through computer time-sharing, mini- and microcomputers, digital business control systems, etc., has rapidly expanded the use of electronics in new and different applications. Huge new markets for man/machine interfaces have been created. As the price of the basic data-processing circuits has decreased, price pressure is placed on such equipment as CRT terminals, displays, and teleprinters which are no longer as compact and inexpensive as the new data processors. At the same time, CRT graphic display systems are rapidly gaining popularity as a means of fast, versatile, and uncomplicated man/machine interaction.

Dot matrix is the most popular character format for computer-terminal CRT display systems. The 5 × 7 dot matrix provides acceptable character shapes for numbers, uppercase letters, and most punctuation marks; however, it tends to cause eye strain if the display changes rapidly. For a display of 60 frames/s, 24 lines/frame, 80 characters/line, and 5 × 7 dot-matrix characters using a standard TV chassis, the dot rate requirement is about 8.6 MHz. The 7 × 9 dot matrix displays rather attractive characters and can handle lowercase letters, but the video bandwidth requirement for displaying lines of 80 characters is more than a standard TV chassis can handle. Moreover, fairly complex digital and analog functions are needed in addition to the character generator ROM.

Aside from the hardware complexities, the dot matrix is a raster scan technique which, while being useful in displaying picture-type images, is very wasteful of time and memory information, and provides poor resolution when used for vector graphics and alphanumeric character displays. Since the CRT display is essentially emulating the human hand in forming characters, a natural approach to character synthesis would be a cursive one.

Cursive characters can be closely approximated by a stroke technique. Each character is formed by drawing straight line segments from point to point. It is found that excellent characters with better resolution than the 7 × 9 dot matrix can be formed with 20 to 40 strokes, as illustrated in Fig. 1.

In order to generate stroke-type characters, analog voltage functions must be generated for x- and y-axis deflection.

Two publications on cursive (stroke) character generation have appeared earlier. Gilbert's approach [1] uses bipolar technology, and uses 60 mil^2 of silicon area to generate each stroke with no intensity control, as compared with 13 mil^2/stroke in our MOS design. Therefore, the MOS design can pack more characters, and more strokes per character, into a chip. Moreover, the MOS technique is inherently less temperature sensitive, and with the program mask dimensions definable to 1-μm increments (conservative), it achieves higher granularity in stroke size. However, it requires two external differential video amplifiers.

Harp's approach [2] uses electromagnetic delay line coupled to programmable strips on etched circuit boards. Due to the natural speeds of electromagnetic transmission lines, the device is not suitable for generating characters slower than 1 μs each; it is also bulky and complicated. The finite rise time of the delay line makes it difficult to separate adjacent stroke signals, and attenuation along the delay line is considerable. Both effects tend to distort the character formation, and they must be compensated for in the character programming.

This paper describes a novel circuit design that realizes a sequential read-only analog memory using conventional silicon-gate MOS technology [3], [4].

THE PROGRAMMABLE WAVEFORM GENERATOR

The new analog ROM circuit technique is illustrated with a conceptual capacitive voltage-divider circuit shown in Fig. 2. When a voltage step is applied to the input, the output voltage

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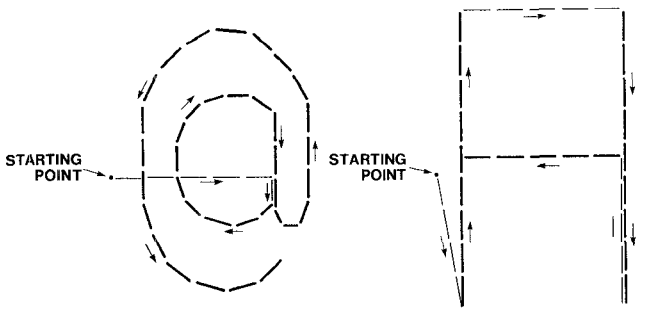

Fig. 1. Two examples of stroke-character formation.

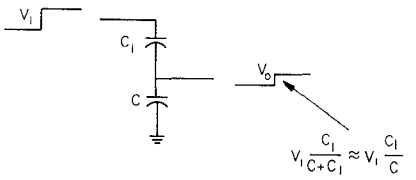

Fig. 2. Capacitive voltage-divider circuit.

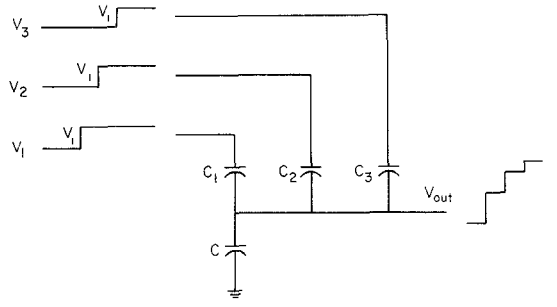

Fig. 3. Circuit for generating a programmable staircase voltage function.

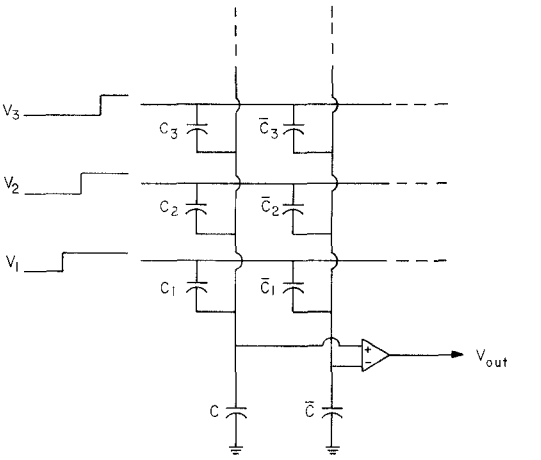

Fig. 4. Circuit for generating a programmable discrete-time voltage function.

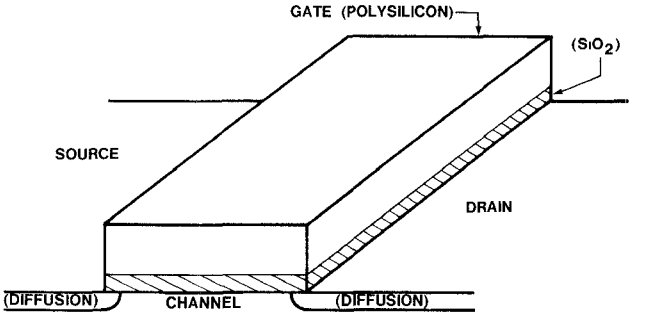

Fig. 5. Silicon-gate MOS transistor.

is a step with an amplitude

$$V_O = V_i C_1/(C + C_1). \quad (1)$$

If $C \gg C_1$, the amplitude of the output voltage step is approximately proportional to C_1, assuming V_1 is kept constant. If connected to C there are several capacitors, $C_1, C_2, C_3, \cdots$, with voltage-step inputs that are of equal amplitude but uniformly spaced in time (see Fig. 3), the output voltage will be a staircase with step sizes proportional to C_1, C_2, C_3, $\cdots$.

If two of these capacitive networks C_j and $\bar{C}_j$ are supplied by the same input steps, the voltage difference between the two outputs can be of either sign, depending on the relative sizes of C_j and $\bar{C}_j$ (see Fig. 4). Connecting a differential amplifier to two such networks yields an output voltage that can be an arbitrary discrete time function which can have both positive and negative slopes. If the sizes of the capacitors C_j and $\bar{C}_j$ are controllable, they can be programmed to produce various voltage functions at the output.

Each C_j and $\bar{C}_j$ pair corresponds to a step increment in the staircase waveform output. When such staircase waveforms are used as x- and y-axis deflection voltages, each capacitor pair can be used to generate either the Δx or Δy voltage for a stroke in the synthesis of alphanumeric characters, while C and $\bar{C}$ can do the summing.

All of what has been said would be equally true if resistors had been used in place of capacitors, but in the implementation that follows, capacitors are the logical choice for the MOS technology.

The MOS Circuit Design

The waveform generation principle just illustrated can be realized with the standard silicon-gate-enhancement MOS transistor, as illustrated in Fig. 5. The gate-to-channel capacitance of the MOS transistor is used for the capacitors $C_1, C_2, C_3, \cdots$ and $\bar{C}_1, \bar{C}_2, \bar{C}_3, \cdots$, while the capacitors C and $\bar{C}$ are off-chip capacitors. The x, y, and z voltages are due to charges induced in the channels of the MOS transistors by voltage steps at their gates. Fig. 6 shows a simplified schematic of the MOS analog memory with its associated off-chip circuitry.

The z signal (intensity control) is a binary signal that tells the CRT beam to go either on or off. A capacitor between the $+z$ line and a particular drive line produces a current pulse during that stroke to turn on the CRT beam, whereas one on the $-z$ line turns the beam off. The $+z$ and $-z$ lines are brought outside the chip and fed into current amplifiers that bring the pulses up to the proper logic levels. They then trigger an R-S flip-flop, whose output is the intensity control signal.

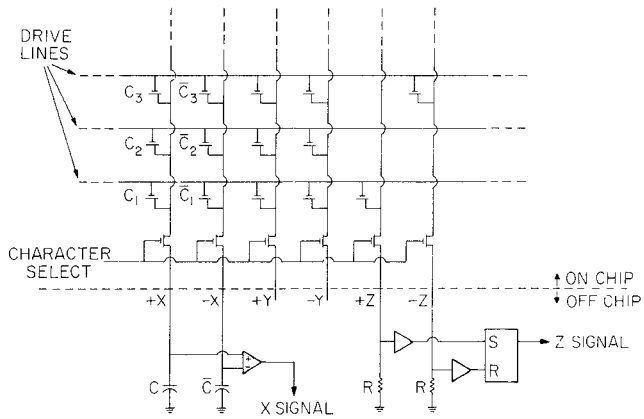

Fig. 6. Schematic for generating the x and z voltages.

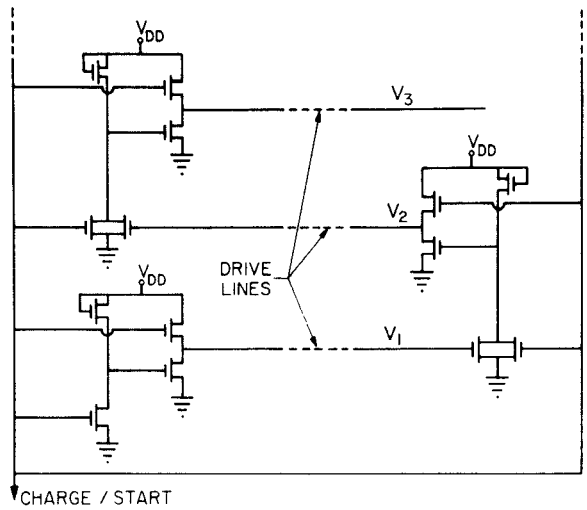

Fig. 7. Charge and discharge circuit for the drive lines.

The characters are encoded in one mask at the diffusion step. For the x and y groups, the gate-to-channel area of the program transistors is the variable parameter. In this design, the width of the polysilicon drive lines is the channel length, and is kept constant, while the channel width is varied by the diffusion mask. For the z group, the choice is whether or not a channel is placed under a particular gate drive line, and is also controlled by the diffusion mask.

The software for programming new fonts has been developed; the font is specified in an artwork language (PAL), and the mask-generation routine encodes the information in the diffusion mask. Stroke lengths are kept fairly uniform in the character font design because display brightness depends on deflection rate; for short strokes, a little bit of intensity variation is not very noticeable in viewing, however. Also, to form a sharp angle, the display is stopped at the corner for one stroke time with the beam turned off.

Fig. 7 shows the schematic diagram of the voltage step drivers. When the CHARGE/START line is at logic "1", all the polysilicon drive lines are precharged in parallel until they are at $V_{DD}-V_T'$, where V_T' equals threshold voltage of the pull-up transistor (with body effect). After the precharge cycle, character generation can be initiated by setting the CHARGE/START line to logic "0." Initially, all the drive lines except the first one are left floating, but the first drive line starts discharging as soon as the CHARGE/START line is at logic "0." This, in turn, causes the second line to discharge, and so on.

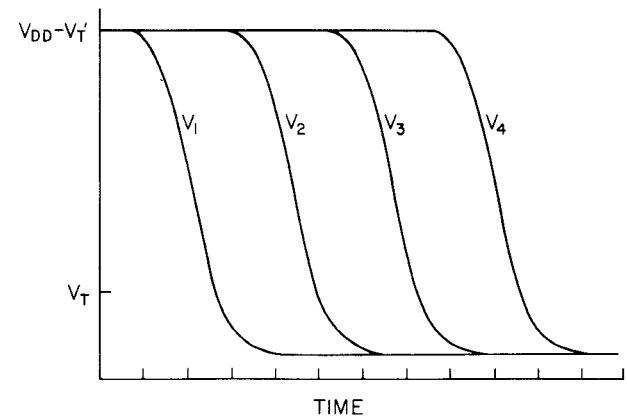

Fig. 8. Waveforms of drive lines.

The time interval between successive steps is the sum of the propagation delay through the inverter and the inverting driver driving the large capacitance of the drive line, plus that due the distributed RC line effect [5]. It amounts to about 100 ns at room temperature. Fig. 8 shows the computer-simulated voltages on the drive lines plotted as a function of time.

The CHARGE/START signal is also used to short the analog outputs to ground during the precharge cycle. This ensures that at the start of each character, the external summing capacitors for the x and y channels are discharged to ground potential.

The operation of each program capacitor is analogous to a single cell of a CCD shift register, where the channel is the potential well. During the precharge cycle, the source-drain diffusions supply minority carriers to the potential well, and they also collect the minority carriers when the potential well is being emptied by the decreasing gate voltage. In order that most of the carriers are collected by the source-drain diffusions and not left behind to be recombined in the substrate, the channel length must be short enough so that the carrier transit time is less than the gate-voltage fall time [6], [7]. However, if the fall time is too long, then successive steps overlap and strokes blend together; this has the effect of low-pass filtering.

The first prototype of this chip was designed and fabricated in 1973, and enhancement transistor was the only type of device available in the MOS process at the time. Since enhancement capacitance disappears when the gate voltage drops below V_T, the effective step voltage is

$$V_{\text{step}} = V_{DD} - V_T' - V_T . \tag{2}$$

assuming that the analog output voltage is close to ground potential.

Fig. 9 shows a block diagram of the character-generator chip. It has been encoded with 32 characters, with a maximum of 48 strokes each. Each character is generated in about 5 μs. Additional groups of 32 characters can be added by merely paralleling additional chips. The entire chip is controlled by only one line other than the 7-bit ASCII code.

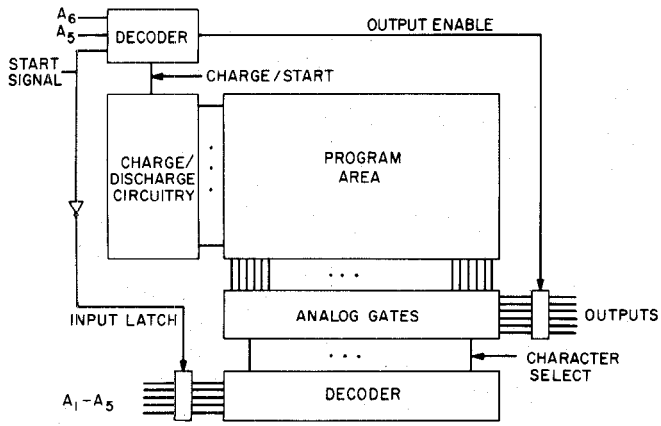

Fig. 9. Block diagram of the character generator chip.

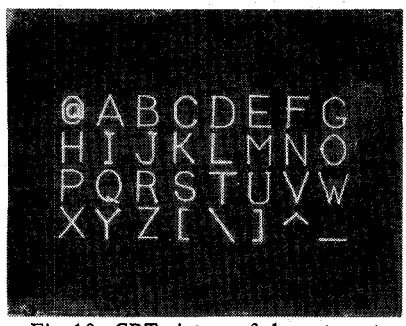

Fig. 10. CRT picture of character set.

The capacitor array is partitioned in two halves, and each half contains the encoding for 16 characters, only one of which can be selected at a given time. The remaining 15 groups have all their signals lines disconnected. When one drive line is being discharged, the capacitors which belong to the 15 unselected characters couple that pulse to their signal lines, and unless these unselected lines are tied to a fixed potential, that pulse will be indirectly coupled to the rest of the drive lines. Since all the drive lines that have not been discharged yet are left floating as dynamic nodes, they can lose their charge prematurely due to this back-coupling effect. Therefore, all the unselected signal lines are tied to ground. This problem would not have existed had static circuitry been used to generate the voltage steps; it would require many more parts in the driver circuit, however.

The off-chip amplifiers for the x and y channels require about 4-MHz bandwidth, while standard TTL or CMOS can be used for the intensity control logic.

Results

Fig. 10 shows an unretouched CRT picture of a character set that was encoded in the prototype chip. Note the legibility and resolution of the characters. Italics can be produced by mixing the x signal with some y signal.

To form a line of characters, the CRT beam can be made to scan horizontally at the line rate while the character generator circuitry superposes the x and y signals into the deflection system. The constant horizontal deflection rate can be compensated for by superposing a negative ramp into the x-axis amplifier.

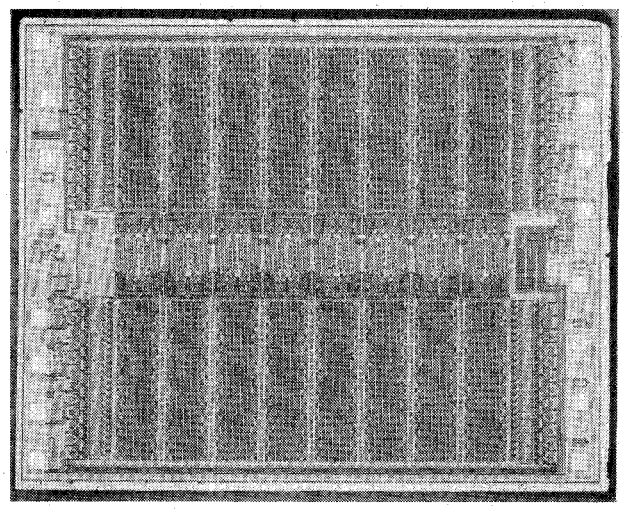

Fig. 11. Photomicrograph of the character generator chip.

As pointed out earlier, the duration between successive steps is due to the distributed RC delay of the drive line, plus the propagation delay in the driver. Since the drivers are on both sides of the capacitor array, and the voltage step propagates from left to right on one drive line and from right to left on the next, only the capacitors in the middle of the array get the steps at regular intervals; the ones near the edge of the array get them with pairs of steps merged together. This is not a serious problem, because such a character appears like it has half as many strokes as it really has, but the general shape is unchanged. However, it would be advisable to reserve the center of the array for characters that contain a lot of curvature (e.g., @, S, O, Q, etc), while the characters that are made of straight lines can be at the edge of the array without any noticeable problem.

Another solution is to abandon the polysilicon gate material which has a sheet resistivity of about 100 $\Omega/\square$, and replace it with molybdenum gate material, which has two orders of magnitude lower sheet resistivity [8], [9]. Yet another solution is to use a silicon-gate process with double-layer metal, and transmit the voltage steps on metal lines.

Fig. 11 shows a photomicrograph of the prototype chip. The chip measures 125 X 165 mil. The memory area for encoding each character consists of a group of six output lines (metal) that run over 48 drive lines (polysilicon) and as many as 240 program transistors of various sizes. One such character amounts to about 310 mil^2. The layout of the chip is arranged to suit the natural geometry of the character groups; the memory area is organized in two halves, with the output multiplexer located at the center.

It should be noted that this chip was designed for MOS technology of the vintage of 1973, using 10-μm linewidths. With the high-density technologies of today, the entire ASCII character set can be implemented on one chip using this circuit technique.

Factors that Affect Operation

With built-in edge-enhancement mechanisms, the human eye is, in general, fairly tolerant to seeing absolute errors of about

5 percent in displacement, but circles such as the letter "O" must close on itself.

Since each stroke results in a Δx and Δy increment in the CRT beam deflection, and only linear circuit elements are involved, the error in each stroke contributes to the error in the overall character display in an additive manner.

The accuracy of the gate-to-channel capacitance depends on such factors as undercutting of the photomask, variations in oxide thickness, and fringing-field capacitance. Variations in photoetching and oxide growth tend to have long-range gradients and do not deviate appreciably over the size of the chip. Experimentally, capacitors on the same chip can be matched to ±2 percent with excellent yield. Such errors can be reduced by using a smaller capacitor array.

However, character size can vary by ±20 percent from chip to chip due to differences in polysilicon linewidth and oxide thickness, which cause a ratiometric error in all the program capacitors throughout the chip. This can be compensated for by gain calibration on the x- and y-axis amplifiers.

Since the channel width is programmed for each stroke, additive error in channel width due to error in photoetching distorts the character shape. Such errors are cancelled out because pairs of program capacitors, C_j and $\overline{C}_j$, feed into a differential amplifier and only their differences contribute to the deflection voltage.

Random variations with short range gradients can cause random errors in each Δx and Δy step. The rms error in absolute displacement after summing n steps is equal to $\sqrt{n}$ times the rms error in each step because random variations tend to average out. Such errors can be reduced by using larger program capacitors.

In computing the gate-to-channel capacitance, the parallel-plate capacitance formula can be used if the gate-length and width dimensions are large compared to the oxide thickness, and the polysilicon thickness is small compared to it [10]; the former condition is mostly true, but the latter is not. Therefore, for the minimum-size capacitor, the parallel-plate formula is in error by about 20 percent due to fringing-field capacitance. The three-dimensional analysis of this problem is difficult because its exact solutions do not exist. However, by lumping it as an edge-related effect, fringing-field capacitance can be treated as additive errors in channel length and width, just like photoetching errors. Our prototype results bear out this simplifying assumption of using the parallel-plate formula.

The size of the voltage steps directly control stroke size and character size. Equation (2) indicates that the supply voltage (V_{DD}) directly controls the step size; MOS threshold voltage also affects it. Threshold voltage has a temperature coefficient of about -3 mV/°C [11], [12]. With a 5-V supply, the effective step size can vary by 10 percent over a 50°C increase in temperature (increase in n-channel, decrease in p-channel). The threshold dependence in (2) can be eliminated by using depletion MOS devices.

The SiO_2 dielectric capacitor has a very low temperature coefficient of about 20 parts per million per degree Celsius (ppm/°C) [13].

The step generation is allowed to ripple asynchronously because the time that it takes to ripple through all the strokes, as defined by circuit layout and device physics at room temperature, just happens to coincide with the speed at which the character generator is expected to operate. However, the generation speed is dependent on temperature. The step driver slows down with increasing temperature due to the $T^{-1.5}$ dependence of the inversion-layer mobility of MOS transistor [14], where T is in degrees Kelvin. For annealed polysilicon film with 100-Ω/□ sheet resistivity, the temperature coefficient of resistance is about +500 ppm/°C [15]. Consequently, the speed decreases by about 15 percent over a 50°C increase in temperature. If desired, a completion signal can be brought out of the chip.

If it is important that the generation speed be accurate, the step drivers can be designed to operate from an external clocking signal. If the voltage steps are synchronized to a clocking signal, then clocked sense amplifiers can be used to sense the $+z$ and $-z$ current pulses, and the intensity control signal can be generated on the chip with very little additional logic.

After the precharge cycle, all the drive lines in the capacitor array are left floating as dynamic nodes while waiting to be discharged. Typically, junction leakage current is the only mechanism for the premature discharging of the dynamic nodes. This is similar to the dynamic RAM retention problem, except that the RAM cell is a binary element which has a much bigger margin of error on its voltage level. However, the drive lines contain much more capacitance on the polysilicon line with respect to junction area of the source-drain diffusions in the drivers, as compared with the dynamic RAM. Reverse-bias leakage current is due to electron-hole pairs generated in the semiconductor near the junction, and is strongly dependent on temperature [16]. We estimate that at 70°C it would take about 1 ms before the voltage drop becomes serious.

In order to approximately linearize (1), each external summing capacitor should be about three orders of magnitude larger than each program capacitor. This is a tradeoff between accuracy and the output-signal size. With 50-pF external capacitors and 5-V supply, the maximum voltage excursion during a character is less than 50 mV towards forward biasing any p-n junction on the chip. The analog output voltage also introduces error on the effective voltage step given in (2) when enhancement program capacitors are used.

Other Applications

If this waveform-generation technique is used for other purposes in which lower speeds are desired (e.g., character generation for electrostatic ink-jet printer), the step generator can then be clocked to generate at any desired speed. With appropriate on-chip programming and suitable control of the clocking signal, single pulse or repetitive waveforms of various durations or frequencies can be generated. Some obvious applications for such a device include different types of audio synthesis. The range of possibilities is only limited by the imagination of the design engineer.

Conclusion

Stroke characters can appear to be more readable and more attractive, and they are more suitable for graphic CRT terminals

than dot-matrix characters. A system that uses stroke characters can achieve higher writing rate while requiring less video bandwidth than that which uses dot-matrix characters. We have described a novel device that generates the x, y, and z analog signals for stroke-character formation, and is ideally suitable for integration in MOS LSI. Because of its simplicity, low cost, and speed, this device is appropriate for application in CRT display systems where the viewing of a large number of characters is required.

Acknowledgment

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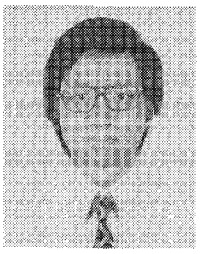

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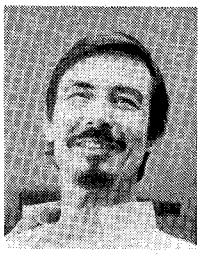

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