Current-Voltage Characteristics of Small-Size MOS Transistors[*]

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Abstract—One-dimensional analysis is used to find an upper and lower bound to the drain current of MOS transistors. The drain and source depletion regions and charge carrier velocity saturation are taken into account. These considerations are important in small devices.

As the channel length of a MOS transistor is made smaller, two corrections to the standard theory [1] should be considered. First, the drain and source regions are no longer negligible compared to the channel length. Second, charge carrier velocity saturation becomes important. One-dimensional analysis, including these two corrections, is used to find an upper and lower bound to the drain current.

1 One-Dimensional Analysis

The metal-oxide-semiconductor (MOS) transistor is essentially a two-dimensional device. It can, however, be analyzed approximately as a one-dimensional device, provided that 1) the channel plus substrate charge per unit area is determined exclusively by the gate voltage and not by the source or drain voltages (all voltages are referred to the substrate), and 2) the electric field component along the channel should be small compared to the normal component in the silicon surface. Both conditions are satisfied in the central region of the channel defined by $W_S < x < (L - W_D)$. L is the channel length, and W_S and W_D are the source and drain depletion region thicknesses in absence of the gate, as shown in Fig. 1. Thus, the one-dimensional analysis can be applied only to the central region of the channel. The problem is then to determine the boundary conditions, i.e., the channel voltages at $x = W_S$ and $x = (L - W_D)$. This is a difficult problem because two-dimensional analysis cannot be avoided.
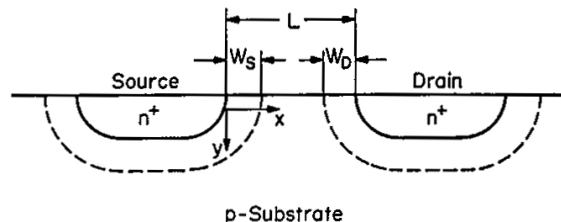

Figure 1: Cross-section of an n-channel MOS transistor. Drain and source depletion regions in absence of the gate extend to the dashed lines. The x, y coordinates used in the analysis are shown.

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[*]Re-typeset from original material by Donna Fox (June, 2017). Originally published in *IEEE Transactions on Electron Devices,* Vol. ED-19, No. 3, March, 1972

We shall consider an n-channel device. The charge per unit area induced in the silicon by the gate voltage is the sum of the channel charge per unit area $-Q$, and the depletion region space charge per unit area $-\sqrt{2\epsilon q C_B V}$. V is the substrate band bending, C_B is the substrate doping concentration, ϵ is the silicon permittivity, and q is the electronic charge. The electric field in the gate oxide is $(V_G - V_{FB} - V)/x_0$, where V_{FB} is the flat-band voltage and x_0 is the oxide layer thickness. Thus

$$Q + \sqrt{2\epsilon q C_B V} = C_0(V_G - V_{FB} - V) \tag{1}$$

where $C_0 \equiv \epsilon_{ox}/x_0$ is the oxide capacitance per unit area. ϵ_{ox} is the oxide permittivity.

The drain current I_D can be obtained by solving the differential equation

$$I_D = Z \int_0^w qn(x,y)v(x,y)dy \equiv ZQv_{\text{eff}} \tag{2}$$

where n and v are the charge carrier concentration and velocity, Z is the channel width, $Q \equiv \int_0^w qn\,dy$ is the channel charge per unit area given by Eq. 1, and v_{eff} is the effective carrier velocity. We approximate the effective carrier velocity by

$$v_{\text{eff}} = v_0 \cdot \frac{dV}{dx} \Big/ \left(\frac{dV}{dx} + \frac{v_0}{\mu_{\text{eff}}}\right). \tag{3}$$

This expression has the correct behavior at the two asymptotes. For low electric fields in the x direction $v_{\text{eff}} \approx \mu_{\text{eff}}(dV/dx)$, where μ_{eff} is the effective mobility. For high electric fields in the x direction $v_{\text{eff}} \approx v_0$, where $v_0 = 1 \times 10^7 \text{cm/s}$ is the saturation velocity of electrons in silicon.

The solution of Eq. 2 with the boundary conditions $V = V_1$ at $x = x_1$, and $V = V_2$ at $x = x_2$ is

$$I_D = \frac{ZC_0\mu_{\text{eff}}}{\left[L' + \frac{\mu_{\text{eff}}}{v_0}(V_2 - V_1)\right]} \left\{(V_G - V_{FB})(V_2 - V_1) - \frac{1}{2}[V_2^2 - V_1^2] - \frac{2}{3C_0}\sqrt{2\epsilon q C_B}[V_2^{3/2} - V_1^{3/2}]\right\} \tag{4}$$

where $L' \equiv x_2 - x_1$. Notice that the effect of charge carrier velocity saturation is to replace the length L' by $[(L' + (\mu_{\text{eff}}/v_0))(V_2 - V_1)]$. Eq. 4 is only valid for $V_1 \leq V_2 < V_{2\text{sat}}$ where $V_{2\text{sat}}$ is the channel saturation voltage defined by

$$\frac{\partial aI_D}{\partial aV_2}\bigg|_{V_2 = V_{2\text{sat}}} = 0. \tag{5}$$

It can be shown that when $V_2 = V_{2\text{sat}}$, the charge carriers at $x = x_2$ have the saturation velocity v_0, so that the channel charge per unit area at $x = x_2$ is

$$Q(V_{2\text{sat}}) = \frac{I_D}{Zv_0}. \tag{6}$$

In addition, if $V_2 = V_{2\text{sat}}$, the electric field along the channel dV/dx is infinite at $x = x_2$. Since the electric field cannot be infinite, we conclude that the channel voltage at $x = (L - W_D)$ is always smaller than $V_{2\text{sat}}$.[1]

The dependence of the effective mobility on the electric field component normal to the silicon surface was not taken into account when integrating Eq. 2. This effect can be approximated by an empirical relation [1] between μ_{eff} and the "average" electric field component normal to the silicon surface, defined by

$$E_S = [V_G - V_{FB} - \frac{1}{2}(V_1 + V_2)]\frac{C_0}{\epsilon}. \tag{7}$$

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[1]This statement is also confirmed by a first-order two-dimensional analysis of the fields near the drain [2].

2   Upper Bound

At the source, the substrate band bending V at onset of strong inversion is $V = V_S + 2\phi$. At the drain, it is $V = V_D + 2\phi$. ϕ is the difference between the Fermi level and the intrinsic Fermi level in the bulk of the substrate. An upper bound to the drain current can be obtained from Eq. 4 by setting L' equal to $(L - W_S - W_D)$, $V_1 = V_S + 2\phi$, and $V_2 = V_D + 2\phi$ or $V_2 = V_{2\text{sat}}$, whichever is smaller. This is equivalent to applying the one-dimensional analysis from $x_1 = W_S$ to $x_2 = (L - W_D)$, but instead of using the correct (but unknown) boundary conditions V_1 and V_2, we use a lower bound for V_1 and an upper bound for V_2. As a result, the drain current obtained by this approximation is an upper bound to the actual current. Standard theory [1] and this upper bound are compared with experiment, for a particular MOS transistor, in Fig. 2(a) and (b).
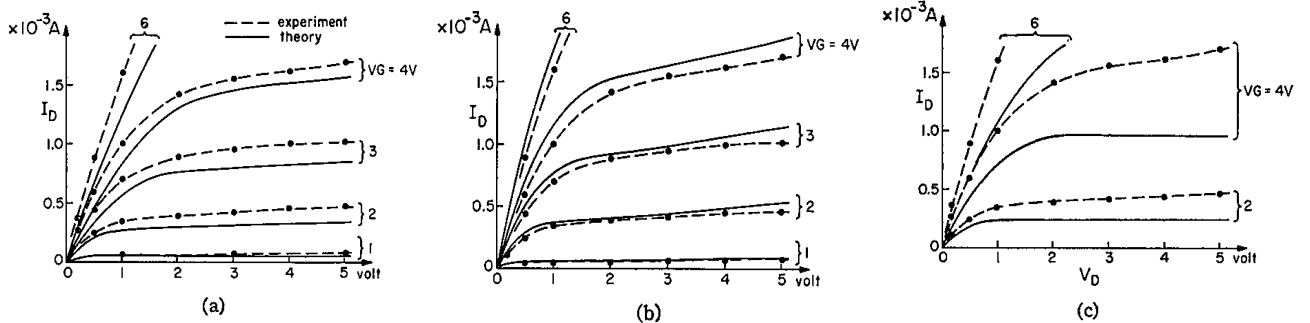

Figure 2: (a) Standard theory, (b) upper bound, and (c) lower bound are compared with the experimental drain characteristics of a particular MOS transistor. The transistor characteristics are $L = 3.4$ μm, $Z = 51$ μm, $V_{FB} = -1.0$ V, $x_0 = 1100$ Å, $C_B = 2.8 \times 10^{15}$ cm^{-3}, and $\mu_{\text{eff}} = 0.0770 - 1.25 \times 10^{-9} \cdot E_S$ (m^2/V_s). The source voltage is $V_S = 0$ V. All voltages are referred to the substrate.

3   Lower Bound

A lower bound to the drain current is obtained from Eq. 4 by setting L' equal to the source-drain spacing L, $V_1 = V_S + 2\phi$, and $V_2 = V_D + 2\phi$ or $V_2 = V_{2\text{sat}}$, whichever is smaller. This is equivalent to assuming that the one-dimensional analysis is valid from source to drain. This approximation underestimates the channel charge per unit area near the drain and near the source, because even without the gate, the substrate is already depleted near the drain or the source. Thus, we conclude that this approximation is a lower bound to the drain current. This lower bound is compared with experiment in Fig. 2(c).

4   Summary and Conclusions

The gate turn-on voltage V_{GT} is obtained from Eq. 1 by setting $V = V_S + 2\phi$ and $Q = 0$. The result is

$$V_{GT} = V_{FB} + V_S + 2\phi + \frac{1}{C_0}\sqrt{2\epsilon q C_B(V_S + 2\phi)}. \tag{8}$$

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If $V_G \leq V_{GT}$, $I_D = 0$. If $V_G > V_{GT}$,

$$I_D = \frac{ZC_{0\mu\text{eff}}}{[L - \alpha(W_S + W_D) + (\mu\text{eff}/v_0)(V_{D'} - V_S)]}$$
$$\cdot \left\{ (V_G - V_{FB} - 2\phi - \frac{1}{2}V_{D'})V_{D'} - (V_G - V_{FB} - 2\phi - \frac{1}{2}V_S)V_S \right.$$
$$\left. - \frac{2}{3C_0}\sqrt{2\epsilon q C_B}[(V_{D'} + 2\phi)^{3/2} - (V_S + 2\phi)^{3/2}] \right\} \quad (9)$$

where $V_{D'} = V_D$ or $V_{D'} = V_{D\text{sat}}$, whichever is smaller.

The drain saturation voltage $V_{D\text{sat}}$ is defined by

$$\frac{\partial I_D}{\partial V_D}\bigg|_{V_D = V_{D\text{sat}}} = 0. \quad (10)$$

(The drain depletion region W_D is kept constant during the differentiation.) In Eq. 9, it is understood that $V_D \geq V_S$, and that neither the source nor the drain junctions are in forward conduction. An upper bound to the drain current is obtained from Eq. 9 by setting $\alpha = 1$. A lower bound is obtained with $\alpha = 0$. The correct value of the factor (or function) α can only be obtained from a two-dimensional analysis, or from experiment. The present analysis guarantees that $0 < \alpha < 1$.

Eq. 9 is the same as the standard expression except for two additional terms in the denominator: $-\alpha(W_S + W_D)$, which takes into account the depletion regions and $(\mu\text{eff}/v_0(V_{D'} - V_S)$, which is due to velocity saturation of the charge carriers.

The standard expression is quite good even for channel lengths as small as $4\,\mu$m because the two corrective terms are of similar magnitude and opposite sign. The upper and lower bounds do not differ by more than a factor of 2, even for the smallest MOS transistor determined by fundamental physical limitations [3].

References

[1] D. Frohman-Bentchkowsky and L. Vadaz. *Computer-aided design and characterization of digital MOS integrated circuits,* April, 1969: IEEE J. Solid-State Circuits, Vol. SC-4, pp. 57–64.

[2] D. Frohman-Bentchkowsky and A.S. Grove. *Conductance of MOS transistors in saturation,* January, 1969: IEEE Trans. Electron Devices, Vol. ED-16, pp. 108–113.

[3] B. Hoeneisen and C.A. Mead. *Fundamental limitations in microelectronics I. MOS technology,* 1972: Solid-State Electronics, 15 (7), pp. 819–829.