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## Transistor Switching Analysis

Dr. C. A. MEAD\*

### Part 2

**Diode Recovery.** Suppose we connect a junction diode in the circuit shown in *Fig. 6*. If the applied voltage  $V$  remains at  $+V_1$  for a sufficient time, the current  $i$  will reach a steady state value very nearly  $V_1/R$ , assuming the forward voltage drop across the diode is small compared with circuit voltages. If now

the applied voltage is abruptly changed to  $-V_2$ , the current is observed to assume a nearly constant value  $-V_2/R$  for a storage time  $t_s$ , after which it decays rapidly to its small steady state reverse value  $i_s$ . The explanation for this action is as follows:<sup>(5)</sup>

At  $t = 0$ , the excess density of minority carriers near the junction is as shown by the top curve of *Fig. 7*. At a slightly later time, the applied voltage

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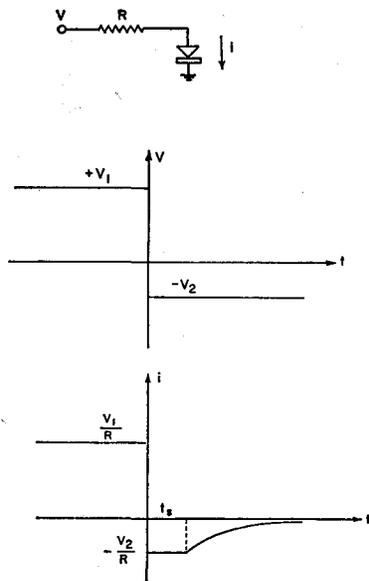


Fig. 6—Recovery of p-n diode from step input.

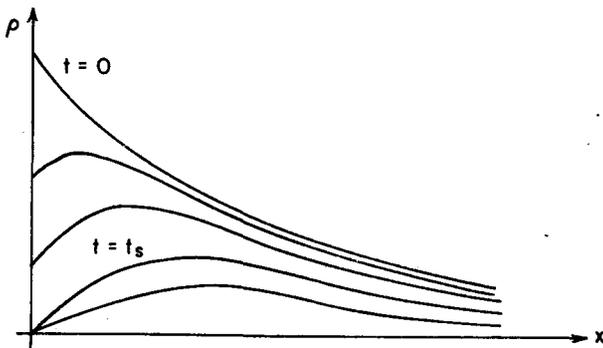


Fig. 7—Excess density distribution in p-n diode during recovery.

has reversed, but the stored carriers have not had time to recombine or diffuse away. The rate at which they may cross the junction is limited to a maximum reverse current of  $V_2/R$ , since a higher value would appreciably forward bias the junction and hence be self-annihilating. However, since the excess density of minority carriers at the junction is greater than zero, the junction must remain slightly forward biased, and the voltage across the junction remains small. As long as the junction remains forward biased, the current is determined by the external circuit. In this case, the current during the storage period is very nearly  $-V_2/R$ . This condition determines the slope of minority carrier density at the junction, which is proportional to the junction current. At the end of the storage time  $t_s$ , the junction excess density has just reached zero and approaches  $-p_n$  as the junction becomes reverse biased. Since the junction excess density is essentially constant (nearly zero) for any reverse bias voltage, the current is no longer af-

ected by the junction voltage but is determined only by the conditions within the semiconductor. Therefore, the decay time is characterized by the minority carrier lifetime.

**Diode Storage Time Calculation.** We may obtain a good estimate of the recovery time from a simple calculation using the one section lumped model of Fig. 5c. Although the results are not nearly as accurate as those which will shortly be obtained for the transistor, they are significant and the method used is typical of all lumped model calculations.

(a) Steady State

Since the diode is forward biased, the voltage across it is small compared with  $V_1$  and we may assume

$$\frac{V_1}{R} \approx I = G\rho_{ss}$$

The voltage across the diode may be found by using the value of  $\rho_{ss}$  obtained from this equation and the exponential junction law.

(b) Storage Period

When the applied voltage changes sign, the charge on C cannot change instantaneously, and hence  $\rho$  must be continuous. As long as  $\rho$  is greater than zero, the diode is forward biased and the voltage across it is small. Hence the current is very nearly  $-V_2/R$ . To determine the storage time  $t_s$ , we find  $\rho$  as a function of time assuming the current remains at  $-V_2/R$ . Then, when  $\rho$  becomes very nearly zero, the junction voltage may assume any negative value, and the current approaches zero. To obtain the complete solution for  $\rho$  as a function of time, we superpose the steady state value upon the response to a negative current step of magnitude  $(V_1 + V_2)/R$ , with the result

$$\rho G = \frac{V_1}{R} - \frac{V_1 + V_2}{R} (1 - e^{-\omega_h t})$$

At  $t = t_s$ , the excess density has just reached zero.

$$t_s = \frac{1}{\omega_h} \ln \left( \frac{V_1 + V_2}{V_2} \right) \quad (4)$$

Since there is no longer any charge on C, the current will abruptly stop at  $t = t_s$ , according to the lumped model. In reality, we know it dies away smoothly. Hence, in this particular case, the lumped model has predicted zero decay time, which may be explained as follows: Since we have used only one lumped section, we have not included the effect of carriers at some distance from the junction, and it is just these carriers which diffuse back to the junction and cause the exponential type decay. With any finite number of lumped sections, the calculated current will exhibit a discontinuity since  $\rho$  at the junction approaches zero with a finite  $d\rho/dt$ , and causes current through the capacitor nearest the junction which must abruptly cease as  $\rho$  is clamped at  $-p_n$ . This lack of accuracy was introduced because of our attempt to use one lumped section to approximate too large a region of

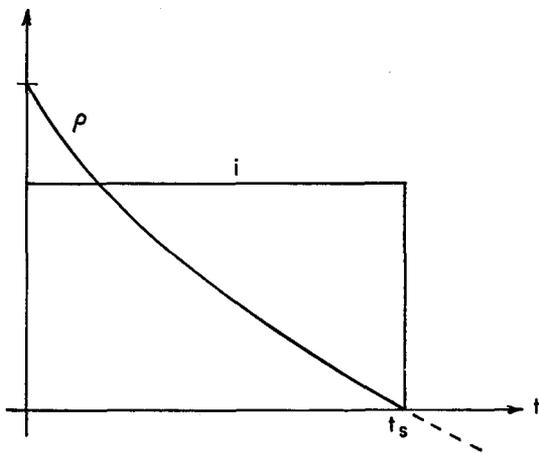


Fig. 8—Recovery characteristic predicted by simple single section model.

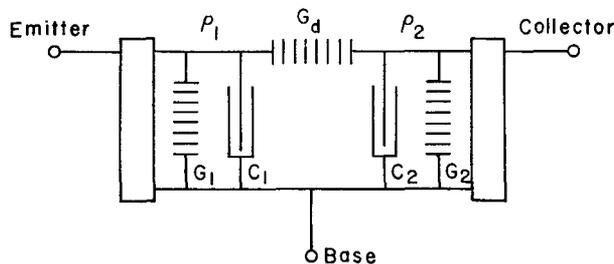
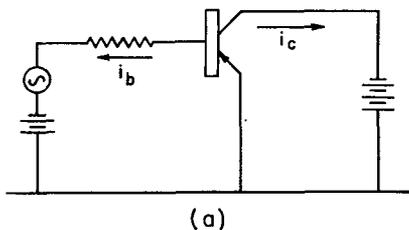
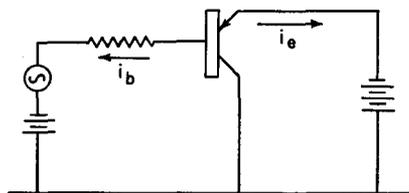


Fig. 9—Complete two-section lumped model of junction transistor with high conductivity collector and emitter regions.



(a)



(b)

Fig. 10—*p-n-p* transistor in (a) normal and (b) inverse connection.

the semiconductor. The problem is especially bad in fast diodes since the lifetime is made very short and consequently the region to be represented by the lumped model is normally many diffusion lengths. On the other hand, in a transistor the base region is only a very small fraction of a diffusion length and the accuracy obtained is very much better. The justification for using the single section diode model is the ease of determining the element values. In practical design work the choice is usually not between a simple or elegant analysis but rather between a simple analysis or none at all.

### Transistor Lumped Model

If the transistor emitter and collector conductivities are high compared to the base conductivity, we may neglect any carrier injection into the emitter and collector and consider only minority carriers in the base region. A two-section model results as shown in Fig. 9. In this figure  $\rho_1$  represents the excess density near the emitter, given by

$$\rho_1 = p_n (e^{q v_{eb}/kT} - 1)$$

where  $v_{eb}$  is the emitter-base junction voltage;  $C_1$  and  $G_1$  represent storage and recombination near the emitter,  $G_d$  represents diffusion from emitter to collector,  $\rho_2$  is the excess density near the collector, given by

$$\rho_2 = p_n (e^{q v_{cb}/kT} - 1)$$

where  $v_{cb}$  is the collector-base junction voltage;  $C_2$  and  $G_2$  represent storage and recombination near the collector. Both voltages are taken positive when the junction is forward biased.

When the transistor is normally biased as shown in Fig. 10a,  $\rho_2 = -p_n = \text{constant}$  and thus no *a-c* current flows through  $G_2$  or  $C_2$ . Therefore, the *a-c* collector current

$$i_c = \rho_1 G_d$$

and the *a-c* base current

$$i_b = \rho_1 (G_1 + sC_1)$$

using the Laplace transform notation. Hence

$$\frac{i_c}{i_b} = \frac{G_d}{G_1 + sC_1} = \frac{G_d/G_1}{1 + s \frac{C_1}{G_1}} = \frac{\beta}{1 + \frac{s}{\omega_\beta}}$$

where  $\beta$  is the low frequency, short circuit, common emitter, current gain and  $\omega_\beta$  is the short circuit, common emitter current gain cutoff frequency. Thus

$$\beta = \frac{G_d}{G_1}$$

$$\omega_\beta = \frac{G_1}{C_1}$$

Since for all reasonable transistors  $\beta \gg 1$ , in all cases of interest  $G_d \gg G_1$ . If the transistor is inverted, i.e., the collector forward biased (acting as an

emitter) and the emitter reverse biased (acting as a collector) as shown in Fig. 10b,  $\rho_1 = -p_n = \text{constant}$  and no *a-c* current flows through  $G_1$  or  $C_1$ .

The *a-c* emitter current

$$i_e = \rho_2 G_d$$

and the base current

$$i_b = \rho_2 (G_2 + C_2 s).$$

Hence

$$\frac{i_e}{i_b} = \frac{G_d}{G_2 + C_2 s} = \frac{G_d/G_2}{1 + s \frac{C_2}{G_2}} = \frac{\beta_i}{1 + \frac{s}{\omega_{\beta i}}}$$

where  $\beta_i$  is the inverted current gain and  $\omega_{\beta i}$  is the inverted cutoff frequency. Thus

$$\beta_i = \frac{G_d}{G_2}$$

$$\omega_{\beta i} = \frac{G_2}{C_2}$$

Since  $\beta_i$  is often quite small, we may make no statement with regard to the relative magnitude of  $G_2$  and  $G_d$ .

By the four simple measurements of  $\beta$ ,  $\beta_i$ ,  $\omega_\beta$  and  $\omega_{\beta i}$ , we are able to determine all of the input elements in terms of one (preferably  $G_d$ ). For many calculations we need not proceed further. However, if we are interested in the voltage across a forward biased junction, we need to determine  $p_n G_d$ . As in the case of the diode, we cannot determine either  $p_n$  or  $G_d$  separately by external measurements. Perhaps the best method of determining  $p_n G_d$  is to measure the *d-c* emitter-base voltage  $v_{eb}$  and the *d-c* collector current  $I_c$  in the normal bias connection.

$$I_c = (\rho_1 + \rho_n) G_d = p_n G_d e^{q v_{eb} / k T}$$

$$p_n G_d = I_c e^{-q v_{eb} / k T} \quad (5)$$

For germanium transistors it is also possible to obtain an approximate value of  $p_n G_d$  from a measurement of  $i_{co}$ , the collector cutoff current when the emitter is open circuited.

$$i_{co} = p_n \left( G_2 + \frac{G_1 G_d}{G_1 + G_d} \right) = p_n G_d \left( \frac{1}{\beta_i} + \frac{1}{1 + \beta} \right)$$

$$\approx p_n G_d \left( \frac{1}{\beta_i} + \frac{1}{\beta} \right)$$

hence

$$p_n G_d \approx \frac{i_{co} \beta \beta_i}{\beta + \beta_i} \quad (6)$$

However,  $i_{co}$  is normally composed of a certain amount of surface leakage current and junction depletion layer generation current. Hence the value of  $p_n G_d$  obtained in this way may be considerably in error. A measurement of  $v_{eb}$  and  $i_c$  at a bias current

large compared to  $i_{co}$  is much to be preferred. In silicon units the  $i_{co}$  is largely determined by carrier generation within the junction depletion region and therefore should never be used in the determination of  $p_n G_d$ .

**Transistor Small Signal Performance.** We have already used the common emitter current gain characteristic of the transistor in order to determine the values of the lumped model elements. It is of interest to investigate the other aspects of small signal performance as predicted by the lumped model. If the transistor is used in the common base connection and normally biased, the *a-c* collector current

$$i_c = \rho_1 G_d$$

and the *a-c* emitter current

$$i_e = \rho_1 (G_d + G_1 + C_1 s)$$

Therefore

$$\frac{i_c}{i_e} = \frac{G_d}{G_d + G_1 + C_1 s} = \frac{\frac{G_d}{G_d + G_1}}{1 + \frac{C_1}{G_d + G_1} s} = \frac{\alpha}{1 + \frac{s}{\omega_\alpha}}$$

where

$$\alpha = \frac{G_d}{G_d + G_1} = \frac{\beta}{1 + \beta}$$

$$\omega_\alpha = \frac{G_d + G_1}{C_1} = (1 + \beta) \omega_\beta$$

Thus the lumped model gives the single time constant approximation for the current gain which is quite accurate for operation well below the alpha cutoff frequency and is commonly used for high frequency calculations. If  $\beta \gg 1$ , we may simplify the last expression as follows:

$$\omega_\alpha \approx \frac{G_d}{C_1} = \beta \omega_\beta$$

In the inverse common base connection similar expressions apply.

$$i_e = \rho_2 G_d$$

$$i_c = \rho_2 (G_d + G_2 + C_2 s)$$

$$\frac{i_e}{i_c} = \frac{G_d}{G_d + G_2 + C_2 s} = \frac{\frac{G_d}{G_d + G_2}}{1 + \frac{C_2}{G_d + G_2} s} = \frac{\alpha_i}{1 + \frac{s}{\omega_{\alpha i}}}$$

$$\alpha_i = \frac{G_d}{G_d + G_2} = \frac{\beta_i}{1 + \beta_i}$$

$$\omega_{\alpha i} = \frac{G_d + G_2}{C_1} = (1 + \beta_i) \omega_{\beta i}$$

where  $\beta_i$  is not necessarily large compared to unity.

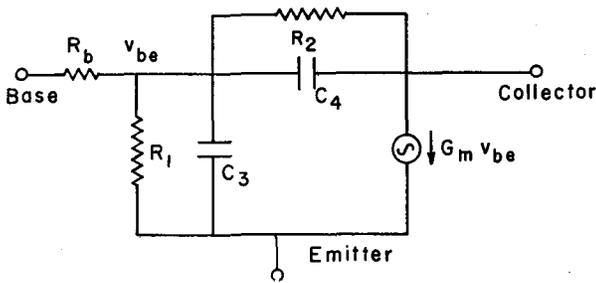


Fig. 11—Transistor small signal equivalent circuit as developed from lumped model.

We may now ask what type of complete common emitter, small signal equivalent circuit results from the lumped model. For small signals, the emitter *a-c* minority carrier density is proportional to the *a-c* emitter-base voltage as shown in equation 3.

$$\rho_1 = \frac{q}{kT} \rho_o v_{be} = K_1 v_{be}$$

The effective *a-c* density at the collector is also proportional to the *a-c* collector-base voltage, due to collector depletion layer widening or Early effect.<sup>(2), (6)</sup>

$$\rho_2 = K_2 v_{cb} \quad K_2 \ll K_1$$

where all quantities of interest are now *a-c* components.

In the common emitter connection, expressions for the base and collector currents become

$$i_c = -\rho_1 G_d + \rho_2 (G_d + G_2 + C_2 s)$$

$$i_b = \rho_1 (G_1 + C_1 s) + \rho_2 (G_2 + C_2 s)$$

Since the emitter voltage is taken as zero, we may rewrite the currents in terms of collector and base voltages.

$$i_c = v_{be} [-K_1 G_d + K_2 (G_d + G_2 + C_2 s)] - K_2 (G_d + G_2 + C_2 s) v_c$$

$$i_b = -v_{be} [K_1 (G_1 + C_1 s) - K_2 (G_2 + C_2 s)] + K_2 (G_2 + C_2 s) v_c$$

These equations correspond to the circuit shown in Fig. 11, where

$$R_1 = \frac{1}{K_1 G_1} \quad R_2 = \frac{1}{K_2 G_2}$$

$$C_3 = K_1 C_1 \quad C_4 = K_2 C_2$$

$$g_m = K_1 G_d$$

The extrinsic base resistance  $R_b$  must be added in series with the base terminal as shown. This circuit is similar to that proposed by Giacometto<sup>(7)</sup> and widely used for high frequency work. Thus, the lumped model reduces simply to a quite accurate representation in this special case, yet is much more general in that it is useful for all transistor operating conditions.

(To be continued)

## Applications Engineering Digests

### APPLICATIONS ENGINEERING DIGEST NO. 50

(Circle 198 on Reader Service Card)

#### Gallium-Arsenide Tunnel Diode Scaler; Philco Corp., Philadelphia, Pa.

Development of high-speed scalers using gallium-arsenide tunnel diodes in series was announced by the Research Division of Philco Corporation. With double-pulse resolution for switching between intermediate states of less than 14 nanoseconds, the device utilizes the characteristic of series-connected tunnel diodes wherein voltage is a multi-valued function of current.

Upon initial application of source current, the stack of diodes—treated

as a two-terminal device regardless of the number of diodes—maintains its lowest voltage. Each pulse of proper amplitude applied to the input terminal boosts stack voltage to the next higher level. The transistor reset circuit is biased to operate when the highest stack level is reached. See Figs. 50.1 and 50.2.

Utilization of GaAs tunnel diodes was encouraged through the devices' in-

trinsically higher voltage swings, their peak-to-valley ratios of greater than ten to one, and switching times of less than a nanosecond.

With the tunnel-diode scaler, extremely high switching and reset speeds are supplemented by significant reduction in space, weight and power requirements in comparison with beam-switching tubes or cascaded transistor binaries used in like applications.

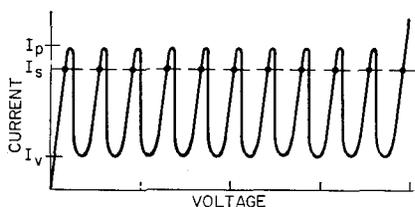


Fig. 50.1—V-I characteristic of tunnel diodes in series.

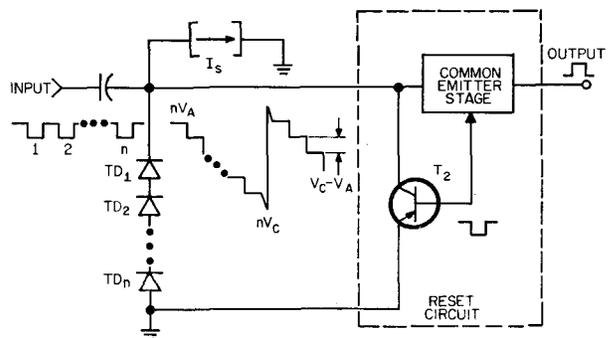


Fig. 50.2—Tunnel diode scaler circuit diagram.