A 160 Kilobit Molecular Electronic Memory Patterned at 10^{11} Bits per Square Centimeter

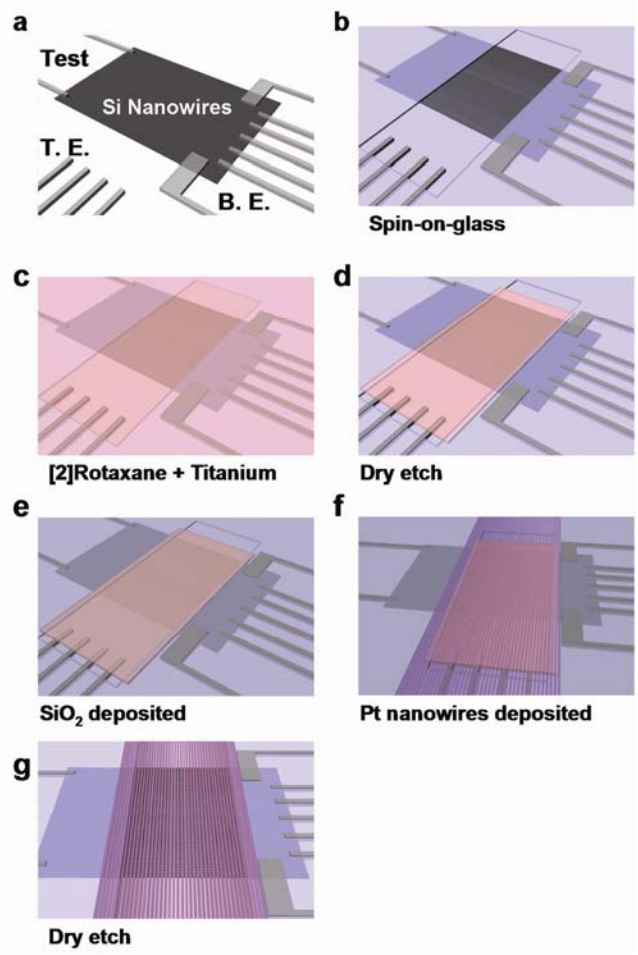
I. SUPPLEMENTARY METHODS

Fabrication and Testing of the Crossbar Molecular Electronic/Nanowire Memory Circuit

A bottom-up approach was the key to the successful fabrication of this memory. This approach both minimized the number of processing steps following deposition of the molecular monolayer, as well as protected the molecules from remaining processing steps. In the following paragraphs, we briefly describe the nanofabrication procedures utilized to construct the memory circuit. A full paper describing these procedures in more detail will be submitted for publication in the near future.

Our 160,000 junction crossbar memory consists of 400 Si nanowire (NW) bottom electrodes of 16 nm width and 16.5 nm half-pitch, crossed with 400 Ti NW top electrodes of the same dimensions, and with a monolayer of bistable [2]rotaxane molecules sandwiched in between. We have previously reported on using the superlattice nanowire pattern transfer (SNAP) technique[19] to fabricate highly ordered arrays of metal and Si NWs[30]. For this work, the SNAP technique was extended to create 400 element NW arrays of both the bottom and top electrode materials, and so was the primary patterning method for achieving the 10^{11} cm^{-2} bit density of the crossbar.

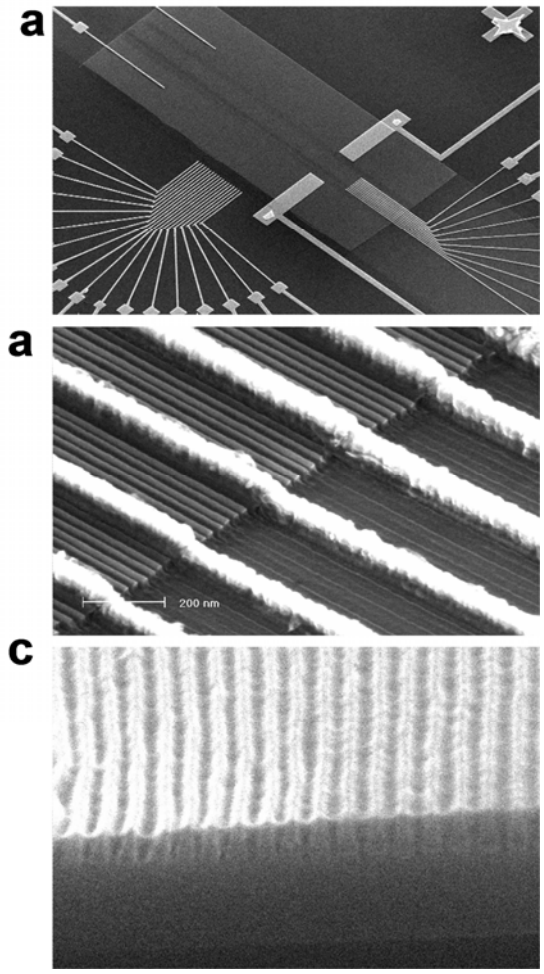
An overview of the process flow used to fabricate the memory is shown in Supplementary Figure 1.



Supplementary Figure 1 | Process flow for preparing the 160 kbit molecular electronic memory circuit at 10^{11} bits/cm^2. a, SNAP-patterned SiNW bottom electrodes are electrically contacted to metal electrodes. **b,** The entire circuit is coated with SiO_2 (using spin-on-glass (SOG)) and the active memory region is exposed using lithographic patterning followed by dry etching. **c,** The bistable [2] rotaxane Langmuir monolayer is deposited on top of the Si NWs and protected via the deposition of a Ti layer. **d,** The molecule/Ti layer is removed except for the active memory region. **e,** A SiO_2 insulator is deposited on top of the Ti film. **f,** An array of top Pt NWs is deposited at right angles to the bottom Si NWs using the SNAP method. **g,** The Pt NW pattern is transferred, using dry etching, to the Ti layer to form an array of top Ti NW electrodes, and the crossbar structure is complete.

Preparation of and contact to the bottom Si nanowire electrodes The Si NW array was fabricated as described previously[19, 30]. The starting wafer for the Si NWs was a 33 nm thick phosphorous doped ($n=5x10^{19}$ cm^{-3}) silicon-on-insulator (SOI) substrate with a 250 nm thick buried oxide (Simgui, Shanghai, China). An array of Pt NWs was transferred onto this substrate using the SNAP method, and reactive ion etching was used to transfer the Pt NW pattern to form a ~2 millimeter long array of Si NWs. The Pt NWs were then removed, and the Si NW array was then sectioned into a 30 μm long region. Electrical contacts to these bottom Si NWs, as well as contacts that are intended for the top Ti NWs were defined at this point using standard electron-beam lithography (EBL) patterning and electron-beam evaporation to produce electrodes consisting of a 15 nm Ti adhesion layer followed by a 50 nm thick Pt electrode (Supplementary Figure 1.a). Immediately prior to metal evaporation, the Si NWs were cleaned using a gentle O_2 plasma (20 standard cubic centimeters per minute (sccm), 20 milliTorr, 10 Watts, 30 seconds) followed by a 5 second dip in an NH_4F/HF solution. After lift-off, the chip was annealed at 450 °C in N_2 for 5 min to promote the formation of ohmic contacts.

Supplementary Figure 2.a shows an SEM image of the device at the stage in which the Si NWs and all of the external electrical contacts have been created. Note that there are four sets of EBL defined contacts. The 18 narrow contacts at the bottom left of the image will eventually connect to the top Ti NW electrodes and are used for testing of the final memory circuit. The 10 narrow contacts to the Si NWs at the bottom right of the image are also used for testing of the memory circuit. Finally there are two narrow test electrodes at the top left and two wide electrodes at the bottom right. The wide electrodes contact about 2/3 of all the Si NWs and serve dual functions. First, they ground unused Si NWs during memory testing (this procedure approximates how a fully multiplexed crossbar circuit would be utilized). Second, when used in conjunction with the



Supplementary Figure 2 | Representative scanning electron micrographs illustrating the crossbar memory fabrication process. a, A 30 micrometer section of the 400 Si NWs with all of the metal contacts to the crossbar top electrodes (not deposited at this stage) and bottom electrodes deposited. **b,** Each EBL-defined metal electrode defined is about 70 nm wide and contacts 2 ~ 4 NWs. **c,** Micrograph verifying that the spin-on-glass layer fills the narrow trenches between the Si NWs. The chip was cleaved after the planarization process to allow for the view shown here.

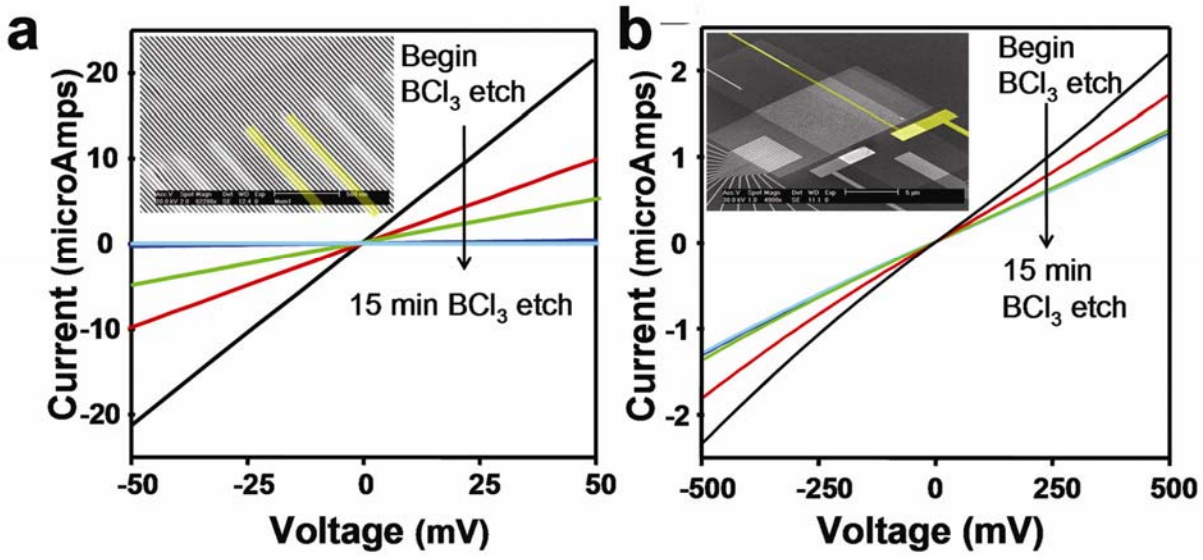
two narrow test-electrodes on the opposite side of Si NW array, they enable testing of the conductivity of the Si NWs throughout the fabrication processes. This testing procedure provided invaluable feedback for finely tuning and tracking many of the fabrication processes. Once these various contacts were established, robust Si NW conductivity was confirmed via current vs. voltage measurements. If the Si NWs were measured to be poor conductors (a very infrequent occurrence), the chip was discarded.

The device was then planarized using an optimized spin-on-glass (SOG) procedure (Accuglass 214, Honeywell Electronic Materials, Sunnyvale, CA). This planarization process is critical because the SOG not only protects Si NWs outside of the active memory region from damage that can arise during subsequent processing steps, but it also

prevents evaporated Ti (explained below) from entering the gaps between the Si NWs where it would be extremely difficult to remove. After globally thinning the SOG layer using a CF_4 plasma (20 standard cubic centimeters per minute (sccm), 10 milliTorr, 40 Watts), an opening in photoresist was lithographically defined over the Si NWs and the tips of the 18 EBL defined contacts. The SOG was then further etched until the tops of the underlying Si NWs were exposed (Fig. (Supplementary Figure 1.b, (Supplementary Figure 2.c). This step was monitored by periodically measuring the Si NW conductivity using the test electrodes. The majority of the dopant atoms in the Si NWs lie within the top 10 nm of the NWs[30, 31]. This feature means it is very straightforward to etch back the SOG without thinning the Si NWs, since the conductivity of the NWs is very sensitive to their thickness. At this stage the entire memory circuit is under SOG (and thus electrically isolated from any further top processing) except for the lithographically defined opening over the Si NWs and the 18 contacts. This opening defines the active memory region.

Deposition of Molecules and Top Electrode Materials A monolayer of bistable [2]rotaxane switches (Fig. 2) was prepared by Langmuir-Blodgett techniques and transferred onto the device as reported previously[20, 32]. 20 nm of Ti was then evaporated over the entire device (Supplementary Figure 1.c). This Ti layer serves to protect the molecules from further top processing. Using photolithographic techniques and BCl_3 plasma etching (10 sccm, 5 mTorr, 30 Watts), the molecule/Ti layer was then everywhere removed except for the memory active region where electrical contact to the underlying Si NWs is made ((Supplementary Figure 1.d). Next, a thin SiO_2 layer was deposited over the entire substrate to isolate the EBL defined electrodes from the Pt NWs deposited in the next step (Supplementary Figure 1.e). Using the SNAP technique, an array of 400 Pt NWs was then deposited over the Ti/SiO_2 layer and perpendicular to the

underlying Si NWs (Supplementary Figure 1.f). Finally, careful BCl_3 plasma etching was used to transfer the Pt NW pattern to the underlying SiO_2/Ti film, thus forming Ti NW top electrodes (Supplementary Figure 1.g). The etch endpoint was determined by monitoring the cross-conductance of the top Ti NWs (Supplementary Figure 3.a). Complete transfer of the Pt NW pattern to the underlying Ti film is indicated by a fall in the cross-conductance to about 10 nS. The cross-conductance does not go to zero since the Ti electrodes, while physically separated, are still electrically coupled through the crossbar junctions and the underlying Si NWs. The health of the underlying Si NWs throughout the Ti-etching steps was also monitored as shown in

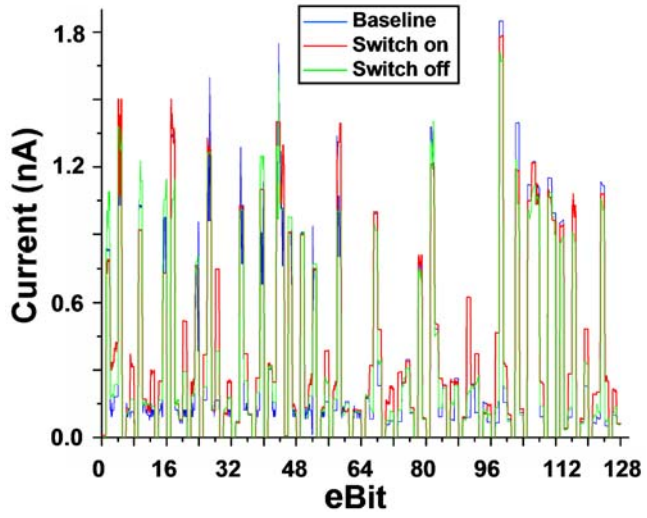


Supplementary Figure 3 | Conductance monitoring during the Ti layer etching. a, Cross-conductance measurements between electrical contacts to the top nanowire array were performed to monitor the Ti layer etching. When the current drops to sub-10 nanoAmps, the top Ti electrodes are separated. The inset SEM image shows two representative contacts to the top Ti electrodes as highlighted in yellow. It is the cross-conductance between such contacts that was used for this measurement. **b,** The conductivities of SiNWs were measured throughout the Ti layer etching to ensure that SiNWs were not damaged. The SEM image (inset) shows the current pathway that was measured.

Supplementary Figure 3.b.

The memory circuit was tested using a custom-built probe card and a Keithley 707A switching matrix for off-chip demultiplexing. Individual ebits (containing between 4 and 16 crossbar junctions, but most often containing 9 crossbar junctions) were electrically addressed within the 2D crosspoint array by the intersection of one Si NW bottom electrode and one Ti NW top electrode. Individual molecular junctions were set to their low resistance or "1" state through the application of a positive 1.5 – 2.3 V pulse (voltages are referenced to the bottom Si NW electrode) of 0.2 s duration. A junction was set to its "0" or high resistance state through application of a -1.5 V pulse, also of 0.2 s duration. To avoid switching an entire column or row of bits, the switching voltage was split between the two electrodes defining the ebit. Thus, to write a "1" with +2 V, a single Si NW electrode is charged to +1 V, while a single Ti NW electrode is set to -1V, and only where they cross does the junction feel the full +2 V switching voltage. Half-selected bits, that is, bits receiving only half the switching voltage, were never observed to switch. Individual ebits were read by applying a small, non-perturbing +0.2 V bias to the bottom Si NW electrode and grounding the top Ti NW electrode through a Stanford Research Systems SR-570 current pre-amplifier. Bits not being read were held at ground to reduce parasitic current through the crossbar array. Note that all the electrical writing and reading operations described herein were done sequentially.

Configuring the memory circuit for information storage proceeded as follows. Initially, all ebits were read to document their baseline current. Then, all ebits were switched to their "1" state, read out, then set to their "0" state and again read out (Supplementary Figure 4 contains the raw data). Good ebits were identified as those with 1/0 current ratios roughly greater than or equal to 1.5. Bad ebits fell into a few classes, with the two most common groups being ebits that wer



Supplementary Figure 4 | The raw data of the memory circuit whose 1/0 is shown in figure 3 in the main text. All of 128 ebits were read and written sequentially as described in the text.

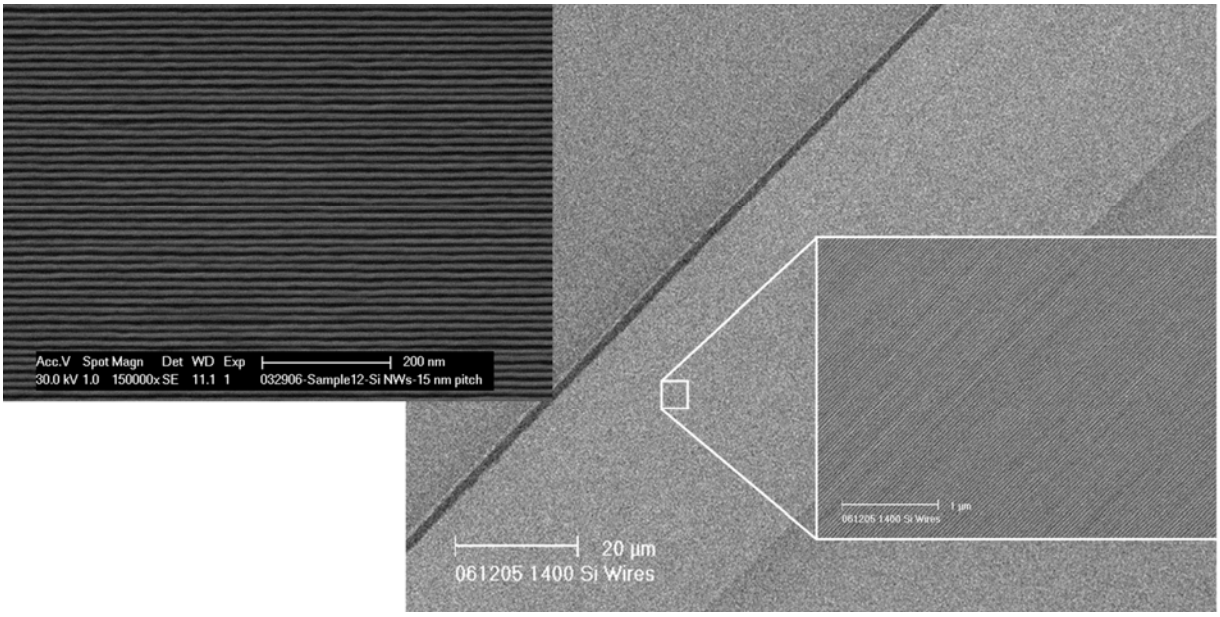
either poor switches with little or no switching response or open circuits. Adjacent, shorted Ti top electrodes were identified when the ebits addressed by those electrodes were not independently addressable. Even though that type of defect is not completely fatal (i.e. two rows of fabricated ebits could still be utilized as a single row), we did not use ebits associated with shorted top electrode defects. Once the good ebits were identified, they were used to store and read out small strings of information written in standard ASCII code. The maximum number of ebits that could be tested was 180, but our electronics were configured to test 128 ebits (< 1% of the actual crossbar), and that was sufficient to demonstrate the key concepts of this memory.

The volatility measurements were carried out by switching selected bits to the “1” or low resistance state, and then reading the current through those bits as a function of time.

II. SUPPLEMENTARY DISCUSSION

Limitations of the SNAP Process for Crossbar Memory Formation

The nanofabrication methods described in the text for creating the 160 kilobit crossbar memory circuit can be significantly extended in terms of both memory size and bit density. For our memories, the crossbar electrode materials choices have proven to be very important for successful memory operation. In other words, Si bottom electrodes and metallic top electrodes with a Ti adhesion layer were key. Metal NWs at 8 nm half-pitch have been reported previously[19]. Such NWs, formed by the SNAP process, only serve as templates for forming the crossbar electrodes. To be used in a crossbar memory, the SNAP NW pattern must be



Supplementary Figure 5 | The limits of SNAP patterning to produce high-density silicon NW arrays for crossbar circuit applications. (left) An array of 7 nm wide Si NWs patterned at 6.5 nm half-pitch. **(right)** An array of 1400 Si NWs patterned at 16.5 nm half-pitch, providing enough NWs to produce an approximately 2 million bit crossbar circuit. The inset shows an expanded view of the array, which is virtually free of defective nanowires.

transferred to Si or Ti NWs for the bottom and top electrodes, respectively. Thus, it is not just the SNAP process, but the ability to translate the initially deposited SNAP NWs to form other NWs that ultimately limits the size and density of the circuitry that can be fabricated. In Supplementary Figure 5 (left micrograph), we present an array of 7 nm wide, 15 nm tall single crystal Si NWs patterned at 6.5 nm half-pitch. This corresponds to a crossbar that would contain approximately 6×10^{11} bits cm^{-2}. While this array may not represent the density limit of what could be achieved, densities in excess of 10^{12} cm^{-2} will be very hard to obtain using these patterning methods.

Similarly, the 160,000 junction crossbar also doesn't represent any sort of limitation. In Supplementary Figure 5 (right two micrographs), we present SEM images of 1400 Si NWs formed using the SNAP method. Such an array size permits the formation of a 2 million bit crossbar, and it is certainly possible to further expand the concept to substantially larger structures. As mentioned in the text, the primary limitation is that the SNAP process is that, while it is a parallel patterning method – since all nanowires within an array are created simultaneously, each array must be fabricated one at a time using a labor intensive process. A single worker, for example, can fabricate only about 20 arrays of Si NWs in a single day. However, recent advances in using nanoimprinting[29] to replicate SNAP nanowires and to form crossbar structures indicate that high-throughput, parallel fabrication methods can be developed, even at the near molecular-densities described in this paper.

Rectification

The amount of rectification is dependent upon the amount of titanium oxidation that occurs at the molecule/Ti interface which, in turn, depends upon the vacuum level of the metal deposition system[33]. For the devices reported here, the Ti was deposited at a pressure of approximately 5e-7

Torr. For isolated devices, but constructed in a fashion similar to what was done here, this typically produces a rectification of about 10:1 at 1 V.

III. SUPPLEMENTARY NOTES

Supplementary Information References

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