Conferences

THE VENERABLE CONVERTER: A NEW APPROACH TO POWER PROCESSING

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ABSTRACT

A regulating dc-to-dc converter is described which utilizes a new circuit configuration to achieve several desirable features including higher efficiency, a single circuit for regulation and conversion, minimized output filter requirements, and simplified control system applications. The dc operating characteristics are derived and the efficiency of the new converter is shown to compare favorably with the conventional boost regulator. An ac model is derived and a comparison is made between analytical and experimental results.

BACKGROUND

The development of the Venable Regulating High Voltage Converter [1] evolved from an IR&D activity authorized in September 1972 at the Hughes Electron Dynamics Division and described at that time as the "Ku-band Multimode TWTA" development program. A prime objective of that program was to achieve efficiency improvements over the conventional boost regulator and dc to dc converter approach for high voltage TWT power processing systems. A novel circuit evolved out of this development program which integrated the regulating and conversion circuits into a single functional block. This circuit enabled the designer to achieve significantly higher efficiencies for high voltage power processors [2].

DESCRIPTION OF OPERATION

DC operation of the Venable Converter may be explained with reference to Fig. 1. The circuit consists of transformer T which couples a secondary load R_o to an input voltage source, V_1, by means of four symmetrically placed switches, Q_1 through Q_4. Current is supplied to T through the switches, and the energy storage inductor, L. Capacitor C_1 provides a local path for large transient currents, and V_1 supplies dc power. Two switches conduct on alternate half cycles, first Q_1 followed by Q_2 and then on the next half cycle, Q_3 followed by Q_4. Not more than one switch conducts at any time. The switch conduction sequence is illustrated in Fig. 2. Operation of the circuit can be readily understood by investigation of two special cases.

First assume that only the outer switches Q_2 and Q_4 conduct. In this case we have the typical converter operation with a steady dc current I_3 and the voltage at the load, V_o is approximated by $(N_o/N_1)V_1$.*

*Rectifier-diode voltage drops and switch saturation drops are neglected.

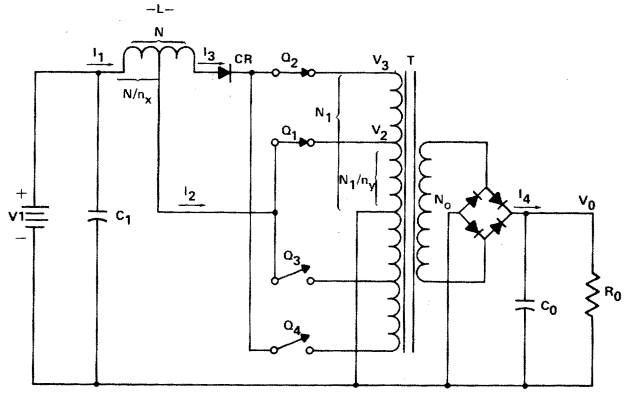

Figure 1 Schematic diagram - the Venable Converter.

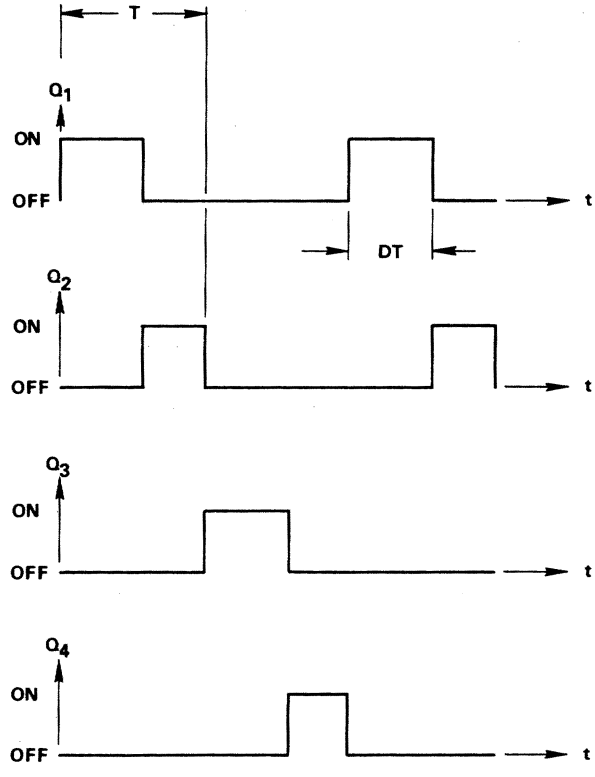

Figure 2 Switch conduction versus time.

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The other extreme case assumes that only the inner switches Q_1 and Q_3 conduct. In this event the output voltage is given by $(N_o/N_1)n_y V_1$.

It is thus seen that the load voltage can be varied a factor of n_y:1 depending upon whether the outer or inner switches provide the switching action. Allowing the inner switch to conduct for a part of the cycle, Δt, and then the outer switch to conduct for the remainder of the half cycle, it is realized that the load voltage must achieve a value

$$\frac{N_o}{N_1} V_1 < V_o < n_y \frac{N_o}{N_1} V_1 \qquad (1)$$

The output voltage, V_o, can indeed be made to vary between these limits by varying the conduction duty ratio D. The circuit may be thought of as an inverter with a continuously variable primary to secondary turns ratio.

At the instant of switching, e.g., Q_1 conducting to Q_2 conducting, ampere-turns of L are conserved. That is, $NI_3 = N/n_x\, I_2$. The special case where $n_x = n_y$ is of particular interest for a practical circuit and exhibits many desirable features.

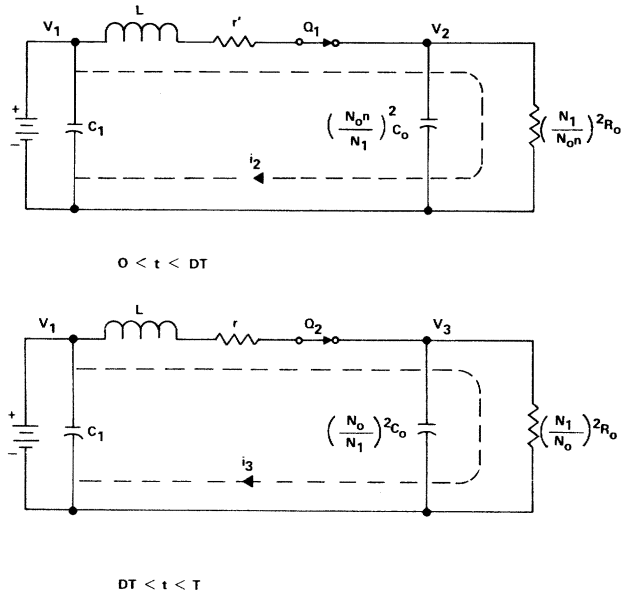


Figure 3 Simplified models for the two states of the Venable Converter.

Desirable Features of the Venable Converter

For the case where $n_x = n_y$:

a. The pulsewidth modulated converter produces a square wave output with continuous load current thus minimizing load filtering problems.
b. The duty ratio transmission function V_o/d is linear and has both a corner frequency, f_o, and peaking, Q, independent of the dc duty ratio D.
c. The duty ratio transmission function has no left or right half-plane zero.

In the general case:

a. High efficiency is achieved by transferring the bulk of the power through the diode-free path of switches Q_1 and Q_3.
b. A single circuit may be used for both load voltage regulation and dc-to-dc conversion.
c. Switches are current-fed thus minimizing switching current transients and reducing power switch stress.

Derivations of Operating Equations

The switch conduction sequence of Fig. 2 is not achieved by applying base drive to the transistors in the sequence shown. Due to the switching action of diode CR, base drive can be supplied to an outer switch before basedrive is removed from the corresponding inner switch. It can be shown that the current in the outer switches I_3 is equal to zero whenever an inner switch is turned on by looking at the voltage across the diode CR.

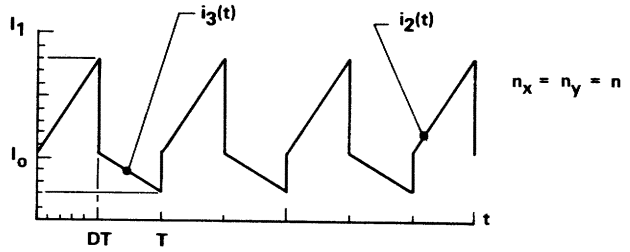


Figure 4 Energy storage inductor current.

For the original Venable Converter in which $n_x = n_y = n$; the voltage across the diode while both inner and outer switches are turned on is

$$V_4 - V_3 = (1 - n)V_1 \qquad (2)$$

Hence, for all values of $n > 1$, which defines the Venable Converter, the diode is back biased as long as the inner switch is conducting. For this period of time lasting DT during each half cycle the inductor current $I_1 = I_2$. When Q_1 turns off the energy stored in the inductor forces the voltage V_4 to rise until the diode CR conducts, clamping the inductor to V_3. For the remainder of the half cycle lasting (1 - D)T the inductor current $I_1 = I_3$. Simplified models for both of these states are shown in Fig. 3.

If the forward voltage of the diode and the saturation voltage of the switches is ignored, for state 1, $0 < t < DT$, the following differential equation may be written:

$$V_1 = L' \frac{di_2}{dt} + i_2 r' + V_2 \qquad (3)$$

where

$$L' = L/n^2 \qquad (4)$$

and r' is the lumped resistive losses for the inner switch current loop. Equation (3) has a solution of:

$$i_2(t) = \left(\frac{V_1 - V_2}{r'}\right)(1 - e^{-t/\tau'}) + I_o e^{-t/\tau'} \qquad (5)$$

where $\tau' = L'/r'$ and I_o is an arbitrary choice of initial current. For state 2, $DT < t < T$, the following differential equation may be written:

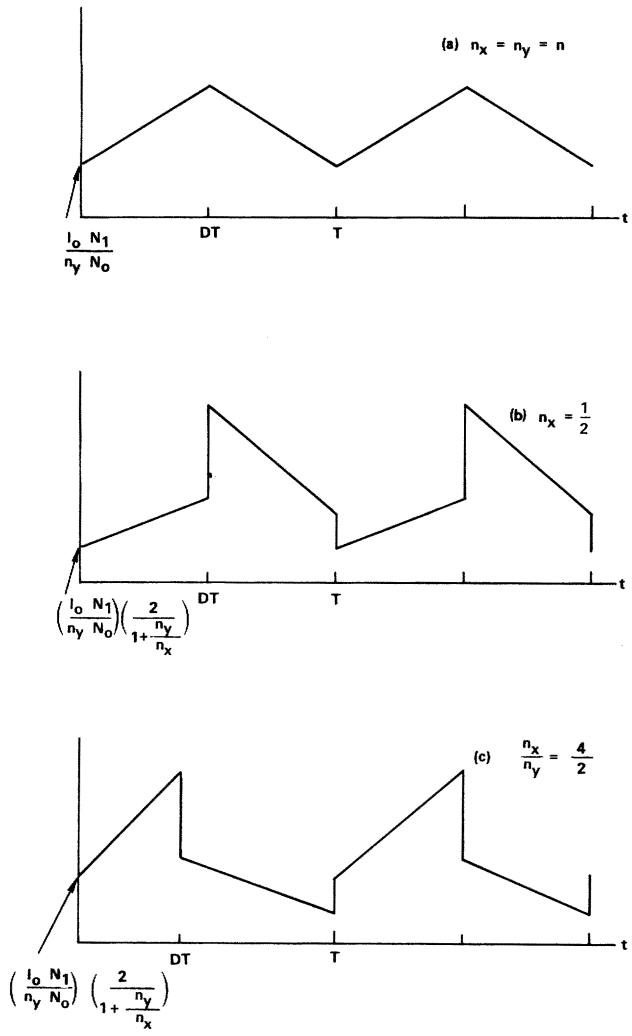


Figure 5 Output Current

$$V_1 = L\frac{di_3}{dt} + i_3 r + V_3 \tag{6}$$

where r is the lumped resistive losses for the outside switch loop. Equation (6) has a solution of:

$$i_3(t') = \left(\frac{V_1 - V_3}{r}\right)(1 - e^{-t'/\tau}) + i_3(0^+)e^{-t'/\tau} \tag{7}$$

where $\tau = L/r$ and $t' = t - DT$.

The initial condition $i_3(0^+)$ is related to $i_2(DT)$ by the conservation of energy requirement for inductor L.

$$\frac{1}{2}L'[i_2(DT)]^2 \equiv \frac{1}{2}L[i_3(0^+)]^2 \tag{8}$$

Substituting equations (4) and (5) into equation (8) and solving for $i_3(0^+)$:

$$i_3(0^+) = \left(\frac{V_1 - V_2}{nr'}\right)[1 - e^{-(DB/\tau')}] + \frac{I_o}{n}e^{-(DT/\tau')} \tag{9}$$

Hence,

$$i_3(t') = \left(\frac{V_1 - V_3}{r}\right)(1 - e^{-t'/\tau}) + \left\{\left(\frac{V_1 - V_2}{nr'}\right)[1 - e^{-(DT/\tau')}] + \frac{I_o}{n}e^{-(DT/\tau')}\right\}e^{-t/\tau} \tag{10}$$

Because of the symmetry of the converter the solutions for $i_2(t)$ and $i_3(t)$ also apply for switches Q_3 and Q_4.

Even though equations (5) and (10) are open ended because of the arbitrary choice of initial current I_o they reveal a great deal about the nature of the energy storage inductor current I_1. In the practical Venable Converter L is chosen to be sufficiently large so that continuous current, $I_1 > 0$, is maintained. In addition r is kept small for reasons of efficiency. As a result both time constants τ and τ' are very large compared to the half cycle switching period T. Equation (5) which applies between the time interval of 0 and DT indicates that the inductor current starts at I_o and ramps at a slope proportional to the difference between the input voltage and the inner tap transformer voltage.

The inner tap voltage is designed to be less than the minimum line voltage which results in a positive slope for $i_2(t)$. When the coefficients of the exponential terms in equation (5) are equal the slope of the current is zero and this defines the minimum permissible line voltage. Equation (10) applies between the interval of DT and T and indicates that the inductor current drops to a level 1/n of the level prior to Q_1 turning off and then ramps at a slope proportional to the difference between the input voltage and the outer tap transformer voltage. The value of n is chosen such that the outer-tap transformer voltage V_3 is greater than the maximum line voltage. This results in a negative slope for $i_3(t)$. Again, when the coefficients of the exponential terms are equal the slope of the current is zero and this defines the maximum permissible line voltage. Fig. 4 depicts this energy storage inductor current waveform for $n = 2.5$ at some nominal line voltage which is greater than V_2 but less than V_3.

It is informative at this time to also look at the output load current I_4. At the instant before Q_1 turns off:

$$I_4(DT^-) = \frac{N_1}{nN_o}I_2(DT) \tag{11}$$

also at the instant after Q_1 turns off;

$$I_4(DT^+) = \frac{N_1}{N_o}I_3(0) \tag{12}$$

Substituting equation (5) into equation (11) and equation (10) into (12) it can be shown:

$$I_4(DT^+) = I_4(DT^-) \tag{13}$$

The same exercise can be performed for the switching interval between Q_2 and Q_3 to show that:

$$I_4(0^+) = I_4(0^-) \tag{14}$$

Thus the output current as seen by the load is continuous as shown in Fig. 5a. This might appear to be trivial in the light of the inductive feed nature of

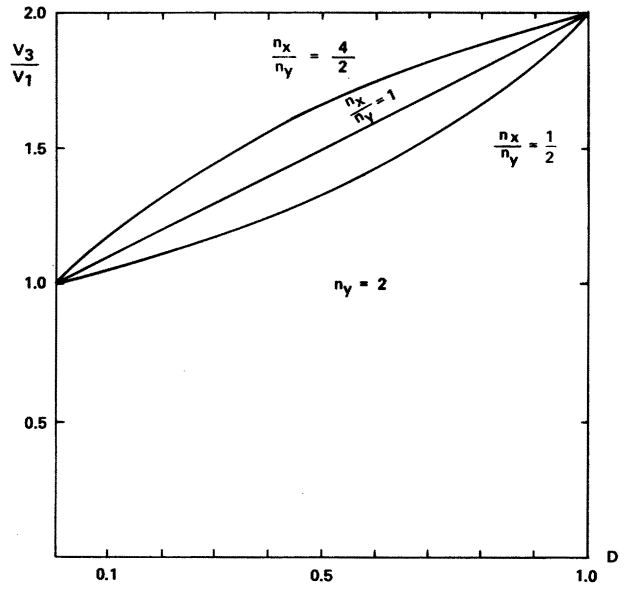


Figure 6 DC control function with different ratios of $\frac{n_x}{n_y}$

the converter. However, the output current is continuous only for the original Venable Converter where $n_x = n_y$. For the generalized converter where $n_x \neq n_y$ it can be shown that:

$$I_4(DT^+)n_x = I_4(DT^-)n_y \tag{15}$$

and

$$I_4(0^+)n_y = I_4(0^-)n_x \tag{16}$$

Thus there is a step in the load current which is proportional to the ratio of n_x to n_y. Fig. 5b and 5c show the output current for $n_x > n_y$ and $n_x < n_y$ with all other parameters including n_y constant.

Continuous output current was one of the principal motivations for the development of the Venable Converter. The primary application of this converter was to generate the high voltage necessary to power a traveling wave tube. These tubes require very small ripple, typically less than 0.01 percent, and it is desirable to accomplish this with a minimum of high voltage energy storage. The Venable Converter implemented with equal turns ratio ($n_x = n_y$) has a continuous output current that can be filtered without inductors and with a minimum of capacitance.

In addition there is a definite advantage for this configuration in terms of the ac control function as is explained in a later section.

The dc control function of the converter may be derived by applying Faraday's Law to the voltages across the energy storage inductor during a half cycle T. During the time period DT the voltage across L is given by equation (3) which when substituted into Faraday's Law yields:

$$\left(V_1 - \frac{V_3}{n_y}\right) n_x = \frac{N\Delta\phi}{DT} \tag{17}$$

The voltage across L during the period (1 - D)T, neglecting the diode drop, is $V_3 - V_1$ which yields:

$$V_3 - V_1 = \frac{N\Delta\phi}{(1 - D)T} \tag{18}$$

Since on the average the voltage time product (Flux Change) seen by L must be zero, we may write:

$$\left(V_1 - \frac{V_3}{n_y}\right) n_x D = (V_3 - V_1)(1 - D) \tag{19}$$

Solving for V_3/V_1 we find:

$$\frac{V_3}{V_1} = \frac{D(n_x - 1) + 1}{\left(D\frac{n_x}{n_y} - 1\right) + 1} \tag{20}$$

Equation (20) is the dc control function for the generalized Venable Converter and is shown in Fig. 6 for different ratios of n_x/n_y. It can be seen that for the original Venable Converter where $n_x = n_y = n$ equation (20) reduces to:

$$\frac{V_3}{V_1} = D(n - 1) + 1 \tag{21}$$

which is a straight line equation with a slope of $(n_x - 1)$ and a zero intercept of 1.

This well controlled linear relationship between dc gain and duty cycle is shown in Fig. 7 for various values of n. The autotransformer nature of the Venable Converter is evident. With the exception of noise sensitivity (PWM jitter) linearity of the dc control function is of little consequence. However, it is highly desirable if some form of feed forward correction or voltage programming is required.

AC Model

A continuous, low frequency small signal model may

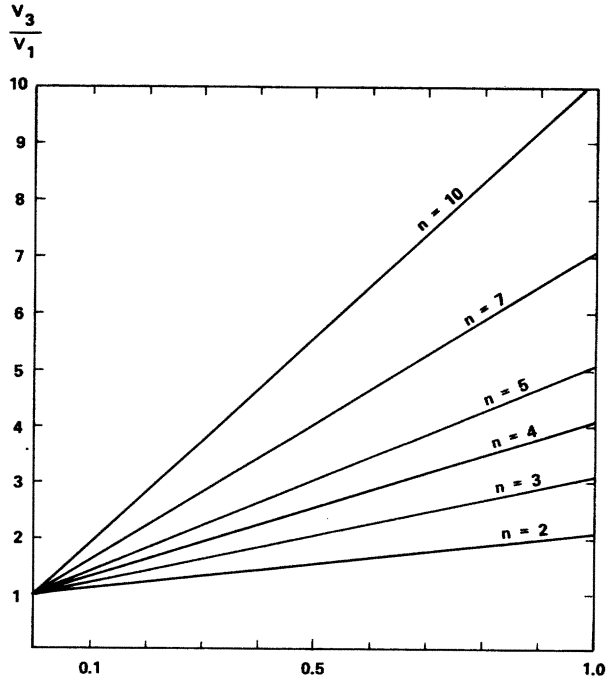


Figure 7 DC control function for the original Venable Converter.

be derived for the original Venable Converter in which the inductor tap ratio and the transformer tap ratio are identical. The model for the general converter where the tap ratios are not the same is treated in the appendix. The method used to develop the model was that of Middlebrook and Wester [3],[4] in which the several different lumped linear models that apply in successive phases of the switching cycle are replaced by a single lumped linear model whose element values are appropriate averages over a complete cycle of their successive values within the cycle. The resulting "averaged" model permits both the input-to-output ("line") and duty ratio-to-output ("control") transfer functions to be easily obtained for both dc (steady state) and superimposed ac (describing function) inputs. The nature of the model derivation inherently restricts the validity to frequencies below about half the switching frequency, and model linearity is ensured by independent restriction of the superimposed ac signal to small amplitudes. The result is therefore a small-signal, low frequency, averaged model.

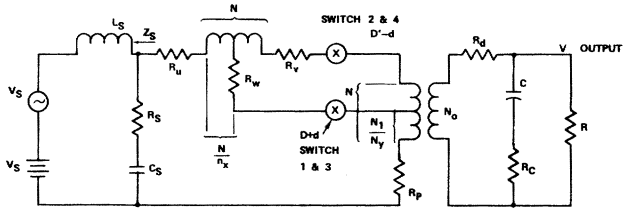


Figure 8 Basic circuit with "dc transformer".

Development of the ac Model

The ac model is developed from the schematic of Fig. 1. The model is manipulated into the configuration of Fig. 8 by assuming an ideal transformer which is good at dc and exploiting the mirror symmetry of the switch positions. The schematic of Fig. 1 has been expanded in the model to include the equivalent series resistance, R_S, of the filter capacitor and a line inductor, L_S in order that the important interaction between the Venable Converter and a typical line filter may be examined.

The model of Fig. 8 is in a form where the switching action may be evaluated with a minimum of complication. The switches 1 and 3 are driven by the duty ratio D + d and switches 2 and 4 are driven by the complementary duty ratio D' - d. The model of Fig. 8 also shows a number of parasitic resistors which are present in real converters. It is readily seen that any ohmic loss in a real converter may be lumped in with one of these parasitic resistors. As an example, R_v actually comprises the resistance of the right hand side of inductor L plus saturation loss in switches 1 and 2 plus the diode saturation loss, plus the resistance of the outer portion of the transformer winding. Each of these resistors will be found in the final model so that the effect of each will be apparent.

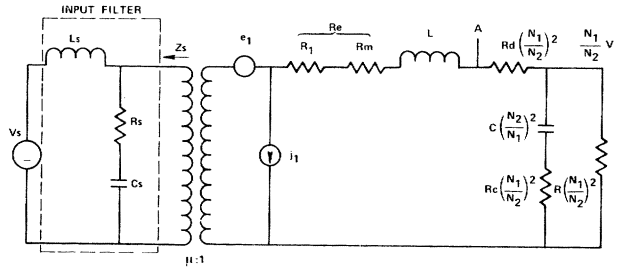
The completed model of the Venable Converter is presented in Fig. 9. The model includes the effects of the averaging filter (L and C), input filter, and all loss elements. From this model the control transfer function and the line transfer function may be derived. In addition, the model includes the effects of storage time modulation of the switching transistors. The model is good for any average duty ratio D. This model is, however, good only for the original case where $n_x = n_y$ (the general case is considered in the appendix).

The model clearly shows that for the original case the averaging filter is not dependent on average duty ratio and the only zero present in the control transfer function is the real left half plane zero due to the ESR of the capacitor R_c and the resistor R_d. The averaging filter is damped by R_1, R_d, and R_M in addition to damping terms due to R. The term R_M represents the damping contribution of the transistor storage time modulation with changing duty ratio [5], and R_M is only present in the ac model in recognition of which R_M is enclosed in an oval. R_1 and R_d however, are ohmic losses which must be considered in the evaluation of the model at dc.

Notice that the ohmic resistance was separated into two parts, viz., R_1 and R_d and the R_d component was not lumped into the effective damping resistor R_e. This is necessary in the model for many practical applications where the feedback for the control amplifier is derived from the transformer primary (point A in the model). In that case R_d forms an important zero in the feedback factor.

Any desired input filter may also be included in the model as shown in the box of Fig. 9. A typical input filter will have a capacitor output in order to provide a stiff source for the switching currents which were shown in the first section.

In consideration of the effect of the input filter the exact behavior of the two generator model of Fig. 9 may not be apparent. The model is ideal for computer analysis but a good deal of physical insight may be lost because of the interacting voltage and current source. A single generator model was therefore developed which shows more clearly how one can get into trouble if the effects of the input filter are not carefully considered. The single generator model is shown in Fig. 10. Notice that only the control describing function is included. This model was derived from Fig. 9 by forcing the line input, V_s, to zero and using Thevenin and Norton transformations to obtain a single generator V_g. Note that the source impedance appears in the expression for V_g. This is a result of the phase of the current source in Fig. 9 and accurately depicts the apparent negative input impedance of the switching regulator. The term $1 - Z_s/\mu^2 R$ which mul-



$\mu = 1/Dn_x + D'$ where $D' = 1-D$

$R_1 = Dn_x^2R_x + D'R_y + DD'(n_x-1)^2R_s$

where $R_x = R_u + R_w + R_p$

$R_y = R_u + R_v + R_p$

$e_1 = (n_x-1)V_s d + [(D-D')(n_x-1)^2R_s-(n_x^2R_x-R_y)]i_e d \cong (n_x-1)V_s d$

$j_1 = \frac{(n_x-1)V_s d}{(R_1+Rd+R)\mu} \cong \frac{(n_x-1)V_s d}{\mu R}$

Figure 9 Complete model for Venable Converter.

tiplies the control function must be investigated thoroughly lest an unseemly notch appear in the transfer function. The single generator model also has L and C independent of duty ratio as in the two generator model but now one may make reasonable approximations to the control function with only a hand calculator or reactance graph paper.

To verify these results, experimental data were obtained for the control describing function. Tap ratios $n_x = n_y = 4$ were selected and the converter was operated at 27 KHz. The values used were $Z_s = 0$, L = 3.5 mH, C = 10 μF, and R = 300 Ω. Magnitude and phase measurements were obtained by techniques described in [7] and [8]. The predicted filter corner frequency is constant at $f = 1/2\pi$ LC = 850 Hz. The measured and predicted result is shown in Fig. 11 for three duty ratios, D = 0.57, 0.43, and 0.28, in which

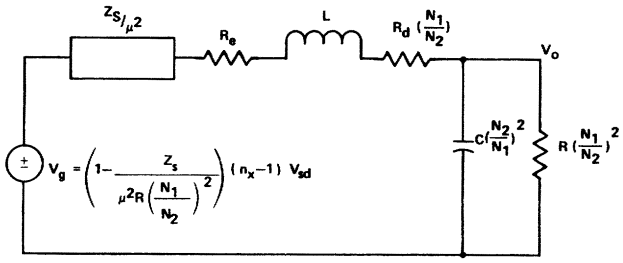


Figure 10 Simplified ac model of control function.

an arbitrary scale factor is used to separate the three sets of results. It is seen that the experimental data points confirm that the corner frequency is constant, independent of D, and that there is no zero within the frequency range of interest. The slight differences in Q factor result from dependence of the effective damping resistance $R_e + R_M$ upon D and are second order effects.

To verify the input filter effect, an input filter and duty ratio were chosen so that at some frequency

$$Z_s/\mu^2 R = 1$$

where one would expect a notch in the control function. The input filter chosen was an L section with L_s = 0.8 mH, C_s = 10 μF and R_s = 3Ω as shown in Fig. 9. For the values chosen there should be a null in the duty ratio transmission function at f = 1.8 KHz and D = 0.78. The computer predicted results of both magnitude and phase are shown in Fig. 12. The experimental result shows a null at f = 1.8 KHz for D = 0.73 and that is shown also in Fig. 12. These results are in extremely good agreement.

General Aspects of Efficiency

The majority of dc to dc converter losses can be grouped into two categories. The first are resistive losses which are primarily a function of the processed power level. The second are power invariant fixed losses that are primarily a function of the converter type. These fixed losses are ideal for comparing one converter type to another while giving some insight into their inherent efficiencies.

The Venable Converter has primarily been used for high voltage applications where efficiency, regulation and ripple are of prime concern. An alternative to the Venable Converter for this application is a boost regulator followed by a simple dc to dc converter. This configuration can achieve low ripple without the necessity of an energy storage inductor on the high voltage output. It can also be implemented for closed loop regulation rather simply with relatively high efficiency. Fig. 13 depicts this converter.

To compare the fixed losses of the Venable Converter to the boost regulator/converter the energy storage inductor current for both converters is simplified to that shown in Fig. 14a and 14b. Assume that both the boost and Venable Converters are designed to operate at the same voltage, frequency and power levels using identical components. To set boundaries on the comparison assume: $1 \geq (V_3/V_1) \geq 2$ so that $n_x = n_y = 2$.

For the Venable Converter the average energy storage inductor current is;

$$I_{avg} = \frac{I_c + I_d}{2}\left(D + \frac{1 - D}{n}\right) = \frac{P_{in}}{V_1} \tag{22}$$

The fixed loss in the two outside transistors, Q_2, Q_4 consists of saturation loss and base drive loss. The saturation loss is given by:

$$PQ_2 + PQ_4 = V_{sat}\frac{I_{c/n} + I_{d/n}}{2}(1 - D) \tag{23}$$

Substituting equation (22) and the dc gain function of equation (21) into equation (23) yields the fraction of input power lost to transistor saturation.

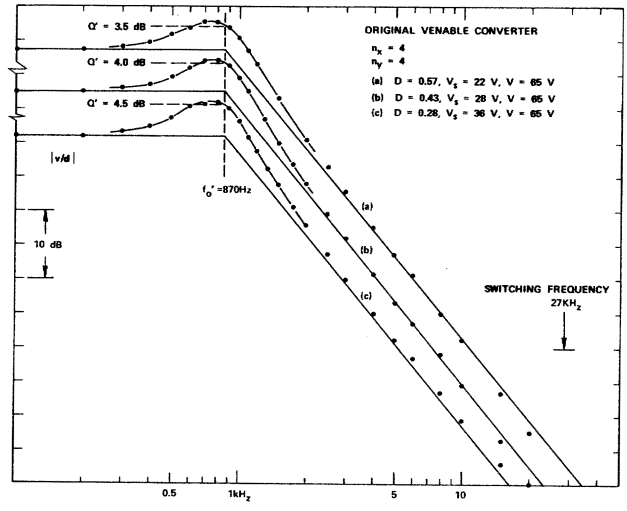


Figure 11 Predicted and measured frequency response for three values of D.

$$\frac{PQ_2 + PQ_4}{P_{in}} = \frac{V_{sat}}{V_3}(1 - D) \tag{24}$$

If we assume that the transistors are driven in proportion to their collector current at a fixed forced beta, the base drive loss is given by:

$$\frac{PQ_2 + PQ_4}{P_{in}} = \frac{\beta_f V_{sat} + V_{BE}}{\beta_f V_3}(1 - D) \tag{25}$$

where $\beta_f = I_c/I_B$.

In a similar manner the losses in the inside transistors can be shown to be:

$$\frac{PQ_1 + PQ_3}{P_{in}} = \frac{\beta_f V_{sat} + V_{BE}}{\beta_f V_3} \text{ (DN)} \tag{26}$$

The loss in the power diode is related to the diode forward drop V_F:

$$\frac{P_{CR}}{P_{in}} = \frac{V_F}{V_3}(1 - D) \tag{27}$$

Equations (25), (26), and (27) represent the power invariant fixed losses expressed as a fraction of input power, for the Venable Converter. The boost regulator/converter in comparison has an average storage inductor current of:

$$I_{avg} = \frac{I_a + I_b}{2} = \frac{P_{in}}{V_1} \tag{28}$$

and the dc gain function, neglecting the diode drop, is:

$$\frac{V_3}{V_1} = \frac{1}{1 - D_B} \tag{29}$$

where: $D_B = t/T$.

Applying equations (28) and (29) to the V_{sat} and V_F losses in a boost regulator, the following fixed losses can be calculated.

Boost transistor

$$\frac{PQ_1}{P_{in}} = \left(\frac{\beta_f V_{sat} + V_{BE}}{\beta_f V_3}\right)\left(\frac{D_B}{1 - D_B}\right) \tag{30}$$

Static Inverter Transistor

$$\frac{PQ_2 + PQ_3}{P_{in}} = \left(\frac{\beta_f V_{sat} + V_{BE}}{\beta_f V_3}\right)\left(\frac{D_B}{1 - D_B}\right) \tag{31}$$

Boost Diode

$$\frac{P_{CR}}{P_{in}} = \frac{V_F}{V_3} \tag{32}$$

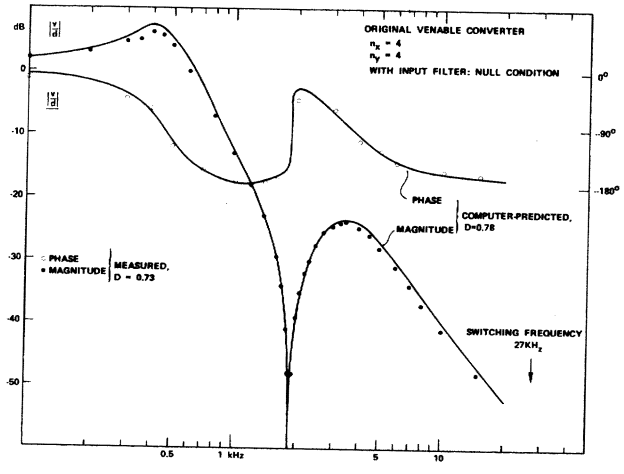


Figure 12 Predicted and measured frequency response showing effect of input filter at null condition.

These fixed loss equations can be compared for the two converter types by knowing the relationship between D and D_B.

Setting equation (29) equal to equation (21) and solving for D yields:

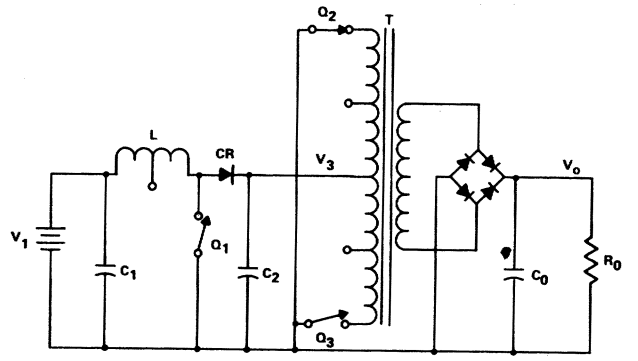


Figure 13 Boost regulator dc-to-dc converter.

$$D = \frac{D_B}{(n - 1)(1 - D_B)} \tag{33}$$

Which under the boundaries set for this comparison, n = 2, reduces to:

$$D = \frac{D_B}{(1 - D_B)} \tag{34}$$

With equation (34) substituted into equation (30) the comparison is complete. Table 1 lists these fixed loss elements for both converters.

It can be seen that the V_F and V_{sat} loss of the power diode and outside transistors is less for the Venable Converter for $D > 0$. On the other hand, the PWM transistor losses are n (2) times greater on the Venable Converter. A numerical example will best illustrate the relationship of these losses.

Assume: $V_{sat} = 0.2V$
$V_F = 1V$
$V_{BE} = 1V$
$V_3 = 40V$

Figure 15 graphs the loss elements as a function of duty cycle.

The Venable Converter shows an obvious advantage over the regulating boost converter. This is primarily because the boost regulator processes all of its power via the power diode whereas the Venable Converter has direct conversion via the PWM switches. In terms of efficiency for high power converters, only the direct conversion PWM inverter is superior. However, this type of converter is not suitable for high voltage power processing because the energy storage inductor which is required at each output must operate at a very high voltage. In addition, the current from this type of converter has a larger ac component so more extensive filtering is required for the same input current ripple as an equivalent Venable Converter.

The Venable Converter demonstrates bulk efficiencies from dc input power to high voltage output power of greater than 91 percent. This has been achieved under varying conditions of line, load and temperature.

Fig. 16 shows typical bulk efficiencies at the 35

and 100 watt level. Complete power processing systems for traveling wave tube amplifiers have typical efficiencies of greater than 85 percent.

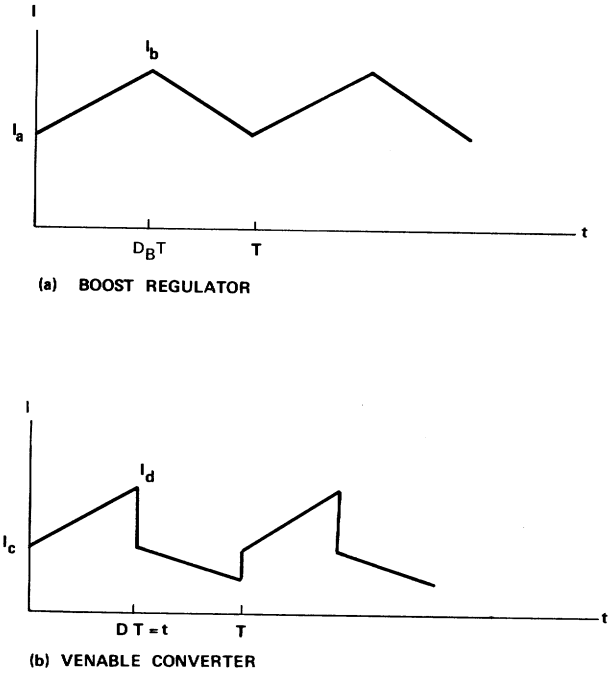


Figure 14 Simplified energy storage inductor current.

SUMMARY

A new circuit configuration, the Venable Converter, has been presented which offers certain advantages over the conventional boost-regulator/converter approach to power processing. Their advantages are especially meritorious when high-voltage outputs are desired due to the continuous current characteristic of the load current.

TABLE 1
VENABLE/BOOST POWER INVARIANT FIXED LOSS ELEMENT COMPARISON

LOSS ELEMENT	LOSS IN PERCENT	
	BOOST	VENABLE
V_F Power Diode	$\frac{V_F}{V_3} \times 100$	$\frac{V_F}{V_3}$ (1-D) x 100
V_{sat}^{PWM} Transistor(s)	$\frac{\beta_f V_{sat} + V_{BE}}{\beta_f V_3}$ (D) x 100	$\frac{\beta_f V_{sat} + V_{BE}}{\beta_f V_3}$ (DN) x 100
V_{sat} Outside Transistors	$\frac{\beta_f V_{sat} + V_{BE}}{\beta_f V_3} \times 100$	$\frac{\beta_f V_{sat} + V_{BE}}{\beta_f V_3}$ (1-D) x 100

The operating equations have been derived to provide analytical expressions for switching current, maximum and minimum line voltage, and the dc gain function.

A continuous, low frequency, small signal model is presented in two forms: a dual generator model suitable for computer analysis and a single generator model more amenable to hand calculator or reactance chart analysis. It is shown that the original ($n_x = n_y$) Venable Converter has significant advantages of control system applications due to the linear characteristic of the control

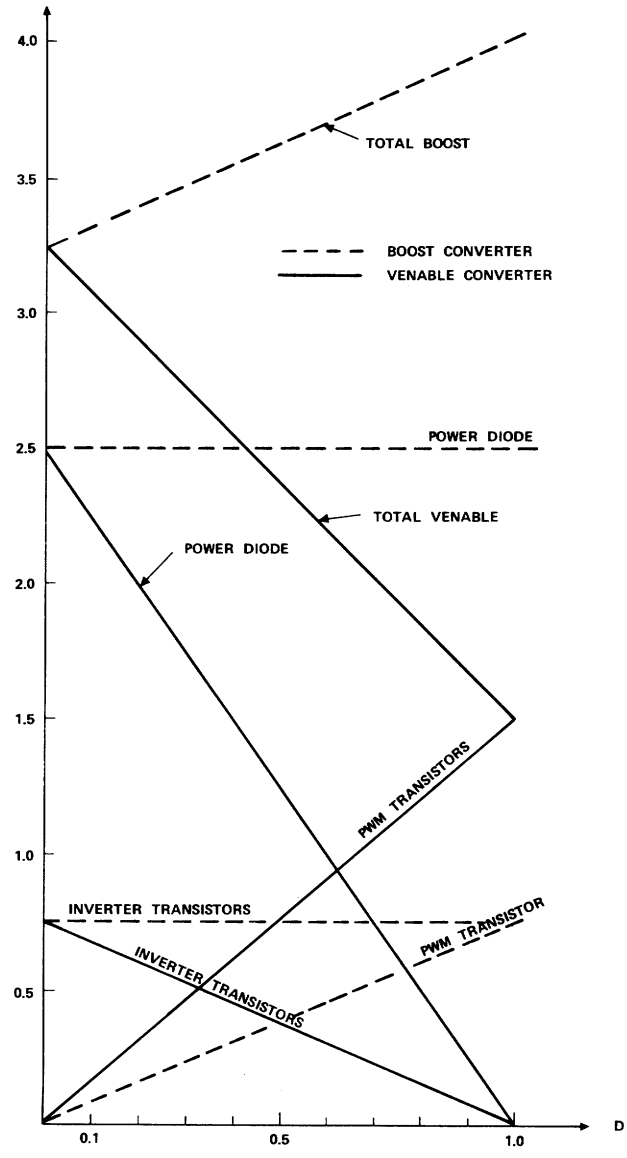


Figure 15 Venable/Boost power invariant fixed loss elements as a function of duty cycle.

transfer function, the lack of right or left half-plane zeros and the fact that the corner frequency and damping are independent of duty cycle.

Experimental data are presented and excellent correlations are obtained from the computer model. The potential problem of loop instability due to nulls in the control transfer-function arising out of the input filter impedance is pointed out.

Finally, a detailed fixed loss comparison between the original Venable Converter configuration and the conventional boost/regulator conversion is made. The results of this comparison show that higher efficiencies are possible with the Venable Converter due to reduced power-diode losses at high conduction duty cycles. Regulated conversion efficiencies of 91 percent have been achieved under varying conditions of line, load and temperature.

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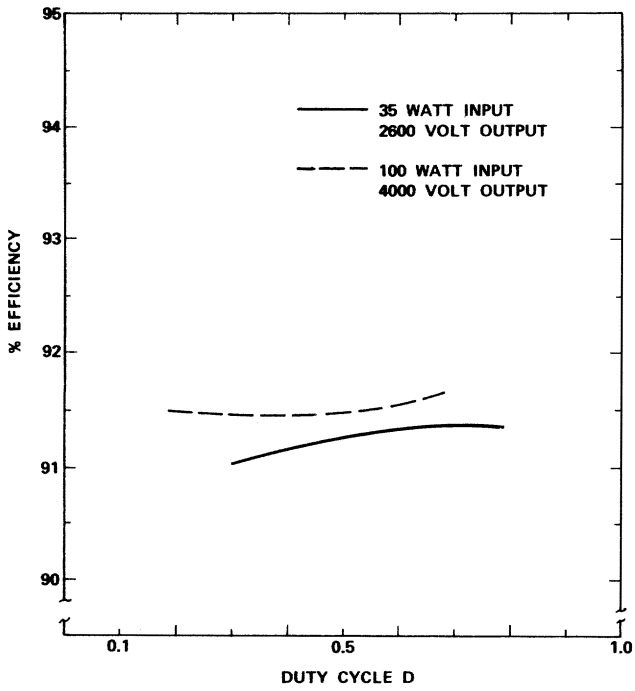

Figure 16 Efficiencies of Venable Converter at 35 watts and 100 watts.

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APPENDIX

AVERAGED MODEL OF THE VENABLE CONVERTER

Although the Venable Converter is invariably used in its "original" form in which the inductor and transformer tap ratios n_x and n_y are equal, the model has been obtained for the "generalized" form in which n_x and n_y may be different. This permits results to be obtained for various special cases, and in particular illuminates the advantages of the original Venable Converter with $n_x = n_y$.

The derivation of the model of the generalized Venable Converter is too long to be given here, so instead the results will be presented and attention given to their interpretation and significance. The model is shown in Fig. A.1, and includes not only the Venable Converter of Fig. 1 itself, but also the modulator whose function is to convert the (analog) control voltage $V_c + v_c$ from some error amplifier into a corresponding duty ratio $D + d$. The notation is that

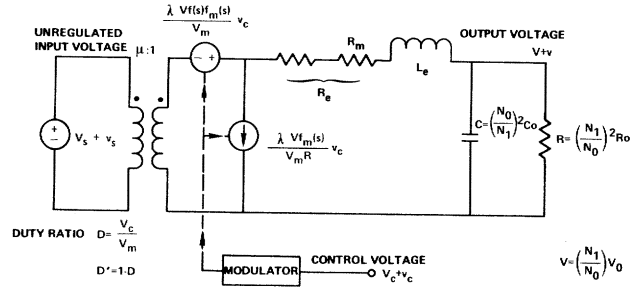

Figure A1 Low-frequency, small-signal model of a pulse-width-modulated switching converter in the continuous conduction mode.

lower-case letters represent small-signal ac variations superimposed upon the large-signal dc value represented by upper-case letters. The essential function of the modulator can be represented simply by

$$D = V_c/V_m \qquad (A.1)$$

where D is the fractional on-time of the inner switch and in which, by definition, V_m is the range of control voltage required to sweep the duty ratio D over its full range from 0 to 1. (If the actual relation is not linear, it can be linearized in the same form and then V_m becomes a function of operating point.) A small variation v_c superimposed upon V_c therefore produces a corresponding variation $d = v_c/V_m$ in D, which can be generalized to account for a nonuniform frequency response as

$$D = \frac{f_m(s)}{V_m} v_c \qquad (A.2)$$

in which $f_m(0) = 1$. Thus, the control-voltage-to-duty-ratio transfer characteristic of the modulator can be represented in general by the two parameters V_m and $f_m(s)$, regardless of the detailed mechanism by which the modulation is achieved. In "half-cycle response" types of modulator, such as those employed in the practical systems described in this paper, the frequency response can be taken to be uniform, so $f_m(s) \simeq 1$, over the frequency range of interest (up to half the switching frequency).

The model of Fig. A.1 represents not only the generalized Venable Converter, but also, with appropriate expressions for the parameters, any dc-to-dc converter including the conventional buck, boost, and buck-boost types and their numerous extensions [6]; it is subject only to the constraint that the converter operates in the continuous conduction mode.

The transformer is to be taken to be "ideal" and has a ratio μ:1 for all frequencies down to dc; it represents the basic dc-to-dc voltage and current con-

version factor. The two generators express the influence of the ac control voltage v_c as an input signal to the modulator/converter. The capacitance C and load resistance R are the equivalent values of the actual C_o and R_o of Fig. 1 reflected to the transformer primary, and the voltage V is the similarly reflected value of the actual output voltage V_o.

The inductance L_e is an "effective" inductance related to the actual inductance L of Fig. 1, but a function also of the dc duty ratio D. The elements L_e and C together constitute an effective "averaging" filter that represents the properties of the actual L and C in recovering the average, or dc, value of the switched waveform and filtering the switching frequency and its harmonics. The resistance R_e is an "effective" resistance that accounts for various series ohmic resistances in the actual circuit (including components due to the esr of both the capacitance C and any input-filter capacitance), and also a "modulation" resistance R_M that arises from a modulation of the switching transistor storage time [5]; R_e is a complicated function of these component resistances and also of the duty ratio, but since it is merely a parasitic resistance whose principal observed effect is upon the

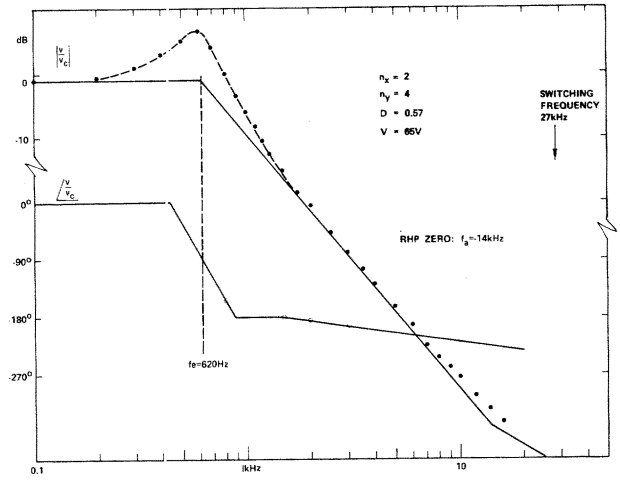

Fig. A.2 Predicted asymptotes and experimental data points for magnitude and phase of the control describing function v/v_c for a generalized Venable Converter with $n_x < n_y$.

Q-factor of the L_eC filter, detailed expressions for R_e will not be given. The modulation resistance R_M is often the dominant component of R_e, and is enclosed in an oval in Fig. A.1 to indicate that it is an element in the small-signal model only, and not in the large-signal dc model; it does not contribute to power loss and is in that sense "nonohmic," but explains the commonly observed higher degree of filter damping than would otherwise be expected.

The principal parameters in the general model of Fig. A.1, that are functions of duty ratio D and which distinguish one converter configuration from another, are μ, λ, f(s), and L_e. For the generalized Venable Converter, expressions for these parameters are:

$$\mu = (Dn_x/n_y + D')/(Dn_x + D') \tag{A.3}$$

$$\lambda = n_x(1 - 1/n_y)/(Dn_x + D')(Dn_x/n_y + D') \tag{A.4}$$

$$f(s) = 1 - \frac{(sL_e/R)(1 - n_x/n_y)(Dn_x + D')}{n_x(1 - 1/n_y)} \tag{A.5}$$

$$L_e = L/(Dn_x/n_y + D')^2 \tag{A.6}$$

where

$$D' \equiv 1 - D \tag{A.7}$$

is the "complementary" duty ratio.

With these results, the model of Fig. A.1 can be used to determine the several transfer functions of interest.

The large-signal dc result for the output voltage V as a function of the input voltage V_s and control voltage V_c (with neglect of the ohmic component of R_e), is simply

$$V = \frac{V_s}{\mu} = V_s \frac{1 + (n_x - 1)D}{1 + (n_x/n_y - 1)D} = V_s \frac{1 + (n_x - 1)V_c/V_m}{1 + (n_x/n_y - 1)V_c/V_m} \tag{A.8}$$

The transfer function from v_s to v, the line describing function, is obtained as v/v_s with $v_c = 0$, so that both generators are zero. The result is $1/\mu$ times the two-pole transfer function of the effective averaging filter. However, in general both the corner frequency and the Q-factor of the averaging filter are functions of dc operating point because the effective inductance L_e is a function of D, by (A.6).

The transfer function from v_c to v, the control describing function, is obtained as v/v_c with v_s = 0. The result is the product of the voltage generator and the two-pole transfer function of the averaging filter (in the absence of a line source impedance, the current generator is immaterial). The control describing function therefore contains not only the operating-point-dependent two-pole transfer function of the averaging filter, but also the frequency dependent f(s). By (A.6), this frequency dependence is expressed by the presence of a real zero in the complex plane. Although (A.6) is not exact (effects due to the parasitic resistance R_e are neglected) it shows not only that the value of the zero changes with operating point, but also the salient feature that the zero is in the left half-plane if $n_x > n_y$ and in the right half-plane if $n_x < n_y$. The presence of a right half-plane zero in the control describing function of course exacerbates the problem of stability in a closed-loop regulator system.

Experimental results for the control describing function v/v_c were obtained for a generalized Venable Converter circuit operated at a switching frequency of 27 kHz, and having the values L = 3.5 mH, C - 10 μF, and R - 300 Ω. A half-cycle response type of magamp modulator was used for which $f_m(s) = 1$ throughout the

frequency range of interest. Magnitude and phase measurements were obtained by techniques described in [7] and [8].

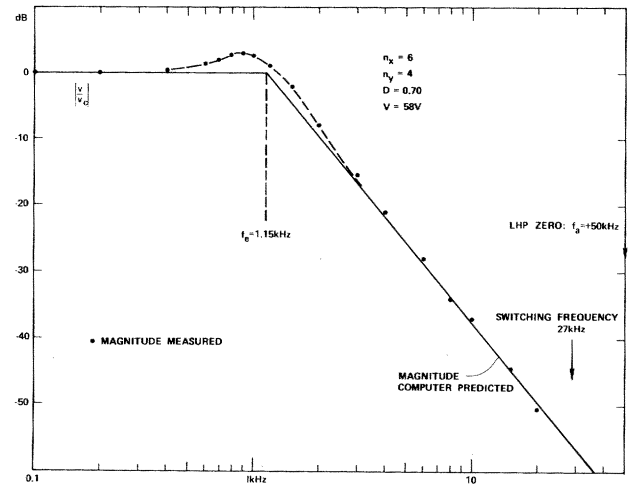

Fig. A.3 Predicted asymptotes and experimental data points for magnitude of the control describing function v/v_c for a generalized Venable Converter with $n_x > n_y$.

First, tap ratios $n_x = 2$ and $n_y = 4$ were selected, and a duty ratio $D = 0.57$ was established. Hence, $Dn_x/n_y + D' = 0.73$, and from (A.6) $L = 3.5/0.73^2 = 6.6$ mH. The corner frequency f_e of the averaging filter is then given by $f_e = 1/2\pi L_e C = 620$ Hz. From (A.5), the zero f_a in the function $f(s)$ is given by

$$f_a = -\frac{R}{2\pi L_e}\frac{n_x(1 - 1/n_y)}{(1 - n_x/n_y)(Dn_x + D')} \qquad (A.9)$$

and insertion of the above numbers leads to $f_a = -14$ kHz. Predicted magnitude and phase asymptotes for the corresponding control describing function are shown in Fig. A.2, and it is seen that the experimentally determined data points agree very well with the predictions. It is to be particularly noted that the phase lag exceeds 180° because of the right half-plane zero f_a.

A second set of tap ratios $n_x = 6$, $n_y = 4$ was selected, and a duty ratio $D = 0.70$ was established. Hence, $Dn_x/n_y + D' = 1.35$, and from (A.6) $L_e = 1.9$ mH leading to an effective filter corner frequency $f_e = 1.15$ kHz. From (A.8), the zero is $f_a = +50$ kHz so that, as expected, the zero is in the left half-plane because $n_x > n_y$. Predicted magnitude and phase asymptotes for the corresponding control describing function are shown in Fig. A.3. Although the zero f_a at 50 kHz is above the switching frequency of 27 kHz, and hence cannot be verified experimentally, it is seen that the experimental data points show no trace of a zero within the range of measurement, and also that the filter corner frequency at 1.15 kHz is well substantiated.

The model of Fig. A.1 also represents certain reduced forms of the generalized Venable Converter if certain values are chosen for the inductor and transformer tap ratios. In particular, if $n_y = \infty$, equations (A.3) through (A.6) reduce to those for the tapped-inductor boost converter [5]; if, in addition, $n_x = 1$, (A.3) through (A.6) further reduce to those for the conventional simple boost converter. In both of these reduced cases, the effective inductance L_e remains a function of D, and the zero in $f(s)$ is in the right half-plane and also has a value dependent upon D.

The special case of the original Venable Converter with $n_x = n_y$ has significant advantages over the generalized form. With $n_x = n_y$, $Dn_x/n_y + D' = 1$ for all D, and (A.3) through (A.6) reduce to

$$\mu = 1/(Dn_x + D') = 1/[(n_x - 1)D + 1] \qquad (A.10)$$

$$\lambda = (n_x - 1)/(Dn_x + D') \qquad (A.11)$$

$$f(s) = 1 \qquad (A.12)$$

$$L_e = L \qquad (A.13)$$

It is seen that L_e is now constant, independent of D, and so the averaging filter corner frequency and Q-factor are constant and do not depend upon operating point. Further, and even more important, the zero in $f(s)$ vanishes (to infinity) so that $f(s) = 1$ at all frequencies. Consequently, the frequency responses of both the line and the control describing functions do not change with operating point, which is a considerable advantage in the design of the loop gain of a regulator containing such a converter (although the scale factor of both describing functions still changes with operating point, since both μ and λ remain functions of D). These advantages are in addition to, and in fact are related to, the advantage that when $n_x = n_y$ the current delivered to the capacitance C is continuous from one switch interval to the next, which gives substantially lower output ripple. All these advantages combine to make the original Venable Converter with $n_x = n_y$ the invariable choice for practical applications.

In the absence of a line source impedance, the current generator in the model of Fig. A.1 is immaterial, but its presence is clearly necessary properly to predict the negative input impedance presented to the line by a closed-loop regulator employing such a switching converter, as can be seen by the following argument. When the regulator is driven by an ac component of line voltage v_s, the high loop gain at low frequencies will force the ac voltage v at the output to be vanishingly small by appropriate modulation of the duty ratio; since v is the output of the L_eC filter, the voltage at the filter input, namely, the voltage across the current generator, is therefore also vanishingly small; hence the impedance Z_i seen by the driving source v_s is simply the ratio of the voltage and current generators reflected through the transformer, or

$$Z_i = -\mu^2 \frac{\lambda V f(s)\, f_m(s)\, v_c/V_m}{\lambda V f_m(s)\, v_c/V_m R} = \mu^2 R f(s) \qquad (A.14)$$

At frequencies low enough that $f(s) = 1$ (or at all frequencies for the original Venable Converter), the result is $Z_i = R_i = \mu^2 R$, simply the negative of the reflected load resistance.

The result of (A.14) is valid only for frequencies at which the regulator loop gain is high; ultimately, beyond loop-gain crossover, the input impedance must revert to having a positive real part. In the presence of a line input filter, as is usual in practical systems, the complex input impedance can result in severe disturbance of the regulator properties and, in extreme cases, instability. This subject is treated in detail elsewhere [9].

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Dr. Middlebrook is a member of Sigma Xi and is Chairman of the Board of Electric Motion Control Corp. International.

STATIC INVERTER WITH SYNCHRONOUS OUTPUT WAVEFORM SYNTHESIZED BY TIME-OPTIMAL-RESPONSE FEEDBACK

Andress Kernick, Senior Member, IEEE, David L. Stechschulte and Donald W. Shireman

ABSTRACT

Time-optimal-response "bang-bang" or "bang-hang" technique, using four feedback control loops, synthesizes static-inverter sinusoidal output waveform by self-oscillatory but yet synchronous pulse-frequency-modulation (SPFM).

A single modular power stage per phase of AC output entails the minimum of circuit complexity while providing by feedback synthesis individual phase voltage regulation, phase position control and inherent compensation simultaneously for line and load disturbances.

Clipped sinewave performance is described under off-limit load or input voltage conditions. Also, approaches to high power levels, 3-phase arraying and parallel modular connection are given.

This paper was presented at the 1976 Power Electronics Specialists Conference, June 9, 1976.

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INTRODUCTION

The powerful method of feedback control in waveform generation, that is modus operandi with high-fidelity power amplifiers, differentiates the "bang-bang" [1] time-optimal-response [2 - 6] static inverter from the waveform feed-forward techniques normally used by virtually all other switching-type power conversion equipments. Makers of fast semiconductor power switches have put the onus upon the designers of static inverter circuits to achieve waveform quality and transient response at high efficiency that approaches what