Alignment-Insensitive Coupling for PLC-Based Surface Mount Photonics

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***Abstract*—A flip-chip waveguide coupler with an order of magnitude greater alignment tolerance than competing approaches is presented for the first time. Experimental data for an "optical jumper" agree with simple design considerations. Application to a planar lightwave circuit-based surface mount photonics platform is outlined.**

***Index Terms*—Integrated optics, integrated optoelectronics, optical planar waveguide components, optical planar waveguide couplers.**

I. Introduction

ONE OF THE most challenging aspects of optoelectronic packaging is efficient and robust power transfer from active devices to single-mode fibers. Motivated by the success of hybrid microelectronic packaging, including flip-chip surface mounting and printed wiring board (PWB) techniques, we embrace a similar vision for optoelectronics in which planar lightwave circuits (PLCs) function as PWBs [1]–[3]. In contrast to the active alignments commonly required in high-end devices today, the viability of this approach hinges upon its potential for low-cost passively aligned power transfer to the PLC platform, while maintaining high single-mode coupling efficiency [4]. To address this need, a new scheme for optical coupling between initially separate waveguides is introduced in this letter that is capable of lossless power transfer. Its most remarkable characteristic is a "flat-top" alignment insensitivity that is expected to be a key enabler of the surface mount photonics (SMP) paradigm. A program for the utilization of this technique with active device structures for SMP-enabled optoelectronics packaging is included.

II. End-Fire Coupling (EFC), Mode Interference Coupling (MIC), and Adiabatic Coupling (ADC)

It is instructive to compare the offset sensitivity of three techniques for optical power transfer between symmetric waveguides in a medium of index n at a wavelength λ. A Gaussian approximation to the waveguide modes (waist w_0 and Rayleigh range $z_0 = \pi n w_0^2/\lambda$) is used where applicable for simplicity. In EFC, the coupling sensitivity to an offset error $\mathbf{x}_e = (x_e, y_e, z_e)$ is given by the well-known expression

$$T_{\mathrm{EFC}}(\mathbf{x}_e) = \frac{\exp\left\{\frac{-(x_e^2+y_e^2)}{(w_0^2(1+Z_e^2))}\right\}}{(1+Z_e^2)} \tag{1}$$

with $Z_e \equiv z_e/(2z_0)$. EFC becomes extremely sensitive to $\mathbf{x}_e$ for the small values of $w_0 \sim \lambda$ typical of semiconductor-based devices that have been optimized for performance. MIC occurs between parallel uniform guides close enough together to be coupled via their modal exponential tails, which are assumed to have a decay length $1/\gamma$ in the vertical (y) direction. This evanescent coupling rate takes the form

$$\kappa(\mathbf{x}_e) = \kappa(0)\exp\left\{\frac{-x_e^2}{(2w_0^2)}\right\}\exp(-\gamma y_e) \equiv \kappa_e. \tag{2}$$

Complete power transfer requires a specific "flopping length" of $L_{\mathrm{MIC}} = \pi/(2\kappa(0))$ along the optical (z) axis, and obeys [5]

$$T_{\mathrm{MIC}}(\mathbf{x}_e) = \sin^2\{\kappa_e(L_{\mathrm{MIC}} + z_e)\} \tag{3}$$

rendering MIC also very sensitive to positioning errors in all three directions. To transfer power, ADC utilizes variation of some waveguide property along the optical axis, such as core index, thickness, or width. Under the unrestrictive assumptions that κ_e retains the form of (2) and the propagation constants of the individual modes vary linearly at a rate δ along the coupler, it is found that

$$T_{\mathrm{ADC}}(\mathbf{x}_e) = 1 - \exp\left(-\frac{\pi\kappa_e^2}{\delta}\right) \tag{4}$$

for long enough coupler lengths L_{ADC} [6]. In the limit of sufficiently strong coupling and slow z-variations, ADC thus, displays the following remarkable properties: 1) T_{ADC} permits ~100% power transfer between guides with no critical dimensions in the design; and 2) T_{ADC} is independent of placement errors $\mathbf{x}_e$, demonstrating characteristic "flat-top" offset tolerances laterally and complete longitudinal independence for $z_e \ll L_{\mathrm{ADC}}$. Adiabaticity also implies fault tolerance to most operational and fabrication errors, making ADC a robust high-performance broad-band solution to the coupling problem and ideally suited to PLC implementation.

III. Design and Experiment

To validate these predictions, we designed and fabricated [7] the "optical jumper" depicted in Fig. 1(a). The layer structure and refractive indexes $(n_{\mathrm{core}}, n_{\mathrm{clad}})$ of Fig. 1(b) were chosen

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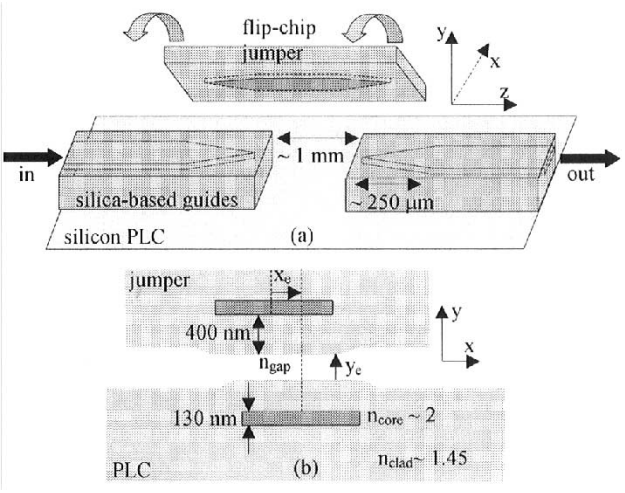

Fig. 1. Flip-chip ADC "jumper" experimental configuration. (a) A three-dimensional view showing guide widths tapering from 2.5 to 0.5 μm along the jumper, input, and output PLC guides. The guides were overlapped to have the same width at approximately the taper mid-points. A uniform, 1-mm-long guide in the jumper, and corresponding gap in the PLC guides, separated input and output. (b) A cross section mid-taper after flip-chipping illustrating offsets (x_e, y_e) as well as layer thicknesses and refractive indexes.

to give modes representative of modern active devices. The flip-chip configuration leverages the tightly controlled vertical tolerances maintained by deposition and etching processes common in the semiconductor industry. For experimental ease, the jumper was designed for transverse-electric polarization at 1300 nm. An ADC length of $L_{\mathrm{ADC}} \sim 15 L_{\mathrm{MIC}} \sim 250$ μm [Fig. 1(a)] is safely within the adiabatic regime. Simple linear tapering of the waveguide core width was used for maximal tolerance to lithographic errors. The wafers were processed using standard silica-on-silicon PLC fabrication techniques [1]. After dicing, the jumper die was held with constant force straddling the input and output PLC guides, which were on a separate substrate, by a flip-chip bonder with a repeatability of ± 0.25 μm. The substrate was mounted on a stage which had a resolution of $\sim$0.1 μm in order to measure transmission through the structure of Fig. 1(a) as a function of relative jumper-substrate position.

IV. Results and Discussion

Fig. 2 demonstrates the lateral placement tolerance of $T_{\mathrm{ADC}}(x_e)$ along with calculations using (4) and the beam propagation method (BPM). With Δx_e defined as the offset for which T_{ADC} remains within 0.1 dB of its peak, the measured lateral flat-top of $\Delta x_e \sim \pm 1.5$ μm closely matches predictions. In contrast, EFC and MIC tolerances are $\sim$5 to 10 times tighter and do not display this flat-top feature. The excess insertion loss of two ADC interfaces was $\sim$0.15 dB relative to cofabricated calibration structures over a measurement-limited bandwidth of $\geq$ 100 nm. The origin of this loss was traced to the blunt lithographic points of the tapers $\sim$0.5 μm through rigorous BPM studies. The calculated sensitivity for vertical errors y_e is shown in Fig. 3, assuming the gap is filled with material of index $n_{\mathrm{gap}} = n_{\mathrm{clad}}$. Again, the jumper displays an offset insensitivity to the transmission with a vertical flat-top of $\Delta y_e \sim$ 300 nm. The extent to which errors (x_e, y_e) along

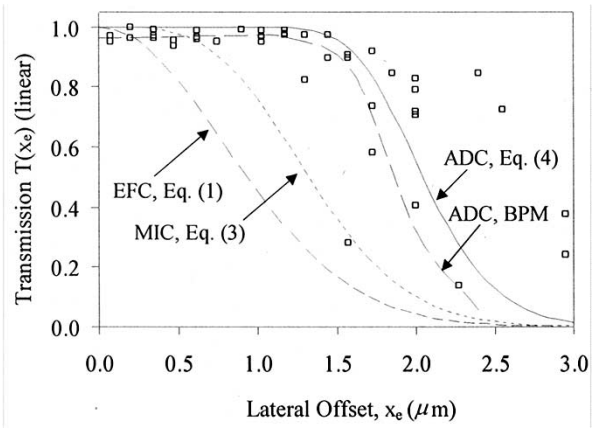

Fig. 2. Jumper "flat-top" measurements demonstrating $\Delta x_e \sim \pm 1.5$ μm, along with calculations for the ADC device of Fig. 1. Predictions for EFC and MIC in an appropriately comparable configuration are also shown.

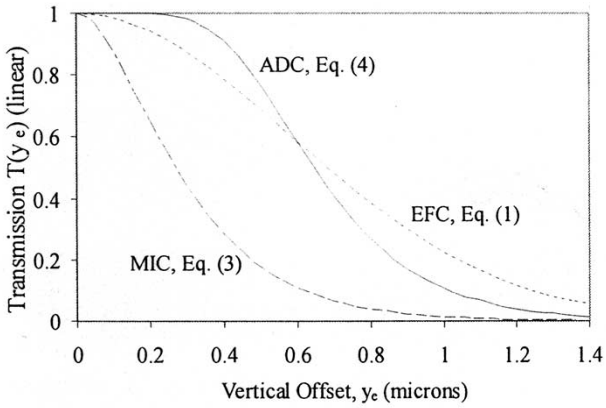

Fig. 3. Calculated curves for the vertical placement errors assuming the gap is filled with an index $n_{\mathrm{gap}} = n_{\mathrm{clad}}$. In our case, the flip-chip configuration along with standard semiconductor processing tolerances ensures negligible error in this dimension.

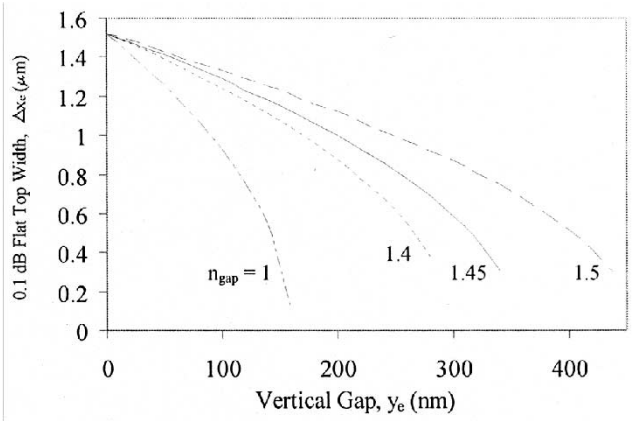

Fig. 4. Expected vertical sensitivity of the 0.1-dB fat-top width Δx_e to a vertical gap of index n_{gap}. Unwanted coupling between axes of this form is extremely limited in our design.

the two transverse axes are coupled depends upon the gap refractive index. Fig. 4 illustrates that the sensitivity of Δx_e to vertical errors y_e is reduced for increasing gap index n_{gap}. In the worst case, for example, an air gap of at least 125 nm is required to reduce Δx_e by a factor of two. Scanning electron

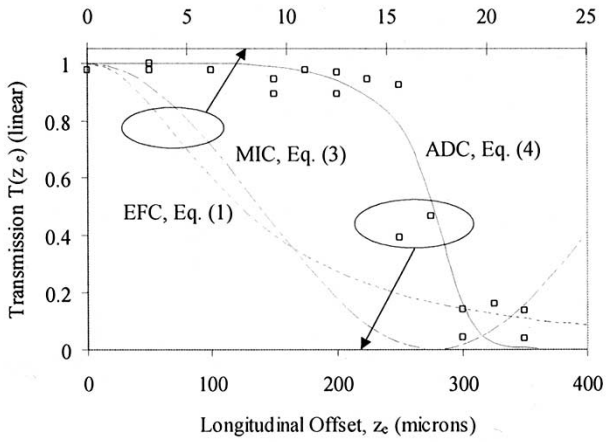

Fig. 5. Measured ADC z_e tolerance is ∼50 times greater than either EFC or MIC predictions. The device only fails when z_e reaches the adiabatic length $L_{\mathrm{ADC}} \sim 250\ \mu$m. Note the scale change along the horizontal axis for the EFC and MIC curves.

microscopy studies, on the other hand, verified our jumper design achieved intimate contact extremely reproducibly. In fact, a single jumper piece was used to produce all of the data in Fig. 1 without noticeable degradation in performance. Furthermore, overcladding thickness tolerances were $\sim \pm 40$ nm, negligibly impacting Δx_e according to the $n_{\mathrm{gap}} = 1.45$ curve. The measurements in Fig. 5 confirm the jumper is completely tolerant to errors z_e of order L_{ADC}, whereas, EFC and MIC are ∼50 times more sensitive along the optical axis.

V. Application to a PLC-Based SMP Platform

The application of ADC to optoelectronics packaging involves five key steps: 1) monolithic integration of glass-based waveguides with etched-facet semiconductor devices [8]; 2) passively aligned surface mount ADC of these devices to the silica-based PLC; 3) mode-expansion of the PLC guide to a fiber mode size [9]; 4) monolithic self-aligned V-grooves for passive fiber placement [10]; and 5) glob-top encapsulation of the complete packaged device to eliminate the need for hermetic packaging. Wafer-scale processing of steps 1, 3, and 4 leverages any necessary precision alignments over many parts at once. Of particular importance, step 1 can be accomplished using standard low-temperature dielectric deposition techniques consistent with III–V device processing. In fact, modern process flows already abundantly make use of these materials for alignment, masking, and passivation. Hence, the ADC coupler in SMP-enabled active devices can closely resemble the passive jumper reported here.

Exploration of the design and process window for the application of ADC to an SMP platform based on this prescription has been extremely encouraging and will be reported elsewhere. There is tremendous design flexibility for the ADC interface due to the forgiving nature of the adiabatic limit.

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