Silicon Nanocrystal Field-Effect Light-Emitting Devices

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(Invited Paper)

***Abstract*—We describe the operation of a light-emitting device in which silicon nanocrystals are electrically pumped via the field-effect electroluminescence (EL) mechanism. In contrast to the simultaneous bipolar carrier injection used in conventional p-n junction light-emitting diodes, this device employs sequential unipolar programming of both electrons and holes across a tunneling barrier from the same semiconductor channel. Light emission is strongly correlated with the injection of second carriers into nanocrystals that have been previously programmed with charges of the opposite sign. The properties of this device are well described by the model of a charge injection through Coulomb field modified tunneling processes. We additionally consider limiting performance bounds for potential future devices fabricated from nanocrystals with different radiative emission rates.**

***Index Terms*—Electroluminescence, light-emitting device, silicon nanocrystals, silicon quantum dots.**

I. Introduction

THERE is a widespread interest in silicon nanocrystals as an optoelectronic material system [1]. In comparison to bulk silicon, nanocrystals exhibit a tunable emission energy and increased oscillator strength due to the quantum confinement of excitons. Low nonradiative recombination rates observed for well-passivated silicon nanocrystals embedded in silicon dioxide lead to a very high internal photoluminescence (PL) quantum efficiency in spite of the relatively slow radiative recombination rates [2]. Our recent measurements demonstrate that this desirable property is maintained in dense nanocrystal ensembles, suggesting that devices might operate at high output conditions without significantly reduced efficiency [3]. However, the insulating matrix that defines a nanocrystal makes the efficient electrical carrier injection challenging. Consequently, the operating efficiencies of the previously reported electrically pumped silicon nanocrystal light-emitting devices have been relatively low [4]–[8]. The development of the efficient electrical pumping methods is a critical challenge for the improvement of the silicon nanocrystal based optoelectronic devices.

We have recently demonstrated the electrical pumping of silicon nanocrystals via a sequential programming technique termed *field-effect electroluminescence* (EL) [9]. Here, we report on the performance of a device that implements this EL mechanism. This device is an example of a general class of *field-effect light-emitting devices* (FELEDs) that rely on the charge-storage capability and optical emission properties of semiconductor nanocrystals. Under appropriate gate bias conditions, the nanocrystal array can be programmed with electrons from an inversion layer or with holes from the channel in accumulation. Excitons can be formed by sequentially programming the nanocrystals with charge carriers of each sign, resulting in EL at transitions in the gate bias. This approach is a departure from the previous carrier injection schemes in which nanocrystals are excited by a constant electrical current.

FELEDs may offer significant advantages over diode-based designs for nanocrystal light sources by enabling precise control over carrier injection processes. For example, durability can be maintained by exciting nanocrystals without resorting to impact ionization processes, in which excess hot carrier energy can result in oxide wearout and eventual device failure [10]. It should also be possible to carefully balance the injection of electrons and holes in order to minimize the wasted carrier transport. This offers the potential for power-efficient operation in an optimized FELED structure. The external power efficiency of our initial prototype devices has been limited by gate leakage currents, but this represents an engineering challenge rather than a fundamental limit for performance. Finally, lower voltage operation may be possible in comparison to the devices that rely on the current flow through a layer of the oxide-embedded nanocrystals.

II. Fabrication and Method

A schematic of our device is shown in Fig. 1. The structure resembles a nanocrystal floating gate MOS transistor memory with two important distinctions [11]. First, the floating gate array of silicon nanocrystals is formed from well-passivated silicon nanocrystals, which are small enough to have excitonic emission energies that are higher than the bulk silicon emission energy due to the carrier confinement. Second, the gate contact has been designed to be substantially transparent at the emission wavelength of the device (750 nm) but to still provide a uniform potential for control of the channel.

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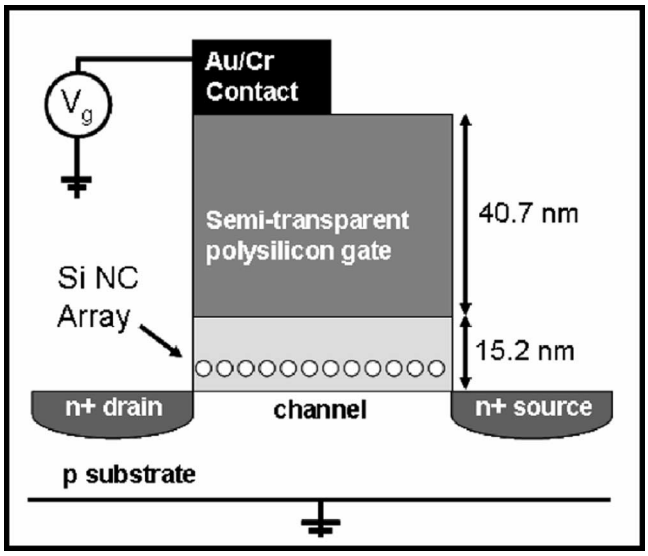


Fig. 1. Schematic of the silicon nanocrystal FELED showing the vertical dimensions of the gate stack determined using transmission electron microscopy.

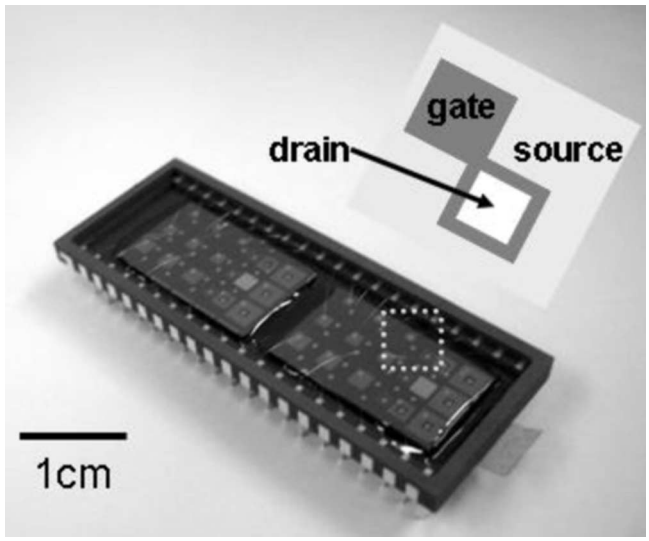


Fig. 2. Two silicon nanocrystal FELED die containing a total of 36 test structures packaged together in a 40-pin ceramic dual inline package. The ring gate transistor structure is shown in the *inset*.

The majority of the sample fabrication was performed at a 300-mm-wafer development facility at Intel Corporation. This required all processes used in the fabrication of our prototype devices to be selected first for CMOS compatibility. Therefore, an ion-implantation based approach was chosen to prepare the silicon nanocrystal layer despite several known nonidealities that such a fabrication method introduces. These undesirable consequences include the inhomogeneous distribution of the nanocrystal sizes and positions within the gate stack and possible degradation of the tunnel oxide layer. Ion-implantation damage can be substantially repaired by high-temperature annealing, however, both the duration and temperature of our nanocrystal-formation annealing step were limited by the constraints of the rapid thermal processing (RTP) tool used in the fabrication process.

An initially grown 15-nm dry thermal oxide was implanted with low energy (5 keV) $^{28}Si^{+}$ ions and annealed (5 min, 1050 °C) to precipitate an embedded array of silicon nanocrystals from the resulting supersaturated solid solution. A 40-nm thick polysilicon layer was then deposited to form a conducting gate contact layer. The absorbance of this layer is negligible at near-infrared wavelengths corresponding to the silicon nanocrystal emission but absorption does reduce the pump power arriving at the nanocrystal ensemble during PL experiments. Subsequent lithographic patterning and etching were used to form ring gate MOS transistor structures. The simplest possible transistor design was selected in order to expedite the fabrication; a more complex process (e.g., one that included sidewall isolation) might result in an increased performance. Blanket implantations of $^{15}P^{+}$ and $^{33}As^{+}$ were used to degenerately dope the gate contact, source, and drain. Device contacts consisting of a 10 nm Cr wetting layer and 100 nm of Au were then added using the thermal evaporation and lift-off process. Finally, devices were mounted in a Au wire-bonded package, as shown in Fig. 2.

Transmission electron microscopy in cross section was used to confirm the dimensions of the FELED structure. Individual nanocrystals cannot be resolved easily in such images due to a low Z-contrast between silicon and SiO_2. We have found that a combination of alternative techniques can more easily provide the desired structural characterization [12]. From ultrahigh vacuum scanning tunneling microscopy (STM) measurements on samples in which the oxide layer of the gate stack was removed with the buffered HF, we find the areal density of the nanocrystals forming the floating gate array to be at least $4 \times 10^{12}/cm^2$. By using ultrahigh vacuum noncontact atomic force microscopy (AFM) on the same sample further treated in an ultrasonic bath to lower the nanocrystal density [Fig. 3(a)], the diameters of most nanocrystals are observed to be $\sim$1.5–3.5 nm [Fig. 3(c)]. The maximum bound on the areal density can be derived from the total fluence of the implanted silicon ions and the average nanocrystal size, and is estimated to be within an order of magnitude of our lower bound. The discrepancy between these bounds may indicate a loss of nanocrystals during the partial etching procedure, implanted silicon that has not been precipitated into observable nanocrystals, and/or a significant loss of material to the bulk during the high-temperature nanocrystal-formation annealing [13]. The crystallinity of the nanocrystals was confirmed by the observation of the diffraction rings in the reflection high-energy electron diffraction (RHEED) measurements of the etched samples [Fig. 3(b)].

A 20-MHz arbitrary function generator with an output termination of 10 MΩ was used to electrically pump the packaged devices, while an Ar^{+} ion laser operating at 457.9 nm was used for the optical excitation. Spectra were collected by a grating spectrometer and a cryogenically cooled charge-coupled device (CCD) array. Stray light was removed by the optical filters and all the spectra were corrected for the detector sensitivity. Time-resolved EL traces were collected with a thermo-electrically cooled photomultiplier tube and a grating spectrometer. The

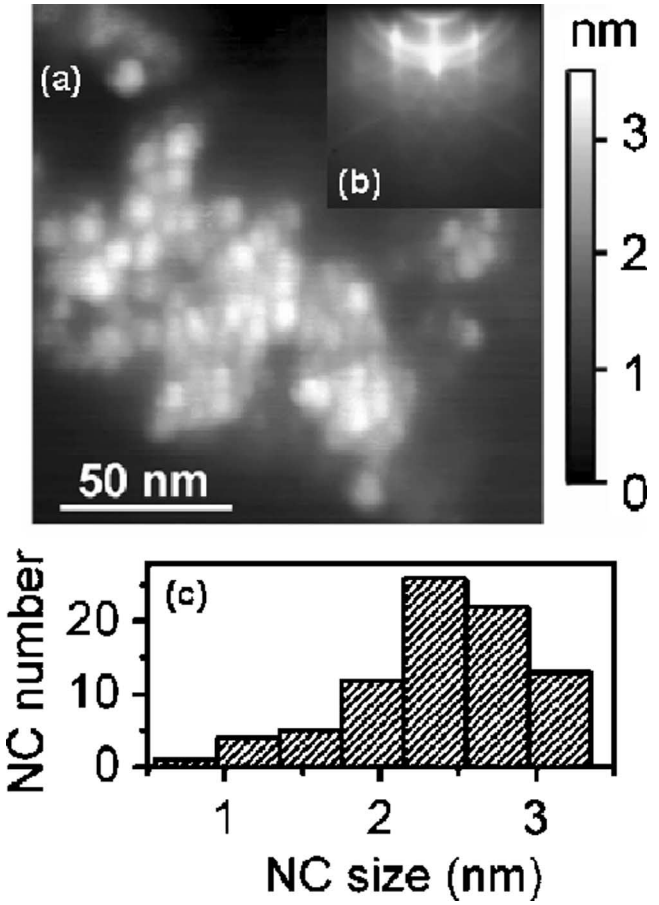


Fig. 3. Structural characterization of nanocrystals in the active region of the device. (a) Ultrahigh vacuum noncontact AFM topography of nanocrystals exposed by etching. (b) RHEED measurements establishing crystallinity. (c) Size distribution of nanocrystals.

time-resolved signal is the integrated emission over a passband of approximately 50 nm centered at the emission peak of 750 nm.

III. EL Properties

Fig. 4 shows a comparison of the nanocrystal PL excited through the semitransparent gate contact and nanocrystal EL excited through the field effect EL. We attribute these spectra to the radiative recombination of excitons within the silicon nanocrystals. Both the PL and the EL spectra peak near 750 nm with full-width at half-maximum (FWHM) of $\sim$160 nm. These emission spectra are typical for silicon nanocrystals fabricated through similar techniques. FWHM is attributed to the inhomogeneous broadening due to the size distribution of silicon nanocrystals in the array.

The electrical excitation process can be understood in more detail by considering the time-resolved EL trace in Fig. 5. Under the negative bias, the p-type channel is in strong accumulation. During this time, the nanocrystal array is charged with holes through tunneling processes. When the bias is abruptly changed to a positive voltage above threshold, an electron inversion layer is formed. Electrons are injected into the hole-charged nanocrystals via a Coulomb field-enhanced tunneling

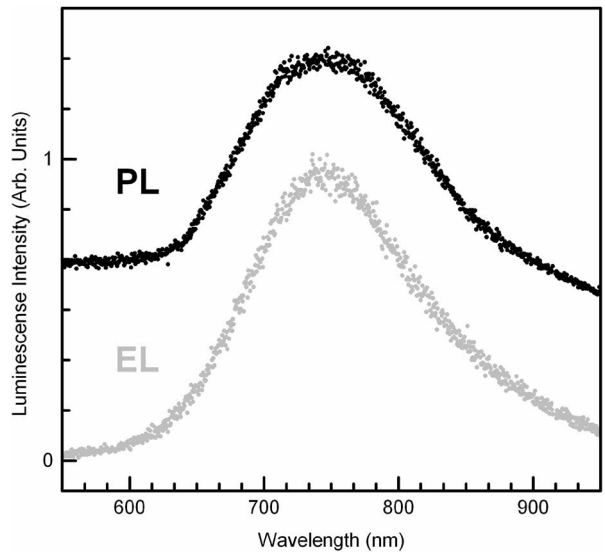


Fig. 4. Spectrum of the emitted light is similar for EL (EL; 6 V_{rms}, 10 kHz) and PL (PL; 457.9 nm, 1 mW/cm^2; data are shown uniformly offset by 0.5). In both the cases, the output is attributed to the recombination of the confined excitons within the silicon nanocrystals of the active layer.

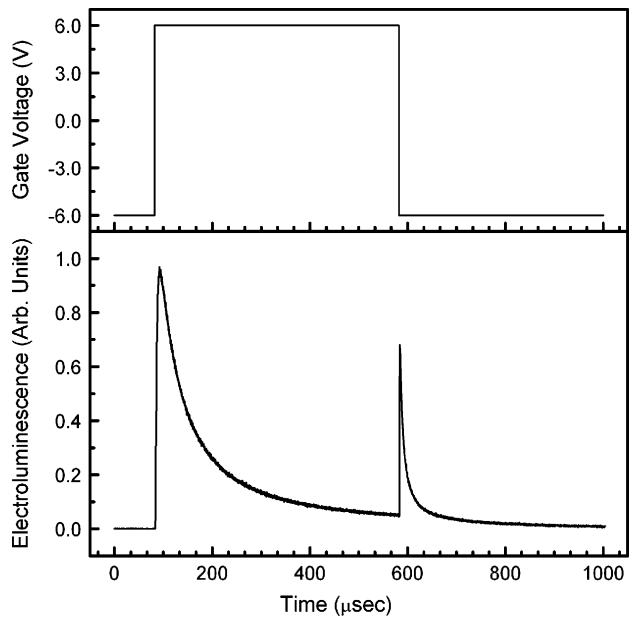


Fig. 5. Time-resolved EL trace demonstrates the correlation between light emission and gate bias transitions that correspond to the sequential programming events in a FELED.

process, forming quantum-confined excitons that recombine to emit light. The onset of the EL is well fitted by a single exponential rise ($\tau \sim 2.5\ \mu$s) at the applied 6-V gate bias.

Note that the observation of the EL necessarily implies that the holes already confined in the nanocrystals have an emission time for tunneling back to the channel that exceeds the Coulomb-enhanced tunneling time for electron injection from the inversion layer. The observation of the EL also implies that single carriers tunnel into each emitting nanocrystal during the charge-injection process because the presence of an additional electron or an extra hole in an excited silicon nanocrystal is

known to result in a rapid de-excitation through a nonradiative Auger process.

After the gate bias is switched from a negative to a positive level, the emission decays from a peak value as the previously injected holes are consumed by electrons in exciton formation and decay. A stretched exponential with a time constant of approximately 30 μs ($\beta \sim 0.5$) characterizes the observed decay [14]. This time constant is longer than the PL decay lifetimes observed for the samples under optical excitation at the same applied gate bias of 6 V ($\tau \sim 5$ μs, $\beta \sim 0.7$). The longer EL decay time constant may reflect an absence of the nonradiative recombination paths that are present for some fraction of the excitons recombining under illumination. Indirect charging processes involving inter-nanocrystal carrier migration are also likely to play a role in increasing the EL time constant by extending the time scales for exciton formation. Thus, some fraction of the exciton population may be formed by the migration of the electron and hole from another nanocrystal rather than by direct carrier injection from the channel. When the EL signal is no longer observed, there are no holes left in the nanocrystals to form excitons. Electrons continue to tunnel into the nanocrystal array due to the positive gate bias, resulting in each nanocrystal becoming recharged with an electron.

When the gate voltage is switched back to a strong negative potential, an accumulation layer forms in the channel and holes tunnel into the electron-charged nanocrystals and form excitons. This process is characterized by a faster single exponential rise in EL ($\tau \sim 240$ ns) and a faster stretched exponential decay ($\tau \sim 10$ μs, $\beta \sim 0.5$) compared to the previous case of electron injection. The peak associated with the hole injection into the electron-charged nanocrystals is smaller in magnitude and shorter in duration than the peak associated with the electron injection into the hole-charged nanocrystals. This asymmetry may be due to the back-tunneling of electrons to the channel during the hole injection. This loss of charge may be more apparent for the hole injection into the electron-charged nanocrystals due to the smaller conduction band offset ($\sim$3.2 eV) than the valence band offset ($\sim$4.7 eV) between the silicon and silicon oxide.

EL is clearly observed to be correlated with the injection of the second carriers, indicating that the field effect induced EL is due to the programmed exciton formation rather than due to the impact excitation resulting from a leakage current through the gate stack. As additionally shown in Fig. 6, emission occurs only for the bias transitions between the complementary gate voltage levels for which a sequential injection can occur. The lack of emission under dc electrical bias is further confirmed by an examination of the frequency dependence of EL in Fig. 7(a). As the measurement integration time is held constant at 2 s, a linear rise in EL is initially observed with an increase in the driving frequency because light is collected from an increasing number of integrated complete cycles. EL emission peaks at a frequency of 10 kHz, and then, begins to decrease, which we attribute to a combination of effects. As the driving frequency is increased, the number of excitons formed at the positive-to-negative (negative-to-positive) bias transition begins to decrease due to the incomplete initial electron (hole) charging. We believe that the $\sim$10 kHz peak in the frequency response corre-

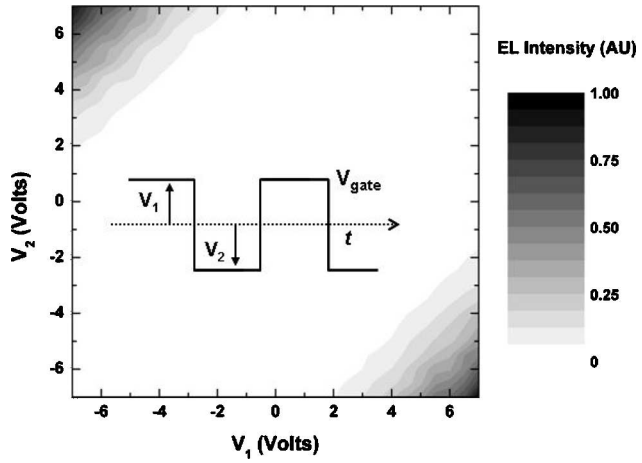


Fig. 6. EL is observed only at transitions in the gate bias (between levels V_1 and V_2) for which a sequential complementary charge injection is expected to occur. Values are for the peak EL recorded in a time-resolved measurement. The driving gate frequency was held constant at 10 kHz, while the amplitude and dc offset of the waveform was changed.

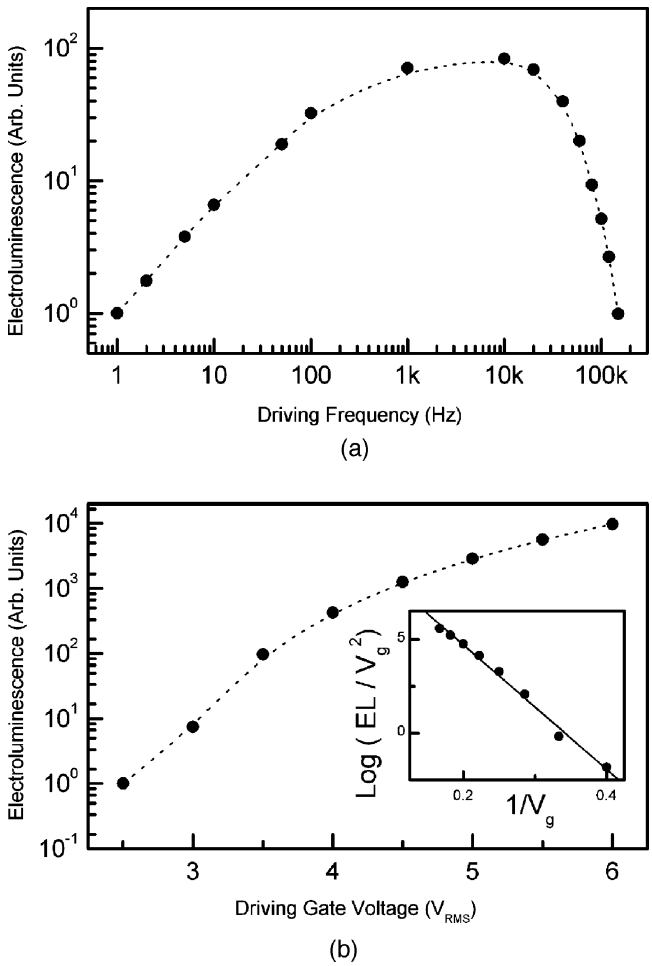


Fig. 7. EL response is a strong function of both (a) driving frequency (gate voltage = 6 V_{rms}) and (b) driving gate voltage (driving frequency = 10 kHz). An equivalent Fowler–Nordheim plot can be constructed (\) indicating that Fowler–Nordheim tunneling may be the tunneling mechanism.

sponds to a performance-limiting charge injection timescale for the first carriers into the neutral nanocrystals of $\sim 50\ \mu$s. This hypothesis is supported by the variable charging pulse length experiments discussed in Section IV (see Fig. 9). At frequencies above ~ 30 kHz, the pulse duration becomes shorter than the radiative lifetime of silicon nanocrystals and some of the excitons do not recombine because of the statistical nature of the spontaneous emission. Presumably, this population of excitons is lost to Auger processes when additional charge is injected at the next gate bias level. At even higher frequencies (~ 2 MHz), we expect charge injection to be further limited by the gate capacitive charging time constant.

The source and drain regions of the FELED are typically grounded during EL measurements. This allows minority carriers to flow laterally into an inversion layer from the source and drain regions and rapidly change the electron density in the channel. A capacitor-based light-emitting device with an identical gate stack would presumably be severely limited by the minority carrier generation and recombination times. Light emitted from our FELED under 10-kHz excitation appears spatially uniform over the entire gate stack area, including the 1-mm^2 contact pad area from which light is most conveniently collected using the free-space optics. In such large devices, it is possible that a portion of the high frequency roll-off in the EL signal is due to the finite electron drift velocity leading to the incomplete formation of the inversion layer.

As can be seen in Fig. 7(b), EL increases dramatically with increasing rms drive voltage. The field across the tunnel oxide is approximately proportional to the gate voltage and the magnitude of the EL signal is proportional to the tunneling current. Thus, we can construct an equivalent Fowler–Nordheim plot Fig. 7(b), inset) that follows a linear trend. This suggests that electron or hole injection into the nanocrystals occurs primarily through Fowler–Nordheim tunneling. Electrostatic modeling (Section V) suggests that the tunneling bias between the channel and the nanocrystals is typically 1–3 V. In order for tunneling to be dominated by the Fowler–Nordheim mechanism at these low voltages, the tunnel oxide thickness must be less than ~ 4 nm. This range is consistent with the oxide thickness targeted in our fabrication process.

IV. Optical Measurement of Charge Injection Processes

Because the magnitude of the EL signal is proportional to the tunneling current into the nanocrystals, we can optically monitor the charging and discharging processes. In particular, charge injection from the substrate into the nanocrystal layer and charge retention after programming can be obtained by observing the EL traces when the gate-substrate electrodes are periodically cycled with a carefully designed waveform.

Fig. 8(a) shows a generic drawing of the waveforms used to electrically pump the device in order to obtain hole injection and electron retention times. Similar waveforms with inverted polarity were used to measure the electron injection and hole retention times [Fig. 8(b)]. The different voltage steps of the waveform are labeled for reference. The injection and retention experiments are separated by the shadowed region III in Fig. 8(a). A reset pulse is performed in region VII to initialize the charge state to the same value at the end of each cycle. The varying parameters are the programming time for electrons/holes ($t_{\rm pe}$ and $t_{\rm ph}$, region I), the dwell time for electrons/holes ($t_{\rm de}$ and $t_{\rm dh}$, region V), and the disturbance voltage at which the retention is measured ($V_{\rm d}$, region V). The values chosen for these parameters are summarized in Table I.

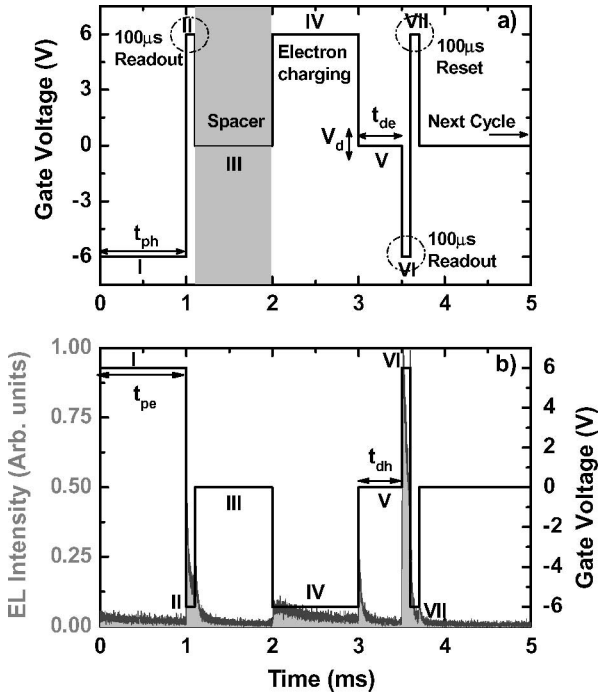


Fig. 8. Schematic of the waveforms used to measure the charging processes in the FELED device. The EL trace typically obtained by driving the device with the waveforms (*gray shading*).

TABLE I
Waveform Parameter Values Measured to Study Charge Injection and Retention

$t_{p(e/h)}$ (μs)	$t_{d(e/h)}$ (μs)	V_d (V)
10,20,50,100,200,500,1000	10,50,100,500,1000	-2,0,2

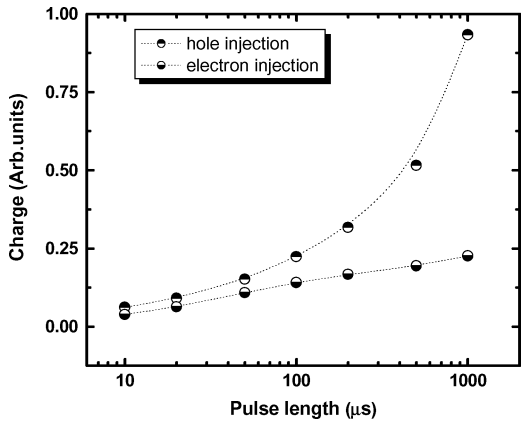


Fig. 9. Charge injection characteristics for electrons and holes inferred from the EL signal integrated over the readout pulse (region II in Fig. 8).

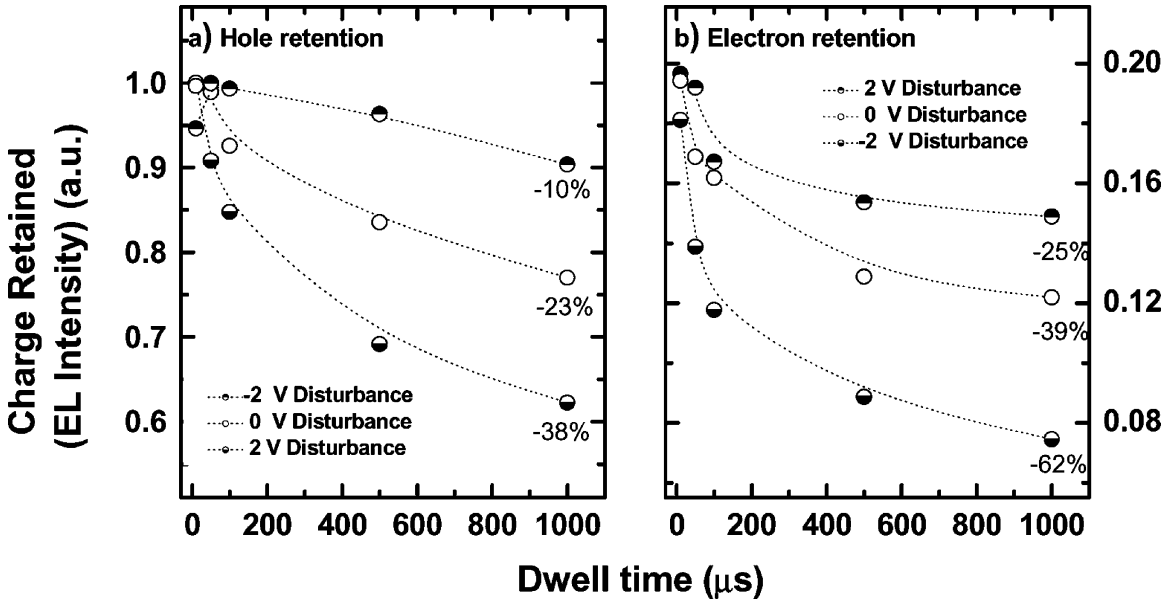


Fig. 10. Retention characteristics for different disturbance voltages as extracted from the integrated EL signal from region VI (see Fig. 8). (a) Hole retention. (b) Electron retention.

When these waveforms are used to cycle a device, a peak in EL is observed at those points where the voltage is abruptly changed [gray-shaded curve in Fig. 8(b)]. A relative change in the EL intensity reflects a relative change in the tunneling current from the substrate to silicon nanocrystals, enabling us to study the device charging and discharging dynamics by means of optical measurements. Note that the EL signal arises only from the tunneling current that drives the formation of excitons in silicon nanocrystals. Our measurements are, therefore, not sensitive to the leakage current through the gate stack that is responsible for the low external quantum efficiency of the device.

Other well-established methods are available for electrically characterizing the charge injection and retention in continuous and discrete trapping memories. However, these techniques measure changes in the conductance of the channel caused by the total charge present in the oxide. In contrast, our optical approach measures the light emitted by the silicon nanocrystals in response to the second carrier injection. Therefore, only the charging of silicon nanocrystals is considered, leaving apart the electrostatic screening effects of other kinds of oxide charging (e.g., trapping defects or ionic contamination). Such an oxide charging is relevant for evaluating the ultimate performance of memories but may obscure charging phenomena related specifically to silicon nanocrystals.

Charge injection characteristics for both the electrons and holes were determined from regions I and II. The silicon nanocrystal array was partially charged with electrons (holes) from the inversion (accumulation) layer when a gate voltage of 6 V (-6 V) was applied for $t_{\rm pe}$ ($t_{\rm ph}$) seconds. The relative amount of charge injected during programming was inferred from the integrated EL recorded during a subsequent -6 V (6 V), 100 μs readout pulse.

The times for electron and hole injection were found to differ as shown in Fig. 9. It may seem contradictory that holes appear more easily programmed than do electrons, considering the larger tunneling barrier SiO_2 presents for the valence band of silicon in comparison to the conduction band. This issue can be resolved by noting the influence of the complementary charge readout pulse. A limitation of this method is the destructive character of the charge measurement, due to the fact that the readout process always implies the injection of an oppositely signed carrier. Since the readout pulse cannot be instantaneous, the charge present in the silicon nanocrystal array may tunnel back to the substrate, resulting in an underestimate of the charge storage. An ideal measurement is reached only when either the measured carriers have an infinite retention or the readout carriers have an instantaneous injection time.

In our device, the measurement of the electron storage is more susceptible to this limitation as a consequence of both the slower injection of holes during the readout pulse and the faster discharging rate for electrons due to the differences in the energy barrier heights. In contrast, the ideal case can be approached for the measurement of the hole storage. The readout process is more reliable as the number of holes tunneling back to the substrate is small. As reported in the literature [15], this carrier asymmetry could potentially be overcome by scaling down the oxide thickness.

In order to quantify the retention times, we proceed similarly, using data from regions IV, V, and VI. First, a gate voltage of 6 V (-6 V) was applied for 1 ms, fully charging the silicon nanocrystal array with electrons (holes). Afterwards, a disturbance voltage $V_{\rm d}$ was applied for $t_{\rm de}$ ($t_{\rm dh}$) seconds. Finally, the remaining charge in the array was measured by integrating the EL intensity trace over a 6 V (-6 V), 100 μs readout pulse.

The disturbance voltage has an important impact on retention, as can be seen in Fig. 10. The electron (hole) release from the floating gate array to the substrate is facilitated by the negative (positive) disturbance voltage due to the gate bias enhanced

back-tunneling process. For $V_d = -2$ V (2 V), the electron (hole) number is decreased by 62% (38%) compared to 39% (23%) of the charge loss during the first 1 ms at $V_d = 0$ V. On the contrary, the retention is greatly increased for electrons (holes) when a positive (negative) disturbance voltage is applied across the structure. This time, the external field inhibits the back-tunneling of electrons (holes), and only 25% (10%) of the initial charge is lost within the first 1 ms.

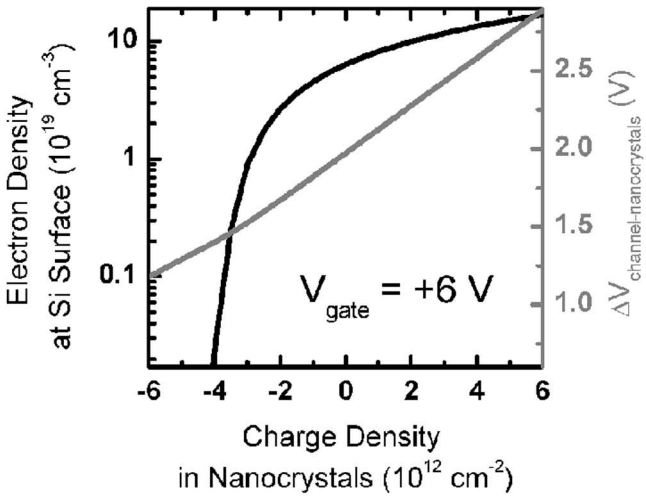
The dynamics of the charge retention typically show a substantial negative slope for retention at short dwell times and a more stable charge level for longer time scales. This may be a consequence of the distribution of nanocrystals within the gate stack, since the tunneling rate for the stored charge will decrease exponentially with distance from the silicon nanocrystals to the interface. The effective potential of the nanocrystal array also changes as charge is removed, which would be expected to improve the stability of a partially charged array. It is worth noting that the previous discussion of charge-storage underestimation in the case of electrons also holds here, and that the actual loss rates obtained for electrons are, therefore, expected to be smaller than those reflected in Fig. 10(b).

V. Simulation

Semiclassical self-consistent calculation was applied to provide a more quantitative explanation for the observed Coulomb field enhanced and inhibited tunneling. The gate stack of the device was modeled as a 15-nm-thick oxide layer. Different levels of stored charge in the nanocrystal layer were modeled as a uniformly distributed charge density in a plane 5 nm from the channel. The p-type channel doping level was 3×10^{18} cm^{-3} and the n-type doping level for the polysilicon gate was 10^{20} cm^{-3}.

Figs. 11 and 12 show the stored charge dependence of the channel carrier density at the silicon interface and the potential difference between the channel and the nanocrystal layer, at gate biases of $+6$ V and -6 V, respectively. The barrier potential for tunneling between the channel and the electrons is dramatically raised or lowered by the presence of previously injected charge carriers. From these data, it is possible to calculate the tunneling current between the channel and the floating gate of the silicon nanocrystals (Fig. 13) [16].

A comparison of the rise times for EL in Fig. 5 (0.25 or 2.5 μs) to the injection time for the first charges ($\sim$50 μs) suggests that tunneling is dramatically enhanced by the presence of the complementary charge in the nanocrystal array. This is confirmed by our modeling, which shows that the electron and hole currents vary strongly as a function of the total charge stored in the nanocrystal layer. For example, the electron injection is enhanced by a factor of $\sim$10 by the presence of holes with an areal density of 2.4×10^{12} cm^{-2} in the nanocrystals and hole injection is enhanced by a factor of $\sim$ 10 by the presence of electrons with an areal density of 1.6×10^{12} cm^{-2} in the nanocrystals (Fig. 13). On the other hand, like charges injected into the nanocrystal array partially shield the electric field due to the gate bias, resulting in a dramatic decrease of channel carrier densities as well as tunneling currents. The phenomenon of Coulomb field inhibited tunneling is especially evident for the injection



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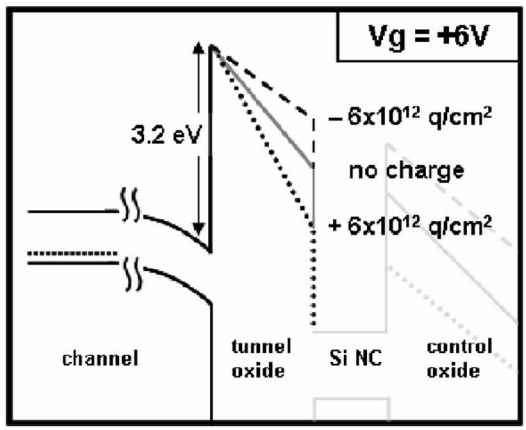


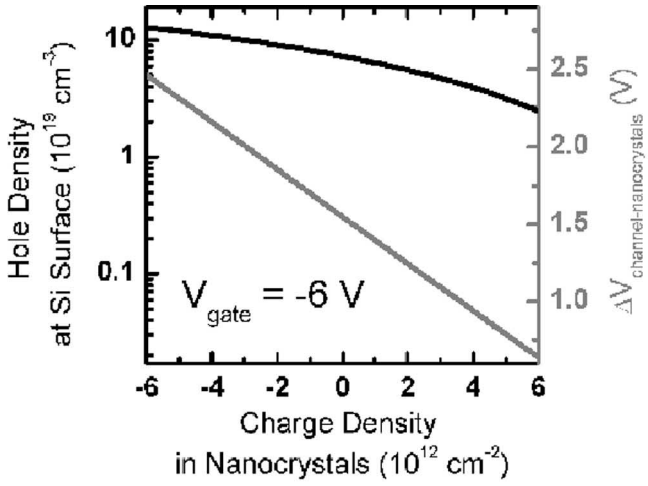
(b)

Fig. 11. (a) Semiclassical self-consistent electrostatic simulation of FELED in equilibrium at a gate bias of $+6$ V. (b) Effect of the stored charge on the potential barrier for electron tunneling.

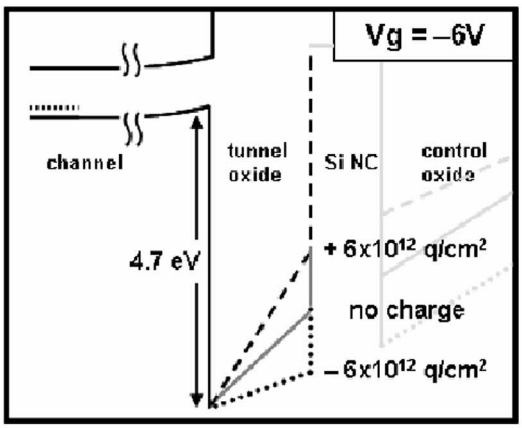
of electrons. At an applied $+6$ V gate potential, the strong inversion layer in the channel disappears when the areal density of electrons in nanocrystals exceeds $\sim 3.5 \times 10^{12}$ cm^{-2}. In this case, the electron tunneling current is dramatically reduced.

VI. Performance Limits

It is useful to estimate the maximum power output that might be achieved from a FELED. For an ideal device containing a close packed array of 2–4 nm diameter nanocrystals, an areal nanocrystal density of $\sim 10^{12} - 10^{13}$ cm^{-2} could possibly be achieved while maintaining a uniform tunnel oxide thickness. Assuming 100% internal quantum efficiency for the nanocrystals, this device could emit as many as two photons per nanocrystal per complete gate voltage cycle. Multilayer designs might conceivably increase this output capacity but will be excluded from consideration here. For conversion to the units of power, we will further assume that the photons are emitted at 1 eV regardless of the nanocrystal recombination rate. This is an acceptable approximation for the material systems that one might consider in practice.



(a)



(b)

Fig. 12. (a) Semiclassical self-consistent electrostatic simulation of the FELED in equilibrium at a gate bias of -6 V. (b) Demonstration of the effect of the stored charge on the potential barrier for hole tunneling.

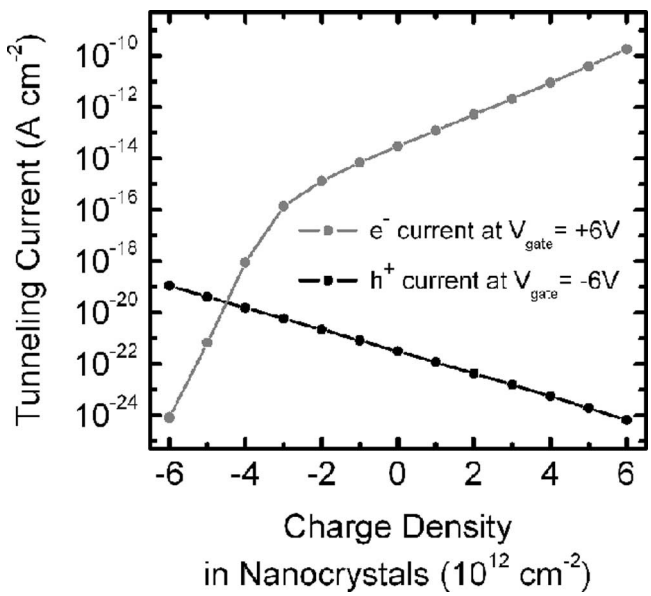


Fig. 13. Calculated tunneling currents from the channel into the nanocrystal layer demonstrate the Coulomb field enhancement and inhibition of the charge injection.

There may be some room for improvement in the gate contact layer used in our current device. The thin polysilicon design strikes a balance between conductivity ($\sim$180 Ω/square) and absorption (calculated $<$10% at 750 nm), but no specific efforts have been made to improve the out-coupling of light from the nanocrystals. For the purpose of argument, we will assume that an ideal device can approach 50% of the external quantum efficiency.

The average power output of a FELED will scale linearly with the driving gate frequency until one of a number of possible limiting factors becomes significant. The maximum useful driving frequency can potentially be limited by the *RC* time constant of the gate or possibly by the minority carrier drift velocity for large devices, the tunneling rate of carriers for devices with thick tunnel oxides, or the statistics of the spontaneous emission. The most important of these factors for an ideal device is the radiative recombination rate for the confined excitons. If the driving gate frequency is increased beyond about half the radiative recombination rate, the output of the device will rapidly saturate while the efficiency quickly decreases. The integrated probability of emitting a photon decreases linearly at such high frequencies, counteracting the linear improvement gained from cycling the FELED at faster rates. Thus, the optimal driving frequency for a FELED will be determined by the radiative rate of the emitting nanocrystals. We can conclude that an optimized silicon nanocrystal FELED will likely saturate at a driving frequency below 100 kHz. It may be possible to enhance the spontaneous emission rate by engineering the local dielectric environment of the nanocrystals or to extract the energy of the excitons by some faster nonradiative mechanism, but such strategies are beyond the scope of this analysis [17].

Presumably, the tunnel oxide thickness, which we believe to limit the maximum output of our silicon nanocrystal FELED, could be scaled down in a straightforward manner to allow operation at driving frequencies well into the gigahertz range. The capacitive time constant is likewise assumed to pose a surmountable design problem. Within this framework, we can calculate the approximate ideal case performance limits for FELEDs constructed from hypothetical nanocrystals with various recombination lifetimes (Fig. 14). The hypothetical performance limits are shown for several commonly studied nanocrystals despite the materials challenges that might arise in the realization of FELEDs that contain them. In consideration of the possible display applications, we have attempted to quantify the luminous intensity of the ideal FELED. The emission wavelength is essential for the conversion of the radiated power to the perceived brightness. Accepted peak values for the conversion factor are 683 lm/W at 555 nm for daylight vision and 1700 lm/W at 507 nm for night vision. We have assumed a value of 300 lm/W in our calculation to reflect an average over the visible range.

We can further speculate on the maximum efficiency attainable in an ideal silicon FELED, which would be reached at driving frequencies much lower than the nanocrystal recombination rate, corresponding to a lower output power regime. We have observed EL at an energy $E_{\rm opt} \sim 1.65$ eV, at driving gate voltages as low as 2.5 $V_{\rm rms}$, and will assume that this represents a realistic minimum operating voltage. On a per-nanocrystal

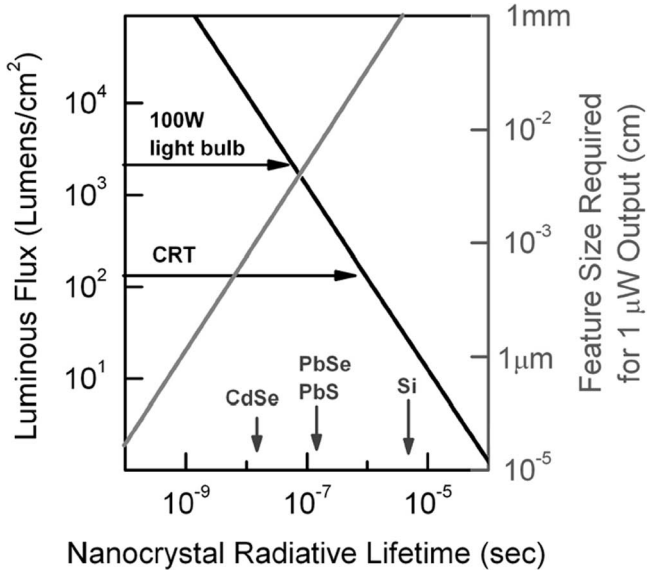


Fig. 14. Approximate ideal case limits for the maximum power output of a FELED parameterized by the nanocrystal radiative emission rate, which effectively determines the maximum cycling rate for each device.

basis, each cycle of the gate voltage will require $\sim$1.2 eV to charge and discharge the gate capacitance. Additional energy will be lost to scattering in the charge injection process, which may be approximated by the voltage drop across the tunnel oxide for the four tunneling events that occur. The potential drop for tunneling into a neutral nanocrystal at a gate bias of 2.5 V is $\sim$0.8 V, incurred twice per cycle. For electrons tunneling into hole-charged nanocrystals, the drop is $\sim$1.1 V, while holes tunneling into electron-charged nanocrystals drop $\sim$0.4 V. Neglecting other sources of loss (e.g., contact resistance), $E_{\rm el} \sim 2.2$ eV is required, on average, to program each exciton in an ideal FELED, in contrast to $\sim$1.1 eV required for the exciton formation in an ideal silicon LED. There are two advantages from a power efficiency standpoint for the silicon FELED. The first is that the internal quantum efficiency of a well-passivated silicon nanocrystal can approach 100%, and the second is the greater energy of the emitted photons. If the nonradiative recombination of the excitons is completely suppressed in the nanocrystals, the ideal silicon FELED might reach an internal power efficiency as high as $\eta_{\rm ipe} = E_{\rm opt} / E_{\rm el} \sim 75\%$.

VII. Conclusion

Field effect EL, as demonstrated in our silicon nanocrystal FELED, is an unanticipated and surprisingly successful approach to electrically exciting excitons in semiconductor nanocrystals. Such a device also provides a useful laboratory tool for the study of the charge injection processes. In a future experiment, one can imagine extending this control over charging, perhaps to deliberately induce Auger quenching of emission by the injection of additional charges.

While the efficiency of our FELED is low due to a significant leakage of currents, it should be possible to demonstrate high power efficiency light emission in future optimized silicon devices. We have additionally considered the power output characteristics of idealized devices to address the feasibility of practical application. In light of our analysis, it appears that an optimized silicon nanocrystal FELED might be a viable candidate for some display applications. While it remains to be experimentally demonstrated that FELEDs can be fabricated in other materials systems, the same performance analysis suggests that a device constructed with direct gap nanocrystals could be very promising.

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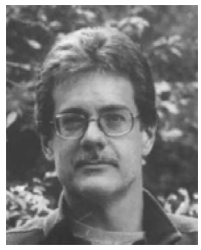

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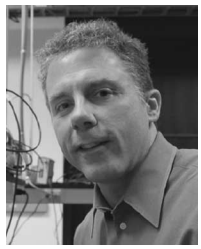

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