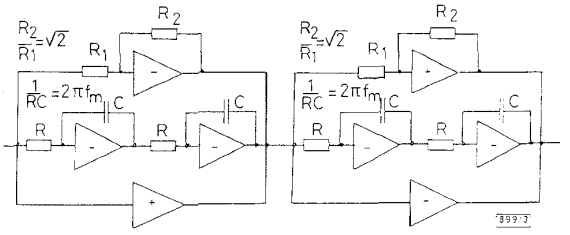

Fig. 3 *MF realisation*

phase or time delay used in common filter design. RCF filters are mandatory for reducing ISI in digital communication systems. The development of a novel active filter is presented in this Letter. The new filter, called the medium filter (MF), includes only two common operational amplifier stages as shown in Fig. 3. The MF provides significantly better ISI performances than two- or even four-order BF as demonstrated in this Letter and shown in Table 1.

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Single-clock-cycle two-dimensional median filter

V.A. Pedroni and A. Yariv

Indexing terms: Median filters, Filters, Image processing

Median filters are of interest to image processing due to their ability to remove impulsive noise. Conventional digital implementations of the median function, however, require multiple clock cycles, a number that is proportional to the size of the 2-D data block. We present in the Letter a complete CMOS implementation, which consumes very little power and computes the median in just one clock cycle, independently from the size of the data block.

Introduction: Median filters are of high interest in modern image processing applications due to their ability to remove impulsive noise without great edge disturbance [1, 2]. They constitute a particular case of rank filters in which the central element (the median) of the ordered set is to be selected. Performing the median function in a low time complexity fashion is a very challenging exercise from the viewpoint of hardware implementation. Digital realisations of this function cannot be performed in a single clock cycle, even for one-dimensional data streams, regardless of the circuit architecture adopted. This fact is illustrated in Fig. 1, which shows a typical digital implementation of a median filter [1]. As can be seen, it relies on threshold decompositions of the M-valued components of the data block (of size $N=n \times n$) into $M-1$ binary strings of length N, which are then binarily filtered and later added together. In this kind of system (as in any digital median filter), it takes several clock cycles for the median element of the data set to be identified. Moreover, the number of clock cycles inevitably grows with the size of the data block.

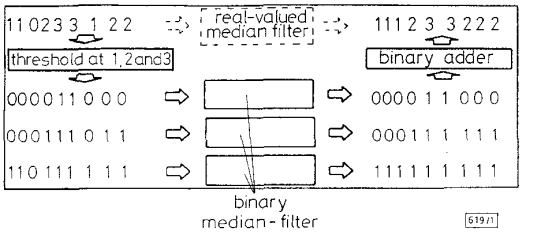

Fig. 1 *Conventional median filter implementation example*

Single-clock-cycle 2-D median filter circuit: We observe that, given a real-valued set $\mathbf{X} = \{x_1, x_2, ..., x_N\}$, the median of $\mathbf{X}$ can be computed as $\text{med}(\mathbf{X}) = \min_j\{\Sigma_{i=1}^{N}|x_j - x_i|\}$. This equation indicates that an array of absolute-distance cells, when properly interconnected, can implement the median function directly and in a single clock cycle. Such a system is illustrated in Fig. 2. As shown in the inset, each individual cell has two inputs and two outputs. One output is equal (or linearly proportional) to the highest input, whereas the

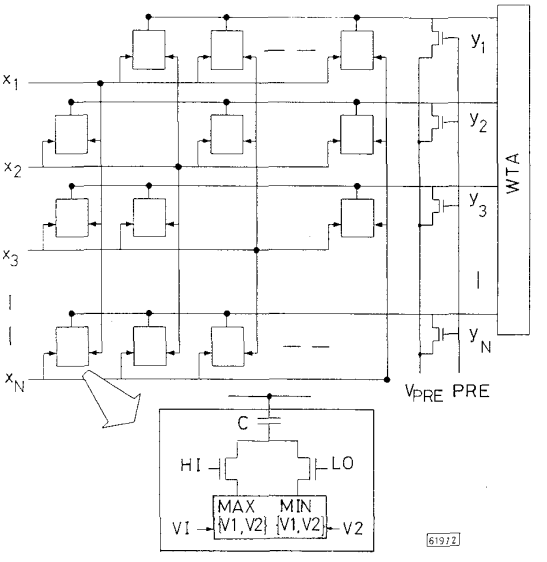

Fig. 2 *2-D median filter of O(1) time complexity*

other is to the smallest one. Then, by applying a (digital) control signal HI/LO (high/low), the outputs can be independently selected. While HI is active, the PRE (preset) signal is activated, precharging all rows with a reference voltage V_{PRE}. After PRE is released, HI is disabled and LO is enabled. This causes the voltage of each row to be lowered proportionally to $y_j = \Sigma_{i=1}^{N}|x_j - x_i|/N$, $j = 1, 2, ..., N$ (due to the action of the HI/LO switch transistors and the coupling capacitors C). Therefore, the row that presents the smallest summation will stay closest to its initial level, V_{PRE}. These row voltages are then applied directly to a winner-take-all (WTA) circuit (i.e. a circuit that detects the highest among its input voltages, e.g. [3, 4]) The input signal to the row identified by the WTA is the median of the data set. Therefore, it takes only one clock cycle for the median to be computed in this implementation.

Fig. 3 depicts three absolute-distance cells. In (*a*) [5], one side of the circuit is normally off, while the other is in subthreshold, being the central transistors needed in order to discharge the output nodes. In (*b*) [3], on the other hand, the transistors operate in saturation. In both cases, a voltage-follower configuration is used, resulting in $V_{O1} \propto \max\{V_1, V_2\}$ and $V_{O2} \propto \min\{V_1, V_2\}$, and similar performances. A more accurate cell is presented in (*c*), where a voltage comparator is employed to select the highest and lowest voltages directly; in this case, a higher transistor count also results.

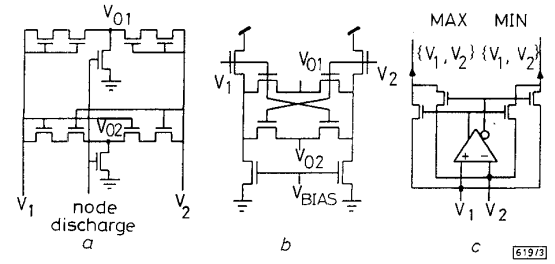

Fig. 3 *Absolute-distance cell implementations*

Experimenial results: A complete N=25 (5 × 5) system was fabricated using 1.2μm CMOS technology. The architecture adopted was that of Fig. 2, with distance cells of Fig. 3*b* [3] and the WTA circuit of [4]. The size of the chip was 1.6 × 1.1mm². The tests were realised with the 25 inputs separated into two blocks of 12 elements each, plus a single element. The voltages Vin_1 and Vin_2 were applied to each of the two blocks, while V_{med} was applied to the single input. The results are depicted in Fig. 4.

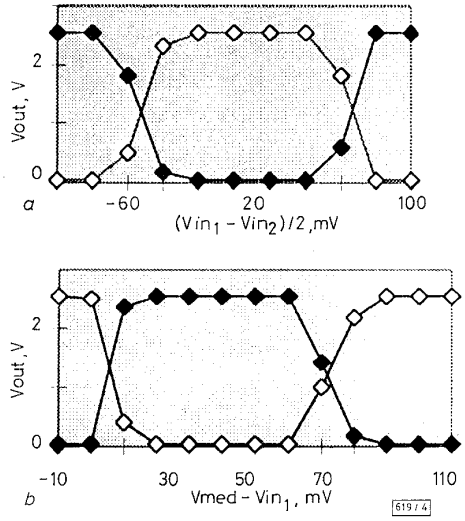

Fig. 4 *Experimental results*

◆ median output, ◇ other output
V_{PRE} = 3V, V_{BIAS} = 0.8V, V_{med} = 2V, Vin_1 = 3.0V, Vin_2 = 3.1V

In Fig. 4*a*, V_{med} was kept fixed at 3V, while $Vin_1 < V_{med}$ and $Vin_2 > V_{med}$ were approximated gradually to V_{med} (worst-case). As can be seen, the median was correctly identified when its value was ~80mV or more from the other elements. In Fig. 4*b*, on the other hand, Vin_1 and Vin_2 were kept fixed (at 3.0V and 3.1V, respectively, i.e., 100mV apart), while V_{med} was varied. As can be seen, the median was correctly identified when it was ~10mV above the lower block voltage or 40mV below the higher.

Conclusion: Computing the median function on 2-D pixel blocks with $O(1)$ time complexity is possible when the proper architecture is used. Such an architecture has been presented in this Letter, which makes use of absolute-distance cells and a WTA network. Experimental results, from an N=5 × 5 system, were also presented. Accuracy in the 6-bit range is easily obtained in this kind of system, allowing therefore the computation on blocks of size > 64 pixels.

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Fractal coding performance for first-order Gauss–Markov models

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Indexing terms: Fractals, Image coding

Fixed block size fractal coding is evaluated for first-order Gauss-Markov models and the effects of varying tile correlation are presented. Performance for this class of statistical models is found to be significantly suboptimal.

Introduction: In fractal coding [1] of signals (usually images), each signal is represented by the coefficients of a contractive affine transform on itself. The signal is tiled by nonoverlapping range blocks, and larger, possibly overlapping domain blocks. The global affine mapping consists of scaling and offset coefficients mapping one of the domain blocks (after averaging to the range block width) to each range block. These coefficients are identified by use of the Collage theorem [2], which bounds the real error on decoding in terms of the collage error. While coding performance evaluations utilising test images have been promising [2], the performance of this coding method has not previously been evaluated for a statistical signal source, leaving fractal coding at a disadvantage in comparison with traditional methods such as transform coding.

Signal model: A Gaussian first-order Markov (or $AR(1)$) process $X(n)$ is generated ([3], Chap. 2) by

$$X(n) = Z(n) + \rho X(n-1)$$

where ρ is the correlation and $Z(n)$ are independently distributed Gaussian values with variance σ_z^2. The autocorrelation function of this process is $R_{xx}(k) = \sigma_x^2 \rho^{|k|}$, with $\sigma_z^2 = (1 - \rho^2)\sigma_x^2$. Transform coding may be shown to be close to optimal for these models [3].

The performance of fixed block size fractal coding schemes for this model were investigated by calculating the distortion for each member of an ensemble of 1000 signals (restricted to 1-dimension to reduce computational requirements) randomly generated according to the model. Results are presented for signal size n, range block size r, domain block size $2r$ with the domain pool consisting of all domain blocks an increment of two samples apart, and contractivity bound s_{max} (for all scaling s, $|s| < s_{max}$). All distortions are mean square error (MSE), with $\sigma_z^2 = 1$ constant as ρ varies.

Real and collage errors: Fig. 1 illustrates the difference between the collage and real error for signals of 4096 samples. In these and all other cases the real error was significantly greater than the collage error, with a decrease in the difference with increasing ρ. Since the collage error may be calculated more rapidly than the real error, it is used as a lower bound for the real error in many subsequent comparisons.

Contractivity: Since $s_{max} < 1$ is sufficient, but not necessary, for contractivity [4], higher values are often employed. Fig. 2