

Nanoelectromechanical Systems for Ultra-Low-Power Computing and VLSI

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Nanoscale devices with mechanical degrees of freedom offer compelling characteristics that make them very attractive for mechanical and quantum logic devices. As we are able to create nanoelectromechanical systems (NEMS) with unprecedented feature sizes, advanced complexity and functionality, and high yield and control (at wafer-scale), they become increasingly interesting for low-power logic and memory, as well as become more meaningful for VLSI. Partly this is driven by NEMS devices' unique merits such as exceptionally large on/off ratio, non-leakage, ultralow switching power, fast speed, and temperature insensitivity. In parallel, this is also an intriguing effort in the quest for the ultimately energy-efficient implementation of logic and computing. In this talk, I shall introduce the Caltech research effort towards these goals, including the recent demonstrations of several generic prototypes of nanoscale electromechanical switching devices, their characteristics and performance, progress on engineering such building blocks for NEMS-based logic and memory, all-mechanical and hybrid NEMS-CMOS, along with discussions and perspectives of technological promises and challenges.