Characterization of a Large-Format, Fine-Pitch CdZnTe Pixel Detector for the HEFT Balloon-Borne Experiment

C. M. Hubert Chen, Walter R. Cook, Fiona A. Harrison, and Jiao Y. Y. Lin

***Abstract*—We have developed a large-format CdZnTe pixel detector with custom, low-noise ASIC readout, for astrophysical applications. In particular, this detector is targeted for use in the High-Energy Focusing Telescope (HEFT), a balloon-borne experiment with focusing optics for 20–70 keV. The detector is a 24×44 pixel array of 498-μm pitch. As a focal plane detector, uniformity from pixel to pixel is very desirable. In this paper, we present the characterization of some detector properties for the 1056 pixels on the HEFT detector. These properties include electronic noise, leakage current, spectral resolution, and count rate.**

***Index Terms*—CdZnTe radiation detectors, radiation detector circuits, X-ray astronomy detectors.**

I. Introduction

We are developing cadmium zinc telluride (CdZnTe) *pixel* detectors for use on the focal planes of *focusing* telescopes. Specifically, the detector design that we present here is targeted for use in the High Energy Focusing Telescope [1] (HEFT), which is a balloon-borne, hard-X-ray telescope, and for the future satellite mission, Constellation-X, in its hard X-ray telescope [2]. For HEFT, the detector needs to oversample a one-arcminute half-power diameter spot, and at the same time, cover a field of view of ten arcminutes or more. For a focal length of 6 m on HEFT, these dimensions translate to a spot size of 1.75 mm and a field of view of at least 17.5 mm. Our project emphasizes on getting good energy resolution from the detectors in the energy range 20–70 keV. In contrast, properties such as high count rate is not important in our application, as we shall only be looking at faint astronomical sources with HEFT.

Similar CdZnTe pixel detector studies has been done by others, both for hard X-ray astrophysics and for other applications. Sharma *et al.* [3], Gaskin *et al.* [4] and Baumgartner *et al.* [5] also studied CdZnTe pixel detectors for use in the focal planes of focusing hard X-ray telescopes, much like HEFT. The pixel pitch and the design of the electronics both differ in these studies, but the operating energy ranges are similar. Baumgartner *et al.* presented the performance of a 12×12 pixel array of pitch 2.1 mm in the environment of a balloon-borne experiment, with observations of Cygnus X-1. They reported an energy resolution of 4.8 keV at 60 keV at $+10\,^{\circ}$C, with a threshold of 18 keV, from ground testing experiments. The detectors studied by Sharma, Gaskin and company has a 300-μm pitch, the smallest amongst these studies. They reported an energy resolution of less than 2% at 60 keV at individual pixels of a 16×16 pixel array. As an alternative to CdZnTe, Mitani *et al.* [6] are developing CdTe pixel detectors. They reported a best energy resolution of 1.7 keV FWHM at 60 keV in an 8×8 pixel array of 2-mm pitch at $0\,^{\circ}$C.

As a focal plane detector, each HEFT detector contains over a thousand pixels, with each pixel having its own amplifier circuitry. The output of these pixels combine to form an image; thus, uniformity is desirable in the many properties of each pixel. To address this topic, we present the characterization of some properties of the HEFT detector in this paper.

II. Detector Configuration

The HEFT detector system consists of a CdZnTe-ASIC hybrid detector, an analog-to-digital converter (ADC) for the ASIC output, a microprocessor to operate the ASIC, and support electronics. Fig. 1 is a schematic diagram of a HEFT detector. We refer the readers to our earlier paper [7] for a description of the configuration of the system in more details. In the following, we concentrate on the CdZnTe and ASIC, which are relevant to the experiments described here.

A. CdZnTe

We purchase CdZnTe crystals with platinum electrodes from eV Products. The size of the sensor is 23.6 mm $\times$ 12.9 mm $\times$ 2 mm thick. This was the maximum size available given specification of single-crystal, highly uniform material at the time of our first design. For the detector discussed in this paper, eV Products reports the electron mobility and lifetime as $\mu\tau_e = 2.4 \times 10^{-3}$ cm^2/V. The cathode is a monolithic platinum contact, while the anode plane is patterned into a 24×44 pixel array of 498-μm pitch, surrounded by a guard ring that is 1 mm on three sides, and 0.1 mm on the fourth, the 'mating edge', so that two detectors can be placed side by side to form a roughly square sensor area with minimal dead area in between. Anode contacts in Row 1, alongside the mating edge, are shrunk in length by 60% to accommodate the presence of the thin guard ring, so that the pixel pitch can remain unchanged across the two detectors. The gaps of bare CdZnTe surfaces in between anode contacts are 30 μm in width throughout the entire anode plane. Fig. 2

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The authors are with the California Institute of Technology, Pasadena, CA 91125 USA (e-mail: hubert@srl.caltech.edu).

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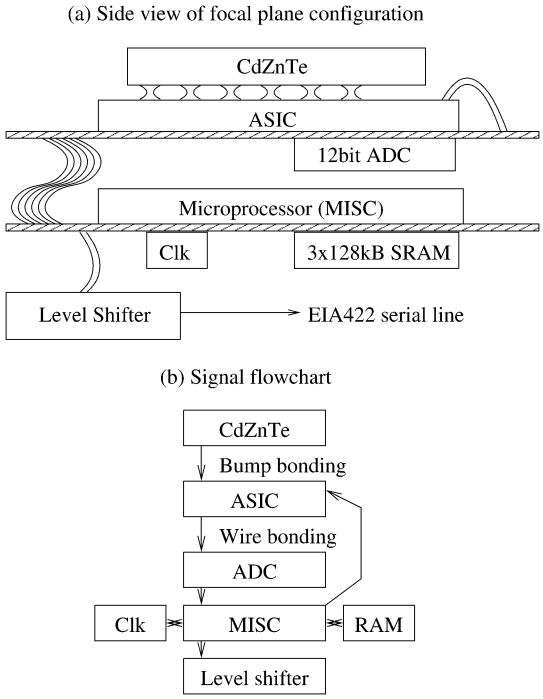

Fig. 1. Schematic diagram of a HEFT detector. (a) The placement of major components in the focal plane assambly. (b) The flow of signals. An X-ray photon captured in the CdZnTe detector produces a signal at the preamplifier input of the ASIC read-out chip. The signal is then amplified and processed in the ASIC and digitized off-chip by a 12-bit ADC. The digitized signal is buffered by the microprocessor and sent out via an EIA-422 serial line. The microprocessor also controls the operation of the ASIC and the ADC. It is implemented as a P24 Minimal Instruction Set Computer (MISC) in a field-programmable gate array (FPGA). See [7] for more details on the system configuration.

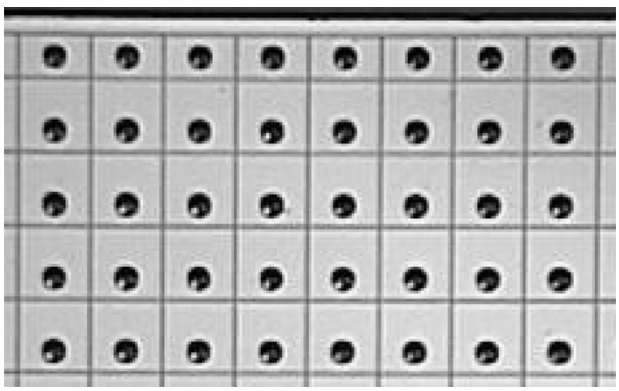

Fig. 2. The anode plane pattern, showing the 30-μm gaps between contacts, and the stencil-printed conductive epoxy bumps prior to bonding with the ASIC chip. The bumps are intentionally offset from the centre of the contacts. The pixel pitch is 498 μm. Pixels along Row 1 at the top are shrunk to accommodate the 0.1-mm guard ring at this mating edge (see Section II-A).

shows the anode plane pattern at a few pixels, including a section of Row 1 and the thin guard ring at the mating edge.

B. Interconnect

The connection between each CdZnTe anode contact to the input of its read-out circuitry on the ASIC is made by flip-chip bonding. Each bond is a series connection of conductive epoxy bumps (on the CdZnTe) and gold stud bumps (on the ASIC). The total height of each connection, from the overglass on the ASIC to the anode plane on the CdZnTe detector, is about 40 μm. Four dots of RTV (room temperature vulcanization) silicone adhesive at the corners of the hybrid detector help to hold the CdZnTe and ASIC together, and no underfill material is used. The gold stud bumps are populated onto the ASIC by Integrated Packaging Assembly Corp, while Polymer Assembly Technology provides the conductive epoxy bumps and performs the flip-chip bonding. More information on these interconnects is presented in [8].

C. ASIC Read-Out

We developed the custom ASIC at Caltech as part of the HEFT program. It consists of a 24×44 pixel array, also of 498-μm pitch, with the pixel pattern matching that on the CdZnTe anode plane. The anode signal is the single input at each pixel; we do not read out the cathode signal with this ASIC. Each pixel is implemented with its own preamplifier, shaping amplifier, discriminator, and sampling and pulsing circuits. All pixels share a serial readout line. The circuitry layout is done using the AMI C5N process (CMOS 0.5-μm N-well).

We designed the ASIC for low noise and power; it consumes about 50 mW of power under normal operation. In order to achieve low power, we have chosen a design that is different from the conventional amplifier chain. In our design, the signal shaping and peak detection stages of the conventional chain are replaced by a bank of 16 switch capacitors arranged to continuously capture successive samples of the preamplifier output. The result is a large reduction in power dissipation—from 250 μW to 50 μW per pixel—while allowing off-chip digital signal processing to extract near optimal energy resolution.

The implementation of the sample and store mechanism with a bank of 16 capacitors is illustrated in Fig. 3. The preamplifier consists of two stages—a charge-sensitive amplifier with a 40 pF capacitor (i.e., a gain of 4 μV per electron), followed by a second amplification stage with a voltage gain of 6. The preamplifier output is converted to a current and is integrated by the switch capacitors, cyclically one by one, with a 1-μs integration time. This process gives us a record of the current level during the previous 15–16 μs at any given time. The preamplifier output is also fed into a simple shaping amplifier with a 300-ns shaping time, and then to a simple peak detect circuit that generates triggers upon events. When a trigger is detected, sampling of the preamplifier output continues for eight more samples, after which the circuit freezes while the voltage levels at the switch capacitors in the triggered pixel are read out of the ASIC chip. The off-chip ADC then digitizes these 16 preamplifier output samples, and send them to the microprocessor. The pulse height of the event is recovered from these 16 samples and related state information at a later time in software.

The HEFT ASIC is sensitive to photons within the energy range 8–200 keV (1600–40 000 electrons), with 15 ADC channels corresponding to 1 keV. We are currently studying the linearity of the energy response. The microprocessor that drives the system runs on an 8 MHz clock. The maximum count rate is 25 counts/s, but we are currently making changes in the microprocessor to double this maximum rate.

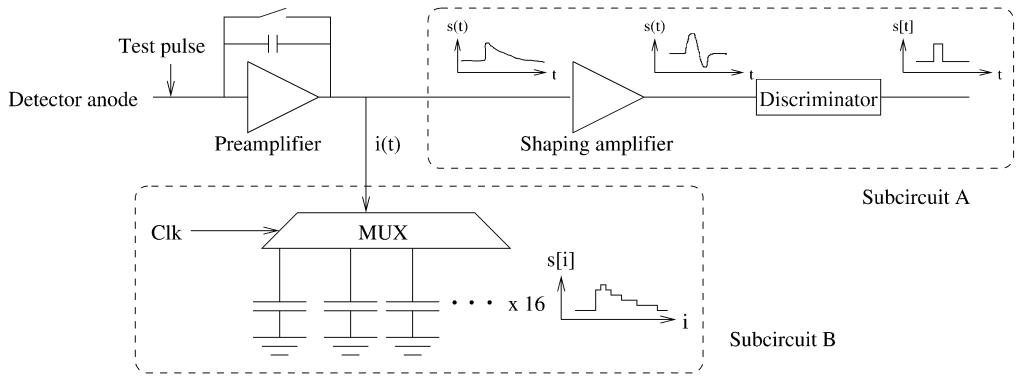

Fig. 3. Schematic diagram of the HEFT ASIC read-out chip. Subcircuit A is the shaping and peak detection stages in a conventional amplifier chain; although this subcircuit exists in the HEFT ASIC, only a simple version is implemented for triggering. Instead, accurate pulse height information is captured in the bank of 16 switch capacitors in Subcircuit B, from which the pulse height is determined. Each pixel in the ASIC contains a copy of the circuit shown in this figure; all pixels share the same serial read-out line for reading out the bank of switch capacitors. See Section II-C.

III. Detector Characterization

In this section, we present the results we have obtained to date from the characterization of our first detector of this design.

A. Electronic Noise

We measure the eletronic noise by sending pulser signals to the input of the preamplifier at each pixel (see Fig. 3), which simulate a 75-keV spectral line. We generate these pulser signals with a precision DC voltage source that is accurate to at least 3 p.p.m., so that the intrinsic variation of the pulser signal is negligible. We then assess the electronic noise as the linewidth of the spectral line produced by the pulser signals, as measured by the ASIC circuitry.

Fig. 4 is a map of the electronic noise at each pixel at room temperature with the bias off. The dark spots represent quieter pixels, whereas the bright spots represent noisier pixels. The same data is tallied here into a histogram, whose horizontal axis is aligned with the color scale for the map. For our detector, the electronic noise amplitude is dominated by the input capacitance between the anode contacts on the CdZnTe and the ASIC backplane. So, unconnected pixels such as the ones at the bottom left corner of the map have lower noise amplitudes, as indicated in their positions in the histogram, between 300 and 400 eV (60–80 electrons). Also, the contacts are narrower in the row of pixels next to the mating edge of the detector. Here, the electronic noise amplitude is also smaller than the other pixels on the detector. On the other hand, pixels with relatively high noise amplitudes are found interspersed over the entire detector rather than concentrated in the same place. This suggests random defects in the VLSI fabrication process as a potential cause of the increased noise magnitude. However, the majority of the pixels display good uniformity in noise characteristics across the entire pixel array. On average, the electronic noise in our detector is (540 ± 56.4) eV, or 108 ± 11.2 electrons, at room temperature. At lower temperatures, the noise amplitude decreases. On the other hand, it increases when a bias is applied across the detector. The combined effect of temperature and bias at 0 °C and HV $= -400$ V is a net increase of the noise amplitude by about 100 eV.

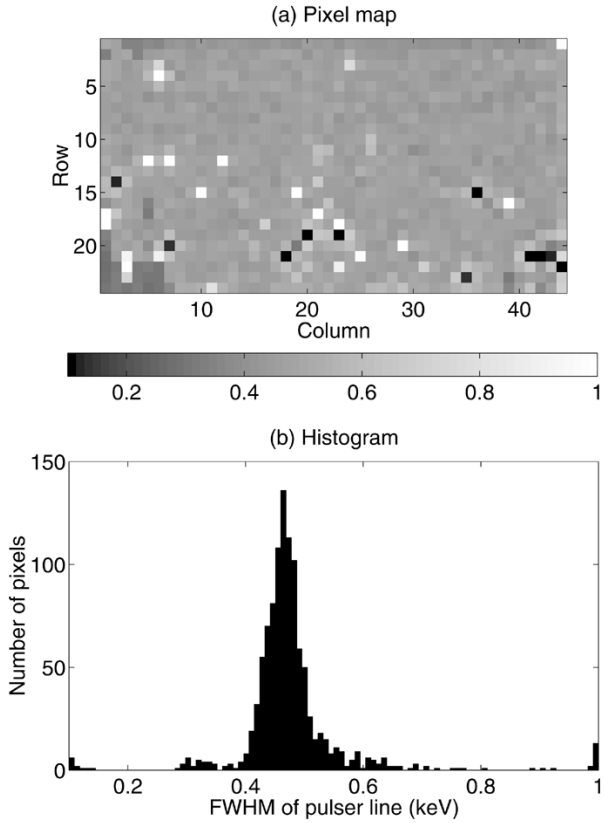

Fig. 4. (a) Map and (b) histogram of the electronic noise distribution at room temperature (23 °C), with the voltage bias off. The mean and standard deviation of the distribution are 540 and 56.4 eV, respectively (108 ± 11.2 electrons). The pixels at the bottom-left corner are unconnected, and thus have lower noise amplitudes, between 0.3 and 0.4 keV FWHM (i.e., 60–80 electrons). All anode contacts on Row 1 are narrower than the ones in the remaining rows (see Section II-A); note the lower noise level across row 1.

B. Leakage Current

Another property of interest is leakage current. We obtain the leakage current at a pixel by measuring the amount of charge accumulated in the sampling capacitors (see Fig. 3) within a fixed duration when the bias across the detector is off, and when it is on. We then derive the leakage current going into the preamplifier input from the difference in charge accumulated with and

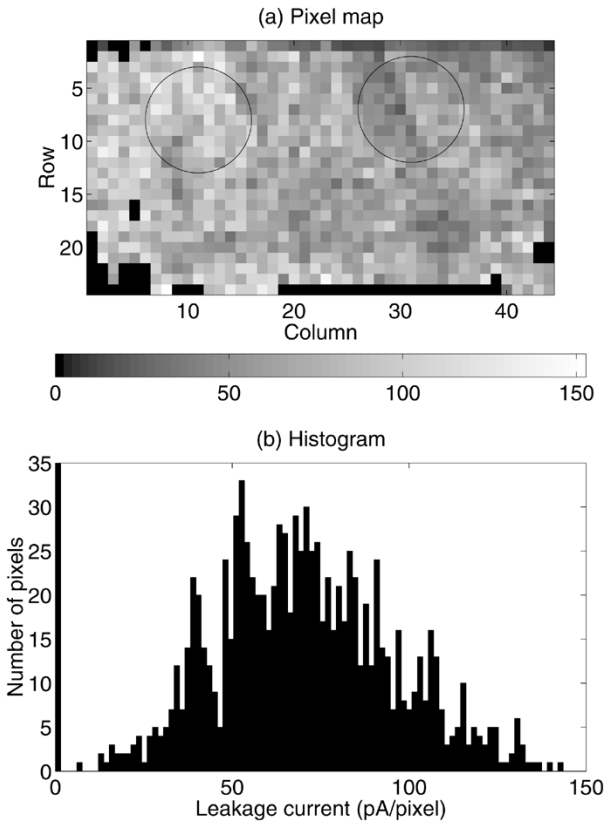

Fig. 5. Leakage current (a) map and (b) histogram at room temperature (23 °C) and detector bias HV $= -250$ V. There is substantial variation in the leakage current at room temperature, with strong spatial correlation. The circles indicate the two regions at which Am-241 spectra are obtained at 0 °C. The spectra are displayed in Figs. 7 and 8.

without the bias, from the time period, and from the preamplifier gain.

Fig. 5 shows the map and histogram of leakage current at each pixel, at room temperature; again, the brighter pixels indicate higher leakage currents, while the darker pixels indicates lower leakage currents. The map and histogram both show that there is substantial variation in the leakage current in this 12×22 mm^2 area of CdZnTe. One also sees in the map a strong spatial correlation in the size of the leakage current. However, if one cools the detector down to 0 °C, then the leakage current becomes negligible. We plot simple i–v curves at the two temperatures in Fig. 6.

For practical reasons (to collect sufficient statistics in a reasonable time), we further study the performance of a subset of pixels with an X-ray source at 0 °C. Although the leakage current is negligible at this temperature, we have nevertheless chosen two regions of pixels with very different leakage characteristics at room temperature for further study, as this choice can potentially reveal further differences in material properties in the two regions. These two regions are indicated by the two circles in Fig. 5. The circle on the left marks a high-leakage region, while the one on the right marks a low-leakage region.

C. Spectral Resolution

For each of the two regions selected, we illuminate it with an Am-241 source that is collimated to within a circle of about

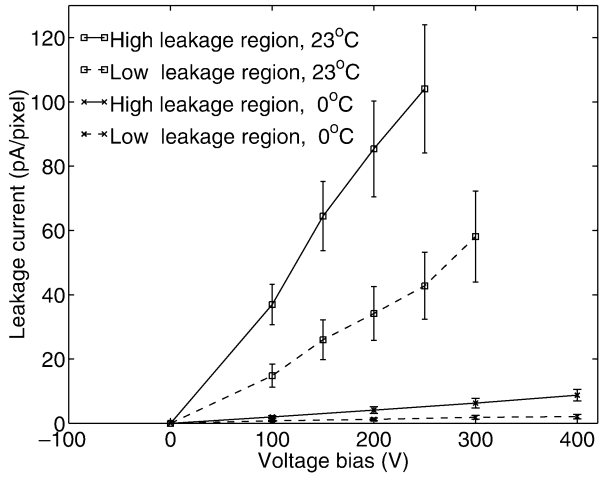

Fig. 6. Current–voltage relations for the two regions circled in Fig. 5, at two different temperatures. There is substantial difference in the two regions at room temperature, but the leakage current becomes negligible at 0 °C. From these measurements, the apparent bulk resistivity at room temperature is 3.4×10^{10} Ω-cm in the high leakage region and 6.3×10^{10} Ω-cm in the low leakage region. At 0 °C, it is above 5×10^{11} Ω-cm in both regions.

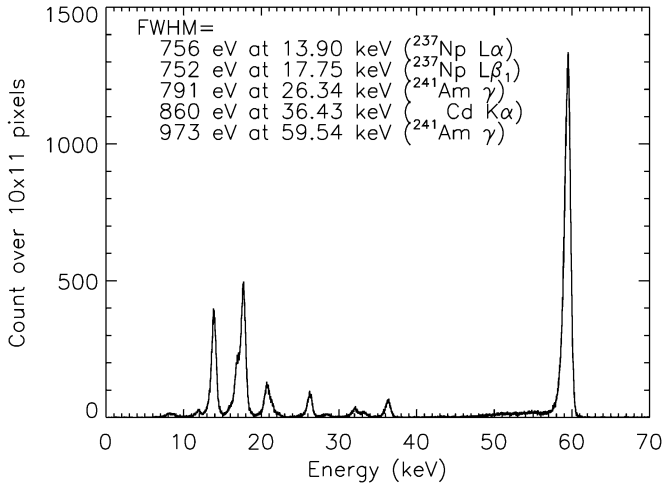

Fig. 7. Am-241 spectrum at 0 °C, obtained from the high-leakage region (at room temperature) circled in Fig. 5. The cathode-to-anode potential is HV $= -400$ V. Data collection took place for 69 minutes.

ten pixels in diameter. We then measure the spectrum at each region at 0 °C, which are shown in Fig. 7 for the region with high leakage currents at room temperature, and in Fig. 8 for the region with low leakage at room temperature. Both of these spectra include all events where one or two adjacent pixels are triggered (we refer to them as one- and two-pixel events, respectively, in short). A tally of the experimental data indicates that one- and two-pixel events account for more than 90% of all the events when the detector is illuminated with a source flooding the region under study, with the remainder being events with three or four adjacent pixels triggered. This statistics is consistent with detector modeling results we found previously [9].

The processing of events with multiple pixels triggered requires additional explanation. For two-pixel events, one has to reconstruct the photon energy by adding the pulse heights from the two triggered pixels together, with the different gains and offsets of the two pixels properly corrected. These corrections

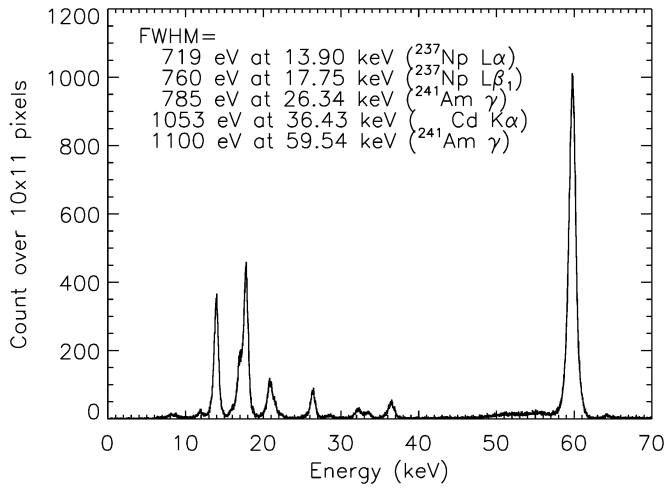

Fig. 8. Am-241 spectrum at 0 °C, obtained from the low-leakage region (at room temperature) circled in Fig. 5. The cathode-to-anode potential is HV $= -400$ V. Data collection took place for 58 minutes.

are done in software, after the pulse height from each triggered pixel is calculated individually from the samples read out and digitized from the ASIC circuitry (see Section II-C). For events with more than two pixels triggered, we currently do not process them, due to their relatively small contribution, and they do not enter the spectra shown in Figs. 7 and 8.

At low energies, electronic noise is the dominating component of the X-ray line widths. At high energies, the line width is further affected by variation in the depth of photon interaction, and the energy resolution is close to about 1 keV (200 electrons) FWHM at 60 keV at 0 °C. As was indicated in the previous section, leakage current turns out not to be an issue at 0 °C.

D. Count Rate Uniformity

Yet another important property for a pixel detector is the uniformity of count rate. We measure the count rate by illuminating the entire detector with an uncollimated point source of Am-241 and measuring the number of counts at each pixel. This measurement was done at room temperature, and the detector bias was set to HV $= -80$ V, a value that is high enough for the detector to be operational, but just low enough that no pixel is saturated by the leakage current.

Fig. 9 shows the map and histogram of the count rate for one- and two-pixel events (ie, over 90% of all events) that correspond to the 60-keV line; as this histogram indicates, we have observed high variation in the count rate that is clearly more than merely Poisson statistics, with the variation being close to the mean. On the positive side, these variations are stable—the count rate at a given pixel remains the same over time—thus, the variation is correctable when the detector is put into use. However, we have tested an identical ASIC that is bonded to a cadmium telluride sensor instead of CdZnTe, and we have not seen such high count rate variation with the cadmium telluride detector. So, this variation in the count rate seems to be a CdZnTe property. Also, when an equal number of test pulses are sent to the input of the electronics at each pixel, no such variation is seen in the number of test pulses detected; this excludes the behavior of the ASIC circuitry as a source of the variation.

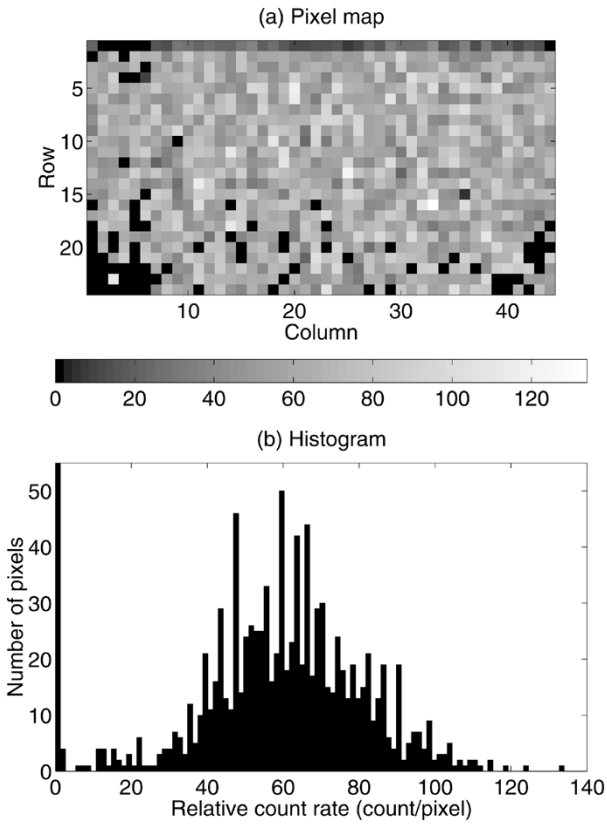

Fig. 9. Count rate (a) map and (b) histogram. The data was taken at room temperature and detector bias HV $= -80$ V. This bias is high enough for the detector to be operational, but just low enough for none of the pixels to saturate at room temperature. Only events corresponding to the 60-keV line of Am-241, and events triggering one or two pixels are included in this figure. The mean and standard deviation of the distribution are 61.8 and 19.5 counts/pixel, respectively.

Per our detector specification to eV Products, this detector should be a single crystal, and should contain no precipitate greater than 100 μm in size. eV Products supplied us with a photograph of the detector taken with infrarad microscopy before the contacts were deposited, and the photograph shows no significant feature that can explain this count rate variation. We suspect that this variation may be due to a nonuniform electric field within the CdZnTe, which causes each pixel to have a different 'effective collecting area'. If this is indeed the case, then a gain in collecting area by a pixel will be compensated by a corresponding loss of area by neighboring pixels. So, if one averages the count rate at each pixel with the rates at its neighbors, the resulting distribution should be fairly uniform. This distribution is shown in Fig. 10, where we convolve the rates in Fig. 9 with a boxcar of three pixels in width in each direction. The distribution after this convolution agrees with Poisson statistics (mean $= 60.98$ counts; $1\sigma = 8.48$ counts). Based on the same logic, one would expect to see a correlation between the count rate and the leakage current at each pixel. The correlation is plotted in Fig. 11, and we do see some correlation.

We note that this investigation of the count rate is still under active investigation as of the writing of this paper; a scan of the detector with a fine X-ray beam and the calibration of the beam with a detector of known efficiency, both to be done in the near future, will provide us with more concrete information

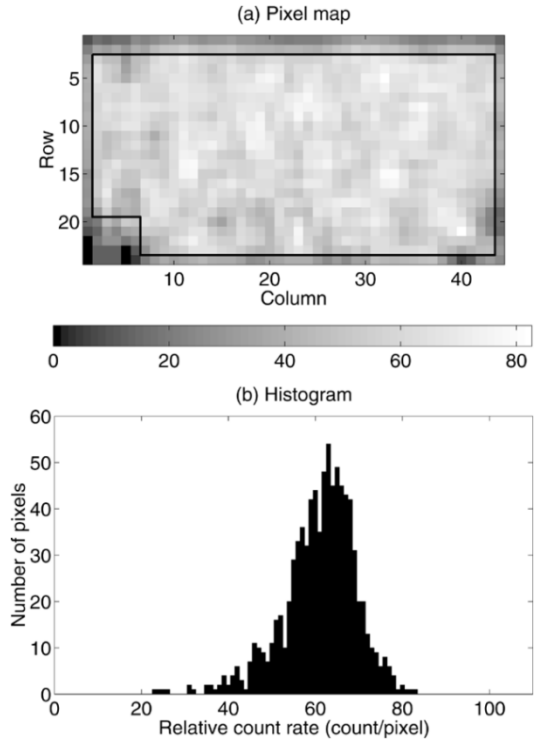

Fig. 10. (a) Map and (b) histogram of the count rate (displayed in Fig. 9) convolved with a boxcar of three pixels in width in each direction. Pixels on Row 1 are narrower (see Section II-A), and the count rates are thus lower accordingly. The lower rates on Row 2 and at the remaining three edges of the detector are due to the convolution of a finite data set. Pixels at the lower left corner are unconnected. These edge pixels and unconnected pixels are not included in the histogram; specifically, only pixels within the interior rectangle marked by Rows 3–23 and Columns 2–43, and outside the unconnected region marked by Rows 20–23 and Columns 2–6, are included in the histogram. The included pixels are outlined in the pixel map in (a) above. Mean $= 60.98$ counts; $1\sigma = 8.48$ counts.

TABLE I
SUMMARY OF SOME QUANTITATIVE PROPERTIES OF THE HEFT DETECTOR

Property	Range
Leakage current	10–140+ pA/pixel at 23^oC
	0–10 pA/pixel at 0^oC
Eletronic noise	(540 ± 56.4) eV FWHM at 23^oC, bias off
Spectral resolution	$\approx$ 1.0 keV FWHM at 60 keV at 0^oC
Count rate	variation $\approx$ mean

on the count rate. Until we report further on the results of these investigations, this report on count rate variations can only be considered preliminary, and any conclusion made in this section speculative.

IV. SUMMARY

For the HEFT, we have developed CdZnTe pixel detectors with large format, fine pitch and low power consumption. The leakage current varies substantially at room temperature, but is negligible at 0 °C. The electronic noise is around 500 eV at 23 °C, whereas the spectral resolution is about 1 keV FWHM at 60 keV at 0 °C. Table I summarizes the values of various quantities for the detector. We are still actively investigating the high variation in the count rate, and we shall report new results on this topic in a future paper.

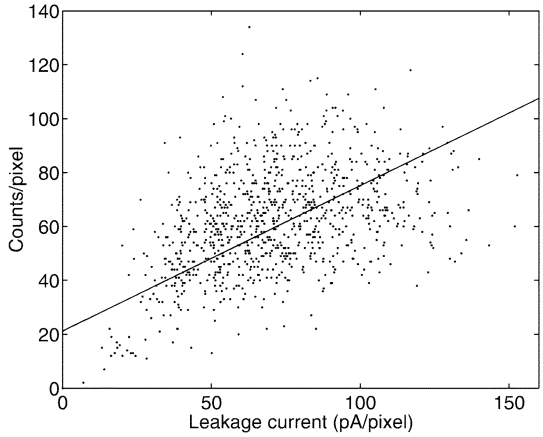

Fig. 11. Leakage current-count rate correlation for the HEFT detector. The count rates are from Fig. 9 (room temperature, HV $= -80$ V), and the leakage currents are from Fig. 5 (room temperature, HV $= -250$ V). Unconnected pixels and pixels registering fewer than 10 event counts are not shown in this figure. The cause of the low count rates at these pixels are likely unrelated to the leakage current, and distorts the correlation. The remainder of the data points, shown in dots, are fitted with a straight line relation, counts$= 0.54 \times (\text{current}/\text{pA}) + 21$, which is also shown in the figure.

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