9.4 A Scalable 6-to-18GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS

Sanggeun Jeon, Yu-Jiu Wang, Hua Wang, Florian Bohn, Arun Natarajan, Aydin Babakhani, Ali Hajimiri

California Institute of Technology, Pasadena, CA

Very-large-scale phased arrays (~10^6 elements) can provide tremendous array gain, noise improvement, and beamforming capabilities for a variety of applications such as radar and communications. Such phased-array systems have traditionally been implemented using compound semiconductors in a module-based approach. However, the dominant cost of these systems is in the electronics. Thus, the large number of active elements involved results in a very high price tag limiting the size of the phase arrays.

Integrated CMOS solutions offer an opportunity for dramatic cost and size reduction in such systems. The high yield and repeatability of silicon ICs allows the entire transceiver to be integrated on a single chip resulting in an order of magnitude reduction in the overall system cost [1, 2]. Silicon CMOS also offers new opportunities for concurrent programmable multi-beam multi-band solutions over a broad range of frequencies with fast response time.

This paper describes the general architecture and the signal-path behavior of a CMOS programmable phased-array receiver element that simultaneously operates at two frequencies between 6 and 18GHz (a tritave) while forming four independently controlled beams (Fig. 9.4.1). A large number of these elements can be used to form a phased array of arbitrary size. Each of the horizontal and vertical polarizations (HP and VP) of the received signal, separated and amplified at the active antenna module, is fed to an on-chip tunable concurrent amplifier (TCA). Each TCA splits the incoming signal into two separate frequency bands, a low-band (LB) from 6 to 10.4GHz and a high-band (HB) from 10.4 to 18GHz (Fig. 9.4.2). The LB and HB signals are then fed to two separate RF mixers driven by the first local oscillator (LO_1). The signal downconversion to baseband is performed in two steps. The phase shifting is done at the second local oscillator (LO_2) using an array of four pairs of in-phase and quadrature mixers (2 pairs per polarization and 2 pairs per band). Each LO phase of the second downconversion mixers is generated independently by the on-chip frequency synthesizers and digital phase rotators [3]. The reference signal of each receiver element is generated from a single off-chip 50MHz crystal oscillator. The downconverted baseband signal is further amplified by a VGA. The signals from each array element are then combined at baseband in a hierarchical fashion allowing for full scalability to very large arrays.

The signal combining improves the effective phase noise of the array output by a factor of 10log(N) (where N is the number of elements combined), compared to a single receiver element. This is due to the uncorrelated nature of the phase noise sources and makes it possible to use on-chip frequency synthesizers for beam forming applications which require low phase noise.

Two desired RF signals with different frequencies in the LB and HB at each polarization are concurrently amplified, filtered, and split into two separate single-ended outputs by a TCA, shown in Fig. 9.4.3. The wideband input matching to 50Ω is accomplished by an active termination with resistive feedback and an impedance transformation network. The active termination contributes less noise to the subsequent blocks than a simple shunt resistive termination [4]. The RF signals are then selectively amplified by two separate cascode amplifiers that have tunable LC output loads. A 3-bit switched capacitor bank at each output load is tuned to cover the entire LB and HB frequencies. This allows for the digital tuning of the amplifier so that it can provide the maximum gain at the desired frequency while attenuating out-of-band signals prior to the first downconversion.

The four resultant RF signals (two bands for each of the two polarizations) are then downconverted in two steps via current-commuting double-balanced mixers. While a shunt-peaking inductor has been used in the LB RF mixers to extend the operating bandwidth, the HB RF mixers have a tunable LC load with a 3-bit switched capacitor bank. One input of the RF mixers is terminated by a bias voltage to convert its single-ended input to differential. The quadrature IF mixers perform not only the second downconversion but also the phase shifting with the digitally controlled phases of LO_2. Eight differential baseband buffers, one for each combination of two frequency bands, two polarizations, and I and Q, drive 100Ω differential output impedance with 1.5V external supply. The baseband VGAs provide 11dB of gain variation in five steps.

The receiver relies upon a dual frequency scheme where the LO_2 frequency switches between 1/2 and 1/8 of the LO_1 frequency which varies from 5 to 7GHz for the LB and from 9 to 12GHz for the HB (Fig. 9.4.2). This dual scheme reduces the required VCO tuning range from 1:1.7 to 1:1.3 with no blind spots within the entire tritave. The phase synthesis process independently generates 2^{10} (~10^3) distinct constellation points for phase and amplitude of LO_2 driving each IF mixer [3]. This dense phase configuration is essential for compensating phase errors that are induced by I/Q mismatches and excessive harmonic contents of the LO_2 signals as well as any skew or systematic error in the distribution of the off-chip reference signal. The selection of RF receiving frequency, LO frequency, and phase shifting is controlled by a built-in digital serial bus.

The wideband phased-array receiver is implemented in a 0.13µm CMOS process with eight metal layers. Fig. 9.4.4 shows the measured performance of the receiver element over the tritave. Particularly, the cross-polarization and cross-band rejections are higher than 63.4dB and 48.4dB, respectively. The discontinuities at 7.6, 10.4, and 13.5GHz occur when the receiver switches the operating band or the frequency scheme. The phase-shifting resolution of the receiver is better than 5° within 2dB baseband amplitude variation across the entire tritave. For the testing of phased-array performance, four receiver chips have been combined together with phase-shifted RF inputs to form an effective wavefront. The phases of LO signals in the four receivers are synchronized by symmetrically distributing the off-chip 50MHz reference signal and calibrating out any remaining systematic skew through the adjustment of the on-chip LO_2 phase. Figure 9.4.5 shows the normalized array patterns at 6, 10.4, and 18GHz of RF with four different LO phase settings. The complete performance summary of the receiver and the four-element array is given in Fig. 9.4.6. Figure 9.4.7 shows a micrograph of the receiver chip that occupies 3.0×5.2mm^2.

Acknowledgments:
This work was supported by ONR's award #N00014-04-C-0588. We thank ONR and Raytheon, particularly J. DeFalco and R. Healy for their helpful feedback.

References:
[1] H. Hashemi, X. Guan and A. Hajimiri, "A Fully Integrated 24GHz 8-Path Phased-Array Receiver in Silicon," *IEEE ISSCC Dig. Tech. Papers*, pp. 390-391, Feb. 2004.
[2] A. Natarajan, A. Komijani, X. Guan et al., "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Transmitter and Local LO-Path Phase Shifting," *IEEE J. Solid-State Circuits,* vol. 41, no. 12, pp. 2807-2819, Dec. 2006.
[3] H. Wang and A. Hajimiri, "A Wideband CMOS Linear Digital Phase Rotator," *IEEE Proc. CICC*, pp. 671-674, Sep. 2007.
[4] P. Ikalainen, "Low-Noise Distributed Amplifier with Active Load," *IEEE Microwave Guided Wave Lett.*, pp. 7-9, Jan. 1996.

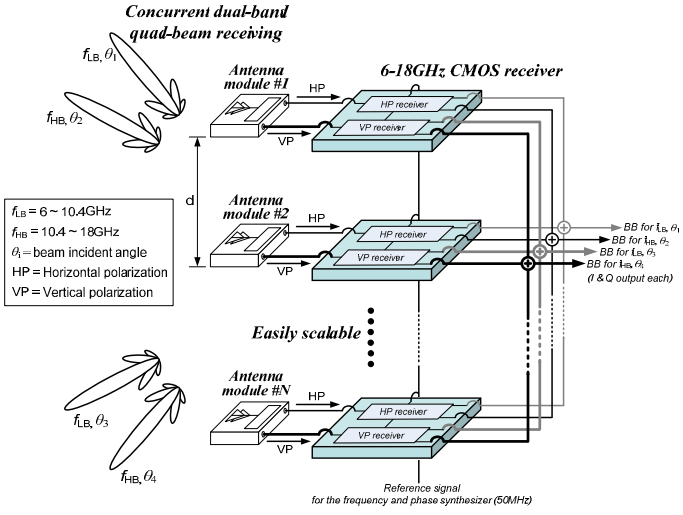


Figure 9.4.1: Scalable 6-to-18GHz concurrent dual-band quad-beam phased-array system.

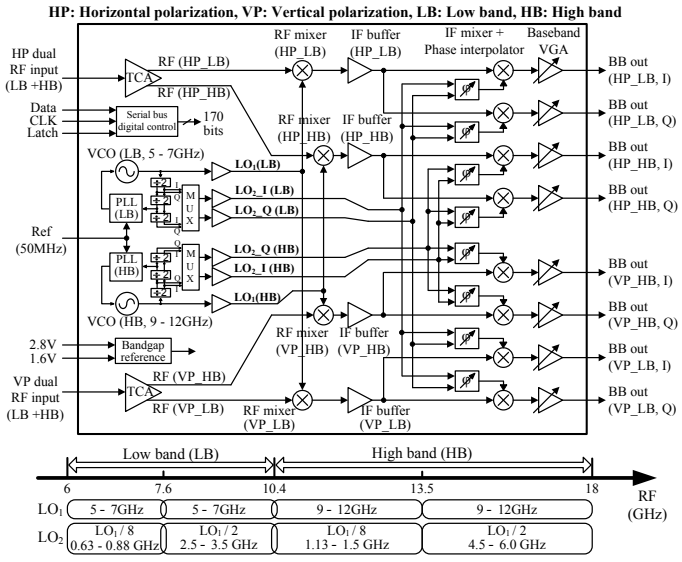


Figure 9.4.2: Architecture and frequency scheme of the receiver element.

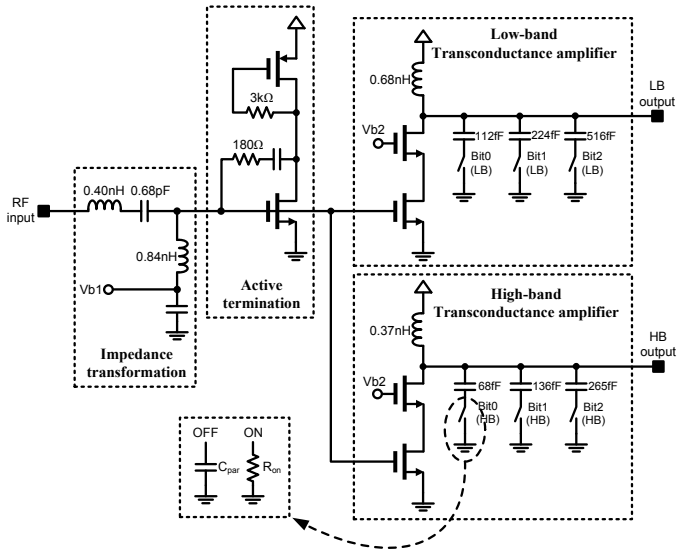


Figure 9.4.3: Schematic of the TCA.

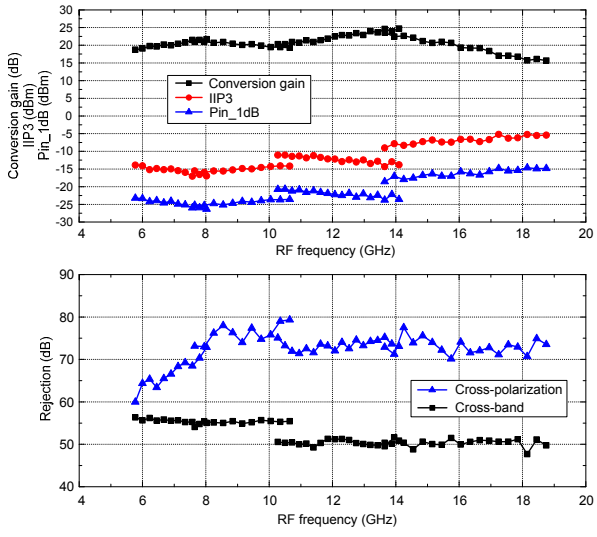


Figure 9.4.4: Measured performance: conversion gain, IIP3, Pin_1dB, cross-band and cross-polarization rejections.

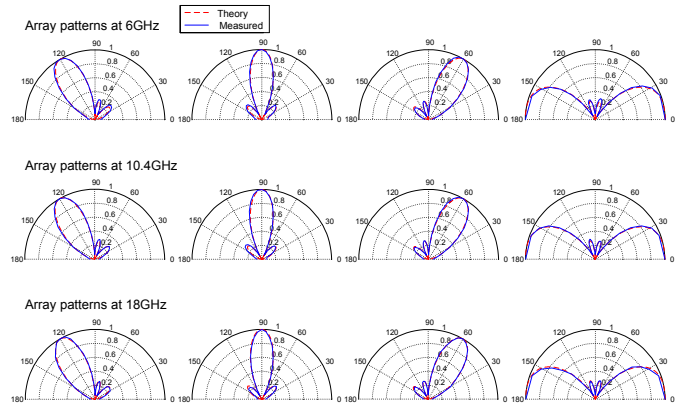


Figure 9.4.5: Measured array patterns (antenna spacing= λ/2 at each frequency).

Receiver Element Performance

Conversion gain (6 – 18GHz)		15.7 ~ 24.7dB
Input-referred 1-dB compression (6 – 18GHz)		−25.9 ~ −14.7dBm
Input-referred IP3 (6 – 18GHz)		−17.0 ~ −5.2dBm
Input return loss (6 – 18GHz)		> 9.5dB
Cross-polarization rejection (6 – 18GHz)		> 63.4dB
Cross-band rejection (6 – 18GHz)		> 48.8dB
LO leakage (6 – 18GHz)		< −24.5dBm
Antenna-to-baseband noise figure† (6 – 18GHz)		2.6 ~ 3.1dB
Phase shifting resolution (6 – 18GHz)		< 5° (within 2dB amplitude variation)
RF channel spacing		225MHz (Div8 LO_2), 300MHz (Div2 LO_2)
Power consumption	RF and LO circuitry	658mA @2.7V, 217mA @1.6V
	Baseband buffers	328mA @1.5V
Technology		130nm CMOS
Die area		3.0×5.2 mm²

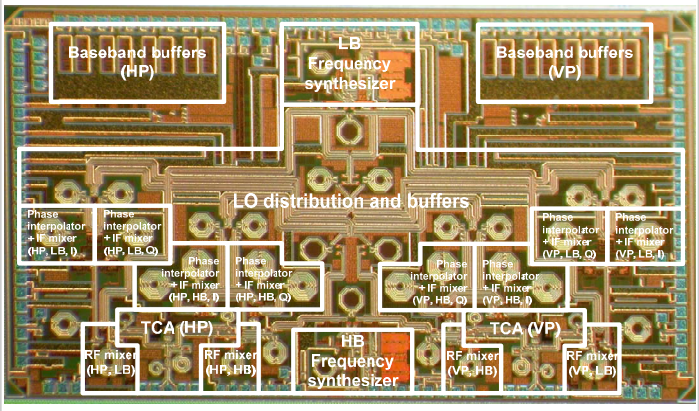
†Including the gain and noise figure of the antenna module consisting of the dual polarized antenna and wideband LNA.

Phased-Array Performance (4 elements measured at 6-, 10.4-, and 18-GHz)

Number of beams concurrently receivable	4
Phase shifting resolution per element	< 5°
Total phased-array gain	> 27.7dB
Beam-forming peak-to-null ratio	> 21.5dB

Figure 9.4.6: Measured performance summary.

Continued on Page 605



HP: Horizontal polarization, VP: Vertical polarization
LB: Low band, HB: High band

Figure 9.4.7: Chip micrograph.

 978-1-4244-2011-7/08/$25.00