Germanium nanowires: from synthesis, surface chemistry, assembly to devices

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In order to continue the ever impressive and successful scaling pace of MOSFETs, tremendous research efforts have been spent to seek new materials to complement or replace Si as the Si-based ones are predicted to reach theoretical limits soon. Ge has low band gaps and high carrier mobilities, thus offering appealing potentials as a candidate of choice for future electronics. For the same purpose of discovering new materials, another area of interest is low dimensional nanostructures such as nanowires (NWs), owing to the facile synthesis, high structure perfection and superior properties. In this context, Ge NW has combined advantages and is particularly promising. I focus on this subject and have advanced in a wide range, from understanding and controlling synthesis and surface chemistry, to highly ordered assembly and devices with excellent performance.

Single crystalline Ge NW can be readily synthesized with a simple chemical vapor deposition (CVD) method at low temperatures from Au nanocluster seeds, with GeH_4 as the feeding stock. The mechanism follows the widely accepted vapor-liquid-solid (VLS) one, in which reactive Ge species decomposed from GeH_4 diffuse into Au seeds and form alloy; after super saturation, excess precipitate out and prolongate to form single crystalline NW. The NW diameter is defined by the seed size and the length is determined by growth duration. Since GeH_4 decomposes easily and the Ge-Au binary alloy has a low eutectic temperature, an unprecedented low temperature of 275°C is achieved. The key to an optimum growth is balanced Ge feeding and its diffusion in growth seed (Figure 1). Understanding and refining the growth chemistry enable excellent control over the synthesis. For example, 100% yield of Ge NWs relative to the Au seeds is obtained, with one-to-one correspondence of NWs to the seeds. This result leads to deterministic GeNW synthesis by patterning of individual Au nanoclusters. Furthermore, these deterministically grown NWs can be aligned into quasi-parallel arrays with a simple post-growth fluidic treatment. Optimized NW growth also makes gram-scale synthesis possible by supporting the growth seeds on high surface area material such as silica. Additionally, *in situ* doping during the growth is achieved with co-flows of precursors containing desired dopants, e.g. PH_3 for n-type and B_2H_6 for p-type, and the doping level can be controlled by adjusting the ratios of Ge to dopants.

Nanostructures have considerably higher surface areas than their bulk counterparts, therefore surfaces often play important, sometimes even dominant, roles in the nanostructure properties. For instance, we have calculated quantitatively that existing surface potentials can affect cylindrical semiconductor NWs more significantly than planar ones: $\frac{4\pi\varepsilon_0\varepsilon\phi_0}{2\pi n} = \left(1-\frac{d}{3R}\right)d^2$. (Equation 1)

The surface chemistry of Ge NWs is studied in a systematic manner and a few novel findings are unveiled. First, Ge NWs with different doping types exhibit different chemical stabilities. It is evident in our experiments that p-type Ge NWs are more stable in ambient air than n-type ones, due to the Fermi level difference for each doping type. Second, with high resolution x-ray photoelectron spectroscopy (XPS), we have quantified the Fermi level of Ge NWs and mapped out the bending due to surface potentials (Figure 2). The bending trend is identified to be opposite for p and n-type. Third, distinct oxidation routes of Ge NWs with p or n-type doping are uncovered for the first time. In the oxidation process, reactive n-type NWs form GeO_2 directly and quickly while p-type ones form GeO first and then gradually convert to GeO_2. In an effort to block the surface oxidation, we find long chain alkylthiols are effective to passivate Ge NWs. The protection is quantified by comparing the degree of oxidation as a function of time for different alkyl chain length. Other chemistry such as alkalization is compared as well and C_{12} thiol yields the best resistance to oxidation.

Successful applications of nanostructures require controlled assembly to afford highly ordered structures at low cost. We have investigated two general assembly techniques for Ge NWs: deterministic synthesis and Langmuir-Blodgett (LB) transfer. As discussed earlier, deterministic synthesis offers ultimate control over NW growth, such as sizes, locations and orientations, etc. It naturally provides a platform for high quality NW assembly and has been successfully demonstrated in our studies. On the other hand, our gram-scale NW synthesis produces high quality bulk quantity materials with uniform properties. We use LB technique as a cost-efficient method to assemble bulk quantity NWs that are functionalized with alkylthiols. This method utilizes the hydrophobity of the alkyl terminations, which help float NWs on H_2O surface. Upon compression, these free-floating NWs are close-packed into parallel arrays, which can be transferred to various substrates with their order undisturbed. For both deterministic synthesis and LB assembly, the essential enabling factor is the cleanness offered by CVD reactions, with which by-products other than high quality NW growth are negligible.

The electrical properties of semiconductor NWs is best manifested in the performance of their field effect transistors (FETs), which also serve as a direct measure of their usefulness as electronic materials. To fabricate Ge NW FETs, we grow doped NWs in a patterned fashion on a heavily doped Si substrate with a SiO_2 capping layer. Afterwards, source (S) and drain (D) contacts are defined and high workfunction metal Pd is deposited as electrodes. In this geometry, the SiO_2 layer works as gate dielectrics and underlying Si is the gate electrode. High hole mobilities ~600cm^2/V-s are obtained. The electrical properties are correlated with the surface characteristics to understand the role of surfaces in nanoelectronics. It is revealed that NW FET properties are highly dependent on the surfaces. As an example, large hystersis is observed for both p and n-type NW FETs when measured in ambient air as a result of strong H_2O absorption to surface oxides (GeO_2). The hystersis can be easily removed for p-FETs by eliminating surface oxides whereas it is persistent for n-FETs due to the easy oxidation of n-type Ge NWs. Thus, for NWs, it is of critical importance to control the surfaces, e.g. functionalizations to reduce surface states and protection against oxidation, etc. For such a goal, we have investigated the compatibilities of Ge NW FETs with high dielectric constant (high-κ) materials deposited by atomic layer deposition, or ALD, because it has

been shown that ALD high-κ can produce excellent Ge-based MOSFETs. Decent device performance comparable to bottom gated FETs is achieved. We have also characterized Ge NW FETs with surfaces protected by alkylthiols and observed drastic device improvement in terms of performance and stability in ambient air. Moreover, this surface modification eliminates surface effect on bulk properties of NWs and makes it possible to probe the intrinsic properties of NWs. We have measured band gaps of Ge NWs with different sizes and found that it is similar to bulk Ge for NWs down to ~10nm in diameters. These types of measurements could only be performed with proper surface functionalizations.

In summary, Ge NW has been studied systematically in my thesis, from synthesis and surface chemistry, to controlled assembly and high performance devices. Many of the approaches and results are generic to other types of NWs as well. Doors are opened up to interesting sciences and applications of this novel structure.

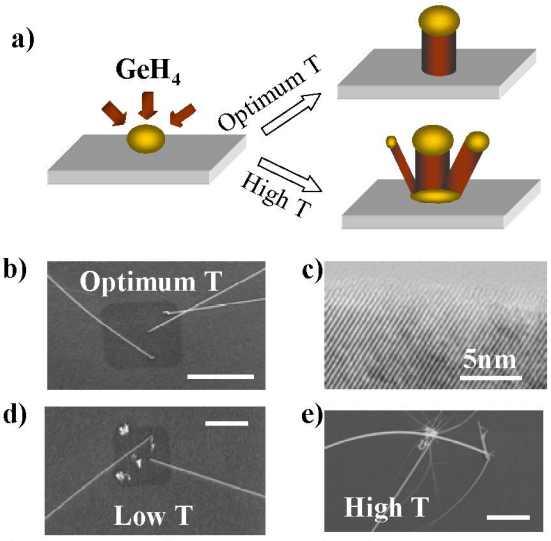

Figure 1. Optimum growth of GeNWs.

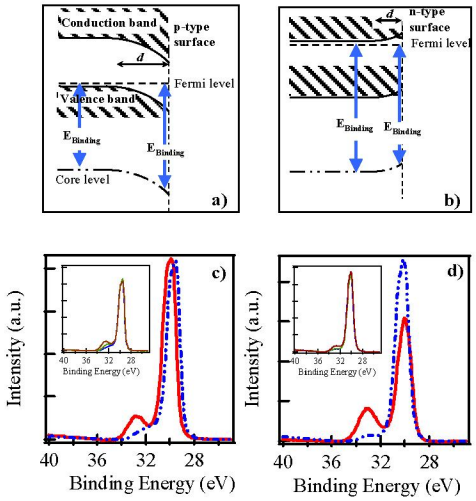

Figure 2. Opposite band bending and distinct oxidation of GeNWs with different doping types.

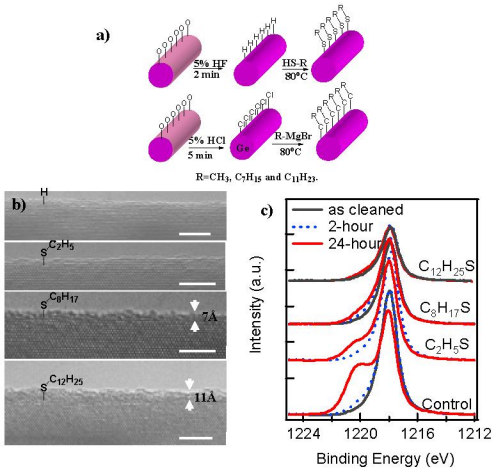

Figure 3. Surface passivation with long chain alkylthiols

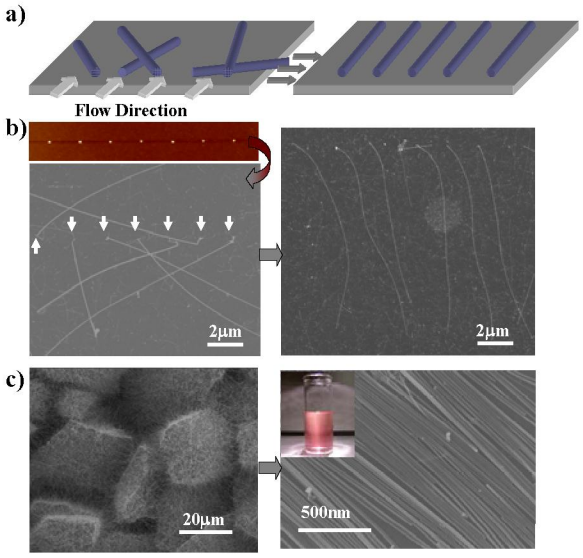

Figure 4. Controlled assembly toward parallel nanowire arrays

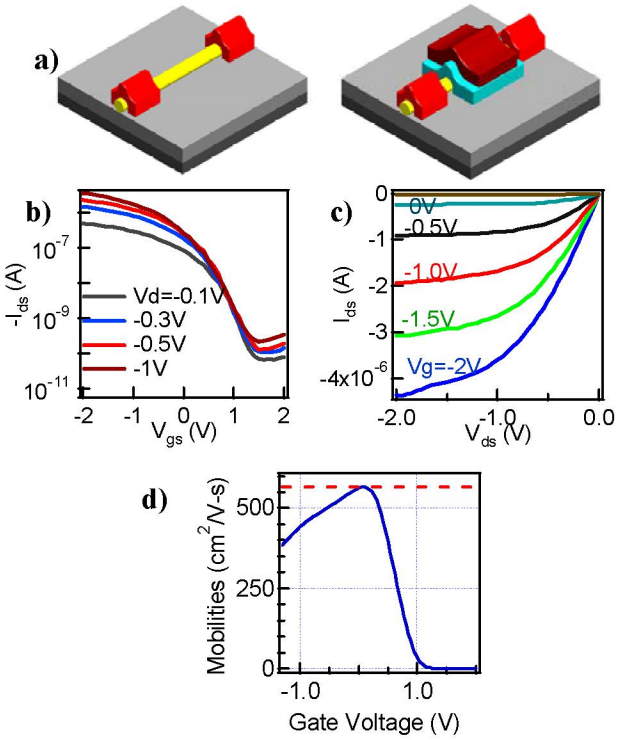

Figure 5. GeNW FETs with SiO_2 and HfO_2 as gate dielectrics.