The emergence of a coupled quantum dot array in a doped Silicon nanowire gated by ultrahigh density top gate electrodes

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Supplemental Online Materials

Device Fabrication (Please refer to Fig. 3 and Fig. 4 in the text)

The starting structures are single-crystal silicon nanowires (SiNWs) defined by patterning a 30 nm thick silicon-on-insulator (SOI) substrate with a 250 nm thick buried oxide (<100> orientation; Simgui, Shanghai, China). The SOI substrate is first doped with boron by thermal diffusion of a spin-on dopant (Boron A, Filmtronics, Butler, PA) to a level of $\sim 5\times10^{18}$ cm^{-3},(Wang *et al.* 2006) as determined by four-point resistivity measurements. The larger SiNWs (~40 nm wide, 30 nm thick) are then patterned using electron-beam lithography (EBL) with aluminum as mask material, while the smaller SiNWs (~17 nm wide, 30 nm thick) are obtained by sectioning out a single NW from an array of SNAP SiNWs: an array of ~17 nm wide SiNWs with 50 nm spacing is first patterned from the SOI using SNAP, (Melosh *et al.* 2003; Beckman *et al*. 2004) and then EBL-defined, ~50nm wide aluminum mask is put down to protect one single SiNW in the array, while all other NWs are etched away with reactive ion etching.

Metallic contacts (Ti/Pt, 20nm/30nm) are established to the SiNWs by EBL to generate source-drain channels that vary in length from 100 – 300 nm. The device is then annealed in forming gas (5% H_2 in N_2) at 475 °C for 5 min to promote low-barrier source/drain contacts,(Wang *et al.* 2006) before a dielectric layer (silicon oxide, 15 nm) is put down on top, followed by a 35 nm titanium layer. An array of ultrahigh-density platinum SNAP NWs(Melosh *et al.* 2003) with ~17 nm width and 33 nm pitch is glued down on top of the titanium layer, perpendicular to the underlying single SiNW, and reactive ion etching (RIE) is used to transfer the platinum pattern into the titanium layer, which serves as the nanowire gate array to define QDs along the underlying SiNW. Note that the titanium NWs over the source and drain leads are not expected to affect the transport properties of the device: the metallic contacts do not respond to a gate voltage. The number of SNAP top gate electrodes across the underlying Si NW (and hence the number of QDs in series) is varied from device to device (3 to ~10) and controlled by the source-drain length, as SNAP wires of the same pitch (33 nm) are always used to define the top gate electrodes. All gate electrodes are shorted to a larger contact. Measurements are done at liquid-helium temperature with standard lock-in technique at low frequency.

Supplementary Figures

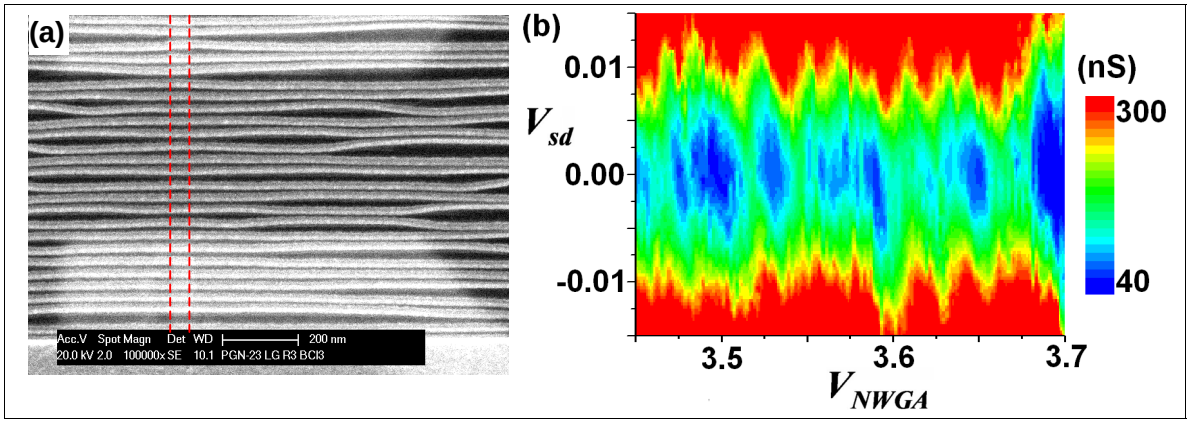

Figure S1. (a) Scanning electron micrograph of a device with an e-beam defined ~40 nm wide underlying SiNW and very little irregularity within the structure of the NWGA, especially where it covers the SiNW. The contour of the underlying SiNW is highlighted with red dashed lines. Scale bar: 200 nm. (b) $\partial I / \partial V_{sd}$ - V_{NWGA} - V_{sd} plot of the device recorded at 4.5 K.

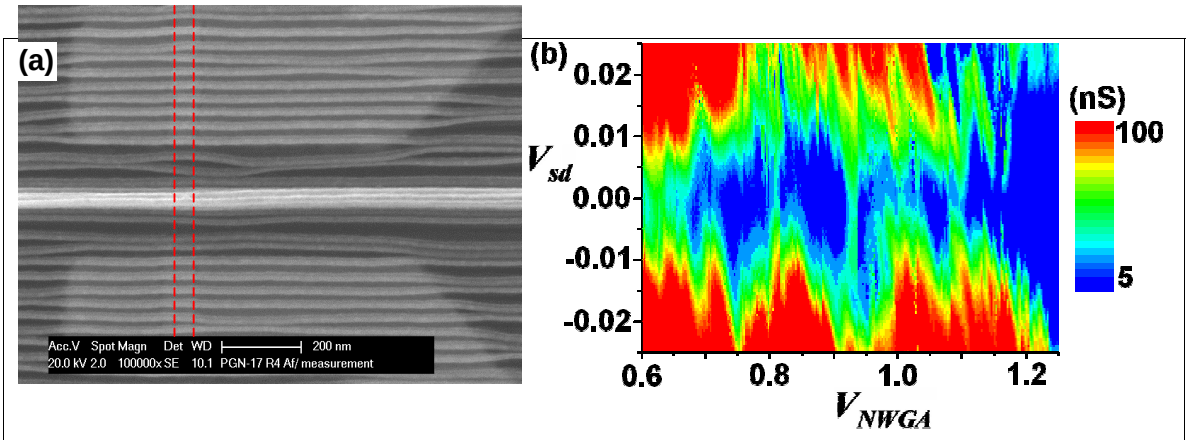

Figure S2. (a) Scanning electron micrograph of a device with an e-beam defined ~40 nm wide underlying SiNW and a highly irregular NWGA. The contour of the underlying Si NW is highlighted with red dashed lines. Scale bar: 200 nm. (b) $\partial I / \partial V_{sd}$ - V_{NWGA} - V_{sd} plot of the device recorded at 4.5 K.

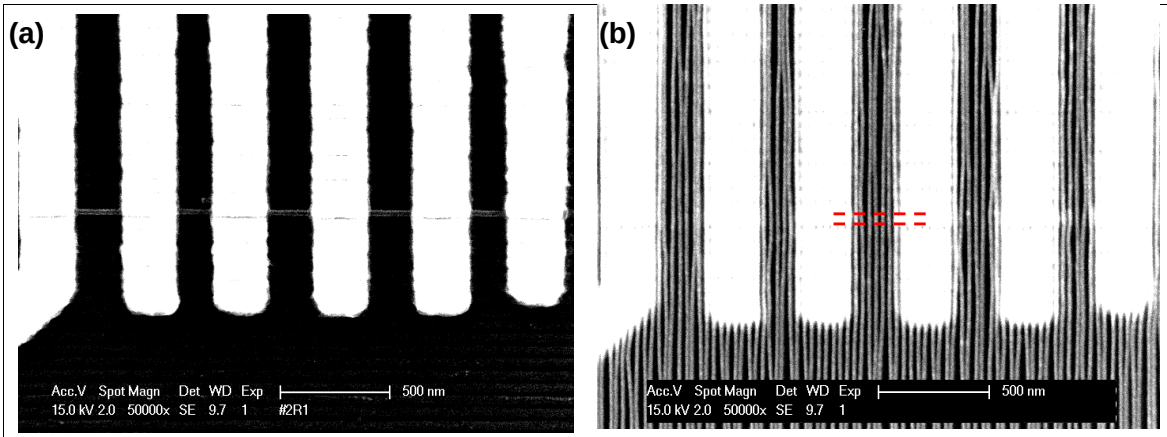

Figure S3. Scanning electron micrographs of a device with a SNAP-defined ~20 nm wide underlying Si NW. (a) Six Ti/Pt contacts made to one single ~20 nm wide SiNW sectioned out from a SNAP SiNW array. Scale bar: 500 nm. (b) The same structure after the dielectric layer and the NWGA are fabricated on top, forming five full devices, with each device corresponding to the structure shown in Fig 3(E). The data reported in Fig 6(b) corresponds to the device marked out with red dashed lines. Scale bar: 500 nm.

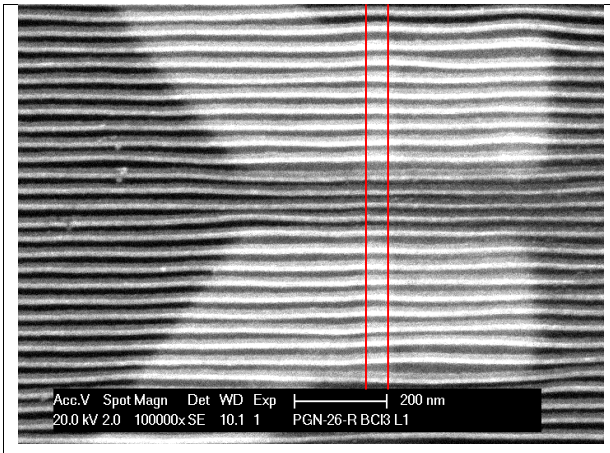

Figure S4. Scanning electron micrograph of a device with an e-beam defined 40 nm-wide underlying SiNW and three highly-regular top gate NWs. The contour of the underlying SiNW is highlighted with red dashed lines. Scale bar: 200 nm.

Reference for the Supplemental Online Materials:

Beckman, R. A., Johnston-Halperin, E., Melosh, N. A., Luo, Y., Green, J. E. and Heath, J. R. (2004). "Fabrication of conducting Si nanowire arrays." *J. Appl. Phys.* **96**(10): 5921-5923.

Melosh, N. A., Boukai, A., Diana, F., Gerardot, B., Badolato, A., Petroff, P. M. and Heath, J. R. (2003). "Ultrahigh-density nanowire lattices and circuits." *Science* **300**(5616): 112-115.

Wang, D., Sheriff, B. A. and Heath, J. R. (2006). "High Performance Silicon p-FETs from Ultra-High Density Nanowire Circuits." *Nano Lett.* **6**(6): 1096.