Nanomechanical Encoding Method Using Enhanced Thermal Concentration on a Metallic Nanobridge

Jeong Oen Lee, Kwang-Wook Choi, Seon-Jin Choi, Min-Ho Kang, Min-Ho Seo, Il-Doo Kim, Kyoungsik Yu, and Jun-Bo Yoon

ACS Nano, Just Accepted Manuscript • DOI: 10.1021/acsnano.7b01475 • Publication Date (Web): 14 Jul 2017

Downloaded from <http://pubs.acs.org> on July 17, 2017

Just Accepted

"Just Accepted" manuscripts have been peer-reviewed and accepted for publication. They are posted online prior to technical editing, formatting for publication and author proofing. The American Chemical Society provides "Just Accepted" as a free service to the research community to expedite the dissemination of scientific material as soon as possible after acceptance. "Just Accepted" manuscripts appear in full in PDF format accompanied by an HTML abstract. "Just Accepted" manuscripts have been fully peer reviewed, but should not be considered the official version of record. They are accessible to all readers and citable by the Digital Object Identifier (DOI®). "Just Accepted" is an optional service offered to authors. Therefore, the "Just Accepted" Web site may not include all articles that will be published in the journal. After a manuscript is technically edited and formatted, it will be removed from the "Just Accepted" Web site and published as an ASAP article. Note that technical editing may introduce minor changes to the manuscript text and/or graphics which could affect content, and all legal disclaimers and ethical guidelines that apply to the journal pertain. ACS cannot be held responsible for errors or consequences arising from the use of information contained in these "Just Accepted" manuscripts.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

Nanomechanical Encoding Method Using Enhanced Thermal Concentration on a Metallic Nanobridge

*Jeong Oen Lee¹†, Kwang-Wook Choi¹, Seon-Jin Choi², Min-Ho Kang³, Min-Ho Seo¹,
Il-Doo Kim², Kyoungsik Yu¹, and Jun-Bo Yoon¹**

¹ Department of Electrical Engineering, Korea Advanced Institute of Science and Technology
(KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 34141, Republic of Korea

² Department of Materials Science and Engineering, Korea Advanced Institute of Science and
Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 34141, Republic of Korea

³ National NanoFab Center (NNFC), 291 Daehak-ro, Yuseong-gu, Daejeon, 34141, Republic of
Korea

*Correspondence to: jbyoon@kaist.ac.kr
† Present address: Department of Electrical Engineering, California Institute of Technology,
Pasadena, CA 91125, USA.

ABSTRACT

We present a fast, energy-efficient nano-thermomechanical encoding scheme for digital information storage and retrieval. Digital encoding processes are conducted by the bistable electrothermal actuation of a scalable nanobridge device. The electrothermal energy is highly concentrated by enhanced electron/phonon scattering and heat insulation in a sub-100 nm metallic layer. The efficient conversion of electrothermal energy into mechanical strain allows digital switching and programming processes within 60 nanoseconds at 0.75 volts with a programming energy of only 54 picojoules. Furthermore, this encoding scheme together with the thermally robust design enables data-retention at temperatures up to 400 °C. These results suggest that the proposed nano-thermomechanical encoding method could contribute to low-power electronics and robust information storage/retrieval systems.

KEYWORDS

Nanoelectromechanical System (NEMS), nanomechanical encoding, non-volatile memory, high temperature, low-voltage electrothermal actuation, Joule heating, Wiedemann-Franz law

The development of micro- and nano-electromechanical systems^{1,2} typically relies on an electromechanical transducer, which is the core component for the conversion of electrical energy into mechanical energy. The electrothermal transducer has been one of the popularly used manipulating techniques in microelectromechanical systems (MEMS)³⁻⁵ and in nanoelectromechanical systems (NEMS), including nanomechanical resonators.⁶⁻⁸ However, its high power consumption is regarded as a considerable drawback:⁹ the generated thermal energy can easily escape to the thermal sink due to the high thermal conductivity of the resistive matter. This makes such devices impractical for use in various integrated-circuit (IC) applications, whereas piezoelectric¹⁰ or electrostatic actuators¹¹⁻¹⁴ have been relatively well established in emerging NEMS approaches for IC applications¹⁵ emphasizing their great potential for low voltage operation^{10,16} and low power consumption.¹⁷⁻²⁰

With nanofabrication technologies pushing deep into the sub-micrometer size regime, it has been found that the thermal properties of nanoscale structures are different from macro- and microscale systems. For instance, compared to bulk thermal conductivity values at room temperature, the thermal conductivities of nanowires are lower;²¹ the theoretical explanation of this interesting phenomenon is generally understood to be due to the scattering of electrons and phonons at surfaces, and by grain boundaries.²² A similar concept has commonly been invoked in many thermoelectric devices^{23,24} to achieve efficient thermal concentration by reducing the thermal-loss mechanisms.²⁵ However, it has not been established whether the enhanced thermal properties in nanoscale systems can be incorporated into electro-thermo-mechanical transducers or emerging nanomechanical devices for IC applications.¹⁵ If the enhanced thermal concentration can be achieved with low-power dissipation and somehow causes permanent mechanical deformation of nanostructures, then it is possible to suggest an efficient

1
2
3 nanomechanical encoding scheme similar to the operation of one-time programmable (OTP)
4
5 devices.
6
7

8
9 In practice, semiconductor one-time programmable (OTP) memories (e.g. anti-fuse and fuse)
10
11 have been widely used in radio-frequency identification (RFID) tags²⁶ and field-programmable
12
13 gate array (FPGA)²⁷ applications because they provide the simplest device architecture,
14
15 enabling low-cost fabrication,²⁸ whereas re-programmed memory technologies require
16
17 sophisticated device architecture and complex fabrication.^{29,30} The most commonly used OTP
18
19 architecture is an anti-fuse³¹ memory device that relies on the breakdown of metal-insulator-
20
21 metal or diode structures. The main drawback is, however, high leakage power³² resulting from
22
23 inherent tunneling current in semiconductor systems. Moreover, its high programming energy,
24
25 low on/off ratio, operating temperature, and high readout voltage need to be improved to
26
27 expand its applications.
28
29
30
31

32
33 Here we describe the development of a nanomechanical encoding method using enhanced
34
35 thermal concentration technique that addresses many of the challenges above. We combine a
36
37 nanomechanical metallic transducer and its electrothermal interaction, which provides
38
39 enhanced electro-thermo-mechanical effects. This enhancement enabled us to highly
40
41 concentrate the thermal energy on a scalable nanomechanical structure while minimizing power
42
43 consumption. The resulting enhanced temperature and corresponding strain yielded a robust
44
45 electromechanical contact that can program and store digital information. As a result, we
46
47 present an energy-efficient nanomechanical encoding technique that is thermally robust
48
49 (400°C) while being accessible at fast speed (60 ns), low bias voltage (sub-1-V), and low
50
51 power consumption (54 pJ). In this study, we investigated a theoretical model of electro-
52
53 thermo-mechanical actuation and demonstrated that the reliable and robust electrical properties
54
55
56
57
58
59
60

of the device can be attributed to the intimate coupling between mechanical actuation and the engineered thermal properties of nanostructures.

RESULTS AND DISCUSSION

Figure 1a shows a scanning electron microscope (SEM) image of the fabricated device. The device employs a cross-point architecture,^{33,34} which has a scalability advantage in terms of storage density. The fixed-fixed beam structure has dimensions of 1.25 μm (length) by 200 nm (width) by 40 nm (thickness), and tungsten, which has an extremely high melting point (3370 $^{\circ}\text{C}$), is used as a structural material. We fabricated the device on an 8-inch silicon wafer using a well-established IC manufacturing process to permit facile systematic integration with standard electronics. As fabricated, the current path from the suspended electrode to the bottom electrode is completely disconnected because of the air-gap separation of over 20 nm. Unless mechanical contact is made, no current flow can be observed between the two electrodes (digital “0”, **Fig. 1b**). However, when voltage is applied across the ends of the suspended electrode, the corresponding resistive (Joule) heating begins to induce a temperature increase, which results in mechanical buckling that establishes the current path from the suspended electrode to the bottom electrode (digital “1”, **Fig. 1c**). A lateral schematic view of the device architecture and the simplified fabrication process are shown in **Fig. 1d** and **e** (see the **Supporting Information** for details of the fabrication process).

For reliable electrical operation, it is important that the buckling should always be directed downward. To ensure consistent downward buckling, we engineered an intrinsic residual stress on the tungsten layer to generate a slightly downward deformation in the suspended nanostructure to function as a buckling trigger. In principle, a residual compressive stress and a positive stress gradient in the fixed-fixed beam structure are responsible for initiating the

downward buckling. Because the width of the suspended electrode is at least five times greater than its thickness, a displacement in the lateral direction can reasonably be ignored. We used the sputtering method to obtain suitable deposition conditions in which the stress was independently evaluated using a wafer-curvature method.³⁵ This technique is based on Stoney's equation,³⁶ which calculates the thin film stress by measuring the change in the curvature radius of the substrate after deposition of the metal film. In practice, the residual compressive stress (2.5 GPa) of the tungsten film induces an initial downward deformation of the structure of approximately 35 nm. Because environmental temperature variations can cause undesirable mechanical contact due to thermal expansion, the device is designed to have a sufficiently large air gap of more than 20 nm (the thickness of the total sacrificial layer is greater than 55 nm) and a sufficiently high spring constant (86 Nm^{-1}) to ensure high-temperature stability. In addition, this enhancement of the mechanical reliability of the device is expected to decrease the risk of stiction failure, which is often induced by competition between the restoring force and the capillary force while removing the sacrificial layer. As a result of developing a stable fabrication process with a high yield, even without applying a critical point drying process we were able to perform a statistical analysis of hundreds of devices.

The typical current-voltage characteristics of a fabricated device are shown in **Fig. 2a**. To insure consistent testing conditions, all measurements were performed in a vacuum chamber ($<3 \text{ mTorr}$) with an electrical shielding. The operation modes can be classified into two different types according to the electrical operation: (1) a one-time-programmable memory mode (the dashed black line) and (2) the traditional reversible switching mode (the solid red line). I_{RD} denotes the read current (crossover current) flowing from the suspended electrode to the bottom electrode *via* the contact interface, and V_g denotes the gate voltage that is applied

across two ends of the suspended electrode. In the sub-threshold regime of $0 < V_g < 0.75$ V, the crossover current (I_{RD}) is identical to the noise reference of the open-pad measurement ($10^{-15} - 10^{-13}$ A), whereas when V_g is raised above a threshold voltage V_{TH} of 0.75 V, an abrupt current jump (the sub-threshold slope $SS = 1.43$ mVdec⁻¹) is observed, which indicates that mechanical contact has been made between the suspended electrode and the bottom electrode. Once the crossover current begins to flow from the top electrode to the bottom electrode, the magnitude of the crossover current plays a key role in determining the operation mode. The current flow essentially increases the local temperature at the physical contact point by Joule heating, allowing for the rearrangement of atoms on the hot interface. The local heating and the electric current can promote the material migration and consequent bonding process. While previous nanowelding techniques used laser heating³⁷ or thermal heating³⁸ throughout a large substrate to create massive interconnection networks, our system can manipulate individual interconnections on integrated devices by controlling bias conditions. For example, if a sufficiently high crossover current I_{RD} is allowed (~ 1 mA) to flow through the contacting point, the top and bottom electrodes are bonded together coalescing crystallized tungsten at the interface. If the adhesion force caused by strong atomic binding dominates the restoring spring force of the nanobridge structure, the device does not return to the initial state even after the electrical bias is removed. Consequently, the device operates in memory mode (the dashed black line) and traces a clear hysteresis curve that represents one-time-programmable non-volatile memory behavior. In contrast, if the external current compliance is approximately 10 nA or below, the device exhibits the reversible switching operation (the solid red line) without forming a permanent contact. By comparing these two modes in the same device and separately visualizing the mechanical actuation in the switching operation, we could infer that the

mechanical actuation and nanowelding process occurred consecutively in a single encoding process.

To understand the underlying thermal interaction in the nano-thermomechanical actuation, we investigated the relation between the resistive (Joule) heating process and the thermal expansion based on a simplified analytical model and a finite-element-method (FEM) simulation. Importantly, if merely the bulk properties of the material are adopted, a significant deviation arises between the theoretical analysis and the experimental result. Because the thickness of our nanostructure is in the mesoscopic range (1.5 – 100 nm), which is comparable to the electron mean free path, the size-dependent electron-phonon effect should be considered; this effect gives rise to a decrease in thermal conductivity. The thermal conductivity κ and the electrical conductivity σ are coupled *via* the Wiedemann-Franz law $\kappa / \sigma = LT$, where L is the Lorenz number and T is the absolute temperature.³⁹ The electrical conductivity ($3.9 \times 10^6 \text{ Sm}^{-1}$) was determined from experimental measurements (**see the Supporting Information**), and the corresponding thermal conductivity was calculated using the Wiedemann-Franz law with the inclusion of a phonon-corrected Lorenz number for tungsten film.⁴⁰ The reduced thermal conductivity ($26 \text{ Wm}^{-1}\text{K}^{-1}$) is approximately one-seventh of the conductivity of the typical bulk material ($175 \text{ Wm}^{-1}\text{K}^{-1}$) and can be understood as an effect of the scattering of electrons and phonons at the surfaces and grain boundaries of a metallic thin film.⁴¹

Using the empirical thermal conductivity of our nanoscale structure, we developed a one dimensional (1-D) theoretical model which predicts the mechanical displacement of a suspended nanobeam as a function of electrical input power. The model estimates the downward displacement of a fixed-fixed beam structure by combining a resistive heating model

with reduced thermal conductivity ($26 \text{ Wm}^{-1}\text{K}^{-1}$) and the temperature-voltage relationship; this results in the thermal expansion of the beam length (ΔL). The threshold voltage (V_{TH}) was defined as the vertical displacement that exceeds the height of the initial air gap. In this way, we obtained a simple analytical expression of the V_{TH} as a function of the dimensional parameters. A detailed description of the model derivation is given in the **Supporting Information**.

Our theoretical model, which accounts for the reduced thermal conductivity ($26 \text{ Wm}^{-1}\text{K}^{-1}$), was well matched to the experimental data points. In **Fig. 2b**, the V_{TH} is plotted as a function of the beam length (L) and the beam width (W). The dashed blue line represents the theoretical prediction when the W is 300 nm, and the solid red line represents the predicted value when the W is 200 nm. This characteristic implies that the V_{TH} can be tailored by determining the dimensions of the nanostructure, and enables multi-threshold voltage engineering for a given fabrication process.

Moreover, ultra-low-voltage operation is also achievable. In the experimental results, V_{TH} were measured between 1~1.25 V when the width of the suspended beam was 300 nm, and it exhibited a V_{TH} of around 0.6 V ~ 0.75 V when the width of the suspended beam was 200 nm. As the model predicted, our nano thermomechanical encoding method enabled sub-1-volt operation. This performance metric is comparable to state-of-the-art techniques such as those reported by Usama *et al.*,¹⁰ or in our previous work.⁴² In addition, the structural design and fabrication process is less complicated than previous methods.

After the programing process, the actual thermal expansion and mechanical deformation of the suspended beam was investigated using cross-sectional transmission-electron-microscopy (TEM) images (**Fig. 2c**). Because of the residual stress in the tungsten film, the suspended

beam had an initial downward bend, even in the OFF-state. This true curvature of the beam was included in the three-dimensional (3-D) FEM model. The 3-D simulation reasonably predicted the temperature profile across the nanostructure, and the displacement, by taking into account parasitic components such as the electrical leads and peripheral electrodes connected to both ends of the suspended nanobeam.

Fig. 3a presents the temperature distribution at the applied voltage of 0.75 V, and the beam profile as a function of voltage. The temperature of a local suspended region can be increased to 1100 K at an applied voltage of $V_g = 0.75$ V with a current density of 3.75×10^7 Acm⁻². Then, the corresponding downward displacement is 23 nm. These values closely match our experimental results for the same bias condition, and are consistent with our 1-D theoretical model (see the Supporting Information, Fig. S4).

Using this simulation model, we examined the influence of the different thermal conductivities on the actuation characteristics, and the equilibrium temperature for the given input power. **Figure 3b** shows the relationship between the beam displacement and the input electrical power. Our thermomechanical system with the enhanced thermal property ($\sigma = 26$ Wm⁻¹K⁻¹) required only 0.18 mW to achieve 20 nm of displacement, whereas the device with the bulk thermal property ($\sigma = 174$ Wm⁻¹K⁻¹) required 0.50 mW to reach the same displacement. This implies that the enhanced thermal property of the nanostructure enables the efficient conversion of electrical power to thermal expansion. The reduced thermal conductivity in the nanoscale metallic structures causes heat accumulation due to thermal isolation, resulting in efficient temperature increase.

In **Fig. 3c**, the suspended nanostructure with a thermal conductivity of 26 Wm⁻¹K⁻¹ (the solid

red line) exhibited rapid temperature increases as a function of input power. In the temperature analysis, we found that the thermal energy generated by resistive heating cannot easily escape to the thermal sink because of the low thermal conductivity of the conduction path; in the suspended structure in particular, the conductive heat loss through the anchoring pad accounted for the majority of the total energy loss. Consequently, this excellent thermal isolation means that the nanomechanical device can reach its critical temperature with relatively low electric energy; in other words, the mechanical structure can be efficiently driven under the given electrical conditions.

Next, we investigated the thermal interaction at the contact interface in the high-crossover-current case. Under typical programing conditions ($V_{TH} < V_g < 1.5$ V, $I_{RD} = 1$ mA), the suspended top electrode and the bottom electrode form a permanent contact which represents the programmed state of the nano-thermomechanical encoding scheme. The SEM image in **Fig. 4a** shows the overall features of the programmed device after the nano-thermomechanical encoding process. To conduct atomic-scale characterization of the contacting interface, a cross-sectional specimen of the programmed device was cut out using focused ion beam (FIB) machining, and examined by TEM (**Fig. 4b**). Although the contact interface appears to have a separate structure in the low magnification TEM image, it is actually filled with low-density tungsten at the critical contact spot, as indicated in the zoomed-in image (**Fig. 4c** and **Fig. S5**).

Interestingly, the tungsten atoms at the critical contact spot exhibited a crystalline structure that was different from its native structure (**Fig. 4d**). As fabricated, our tungsten layer had a randomly oriented polycrystalline structure with weak crystallinity, whereas in the programmed state, we observed that the crystalline structure in a local region was reoriented along a

1
2
3 preferred crystal orientation of [210] (**Fig. 4e**), which was clearly distinguishable from a
4
5 randomly oriented crystal structure of native tungsten layer found in the suspended region or
6
7 the bottom electrode of the same device (**Fig. S6**). By investigating a few samples, we found
8
9 that approximately 20% of the bottom electrode was reoriented in a preferred oriented crystal
10
11 direction while forming a crystalline tungsten column with a diameter of 50 – 100 nm. This
12
13 crystalline reorientation, which was observed across the entire contact interface, led us to
14
15 believe that in this device architecture, the thermal and electrical energy flowed through a large
16
17 effective contact area rather than atomic-scale asperities.
18
19
20
21

22
23 The highly stable and reproducible I - V characteristics observed in the electrical
24
25 measurements can be also explained by the uniform contact interface indicated in the atomic-
26
27 scale TEM analysis. **Figure 5a** presents the log I - V plots derived from the programmed state
28
29 and un-programmed state of 10 different devices, which were fabricated with an identical
30
31 layout. The crowded data points of the programmed state indicate the consistency of the
32
33 thermomechanical programming process. Although the programmed states were generated by a
34
35 mechanical contact, they exhibited nearly identical electrical features from device to device. In
36
37 view of this fact, we believe that the concentrated thermal energy is responsible for the
38
39 crystalline arrangement at the critical contact point and leads to a reliable programming process
40
41 with consistent electrical contact properties. If the current and thermal energy flowed through
42
43 many distributed asperities without crystalline arrangement, the electrical characteristics should
44
45 dynamically vary depending on the single dominant atomic contact and present large variation
46
47 in the readout current I_{RD} .
48
49
50
51
52
53

54
55 As mentioned above, our nanomechanical device can be programmed by applying a single
56
57
58
59
60

voltage pulse to the gate while holding the other electrodes at 0 V (or ground). The read current I_{RD} is measured afterward to ensure that the device has indeed responded to a certain pulse width and been programmed. For example, the permanent contact was not activated with a pulse width below 50 ns, whereas the device was encoded by pulse widths larger than 60 ns, which indicates the minimum programming time (**Fig. 5b**). The minimum programming time of our nano-thermomechanical encoding process is comparable to the programming speed of conventional electronic data-storage systems. **Table 1** briefly summarizes performance factors of various non-volatile memories and one-time programmable memories along with our work. Although the programming process in our system is based on resistive thermal actuation, the required energy is only 54 picojoules (pJ) per bit. The energy (E) was calculated from the electric energy and power equation⁴³ $E=P\Delta t$, where the programming power (P) was the product of the driving current ($I=1.2\text{mA}$) and the pulse voltage ($V=0.75\text{V}$). In this condition, the required programming pulse width (Δt) was 60 nanoseconds (ns).

To study high temperature properties, we verified that the electrical state of the programmed/un-programmed devices is consistently preserved even after baking at 400 °C in N_2 atmosphere. The thermal stability of the mechanically programmed digital information is illustrated in **Fig. 6a**. In the 400 °C condition, we demonstrated that 100% (60/60) of the devices could retain their initial states without any electrical degradation. Although our theoretical model suggests that the maximum temperature can be extended to 700°C (see the **Supporting Information, Fig. S7**), 26.7% (19/71) of the devices failed to retain the expected data at 500°C. It may indicate that fabrication improvement and design optimization would be necessary in the further study.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

Nonetheless, these measurement results are meaningful in two respects: first, high-temperature data storage, which is an essential component of a high-temperature logic device, has been demonstrated; our method for overcoming the electronic limitations of this task suggests that a nanomechanical approach may offer a viable solution for surpassing the current temperature limits of electronic data storage. Second, the excellent electrical performance achieved by concentrating the electrothermal energy leads us to believe that the critical disadvantage of the thermal actuation method, namely, its extremely high energy consumption in microsystems, can be effectively compensated when the system is scaled down, thereby enabling efficient and reliable actuation in nanomechanical systems.

CONCLUSIONS

The present technique and the results of its experimental investigation provide prospects for implementing a robust, high-temperature, and fast operating nanomechanical system for applications in digital data storage and encoding. In combination with an efficient energy-concentration method based on the scattering of electrons and phonons in nanostructures, we present a nanoscale electrothermal actuator that is able to operate with low-voltage and low-power specifications that can be conveniently incorporated into conventional integrated-circuit technologies. To establish the feasibility of this technology, we demonstrated the operation of a nanomechanical data-storage device at temperatures of up to 400 °C, which is not accessible to conventional semiconductor-based solid-state electronics. In this regard, the high robustness and co-integration ability of the proposed method offers a promising pathway toward realizing a complex information processing system that is suitable for operation under extremely harsh conditions, such as those found in aerospace, geothermal and automotive applications.

METHODS

Electrical measurement. The low noise *I-V* measurements were performed on a shielded vacuum probe station (MSTECH, Vacuum Chamber M6VC) with a semiconductor parameter analyzer (Agilent, 4156C). Three-terminal tungsten electrodes (100 μm × 100 μm) were probed by bending-type gold tips (MSTECH, M5BG; leakage ~10 fA). In order to eliminate the current noise (pad-to-pad leakage current) induced from water condensation on a sample surface, all devices were kept in a vacuum container (~10 mTorr) before measurements. The programming time and cyclic characteristic were measured with a semiconductor device parameter analyzer (Agilent, B1500A) using script control.

High-resolution electron microscopy. For the TEM sample preparation in Fig.3, we first electrically programmed a device, and amorphous carbon was subsequently coated (Gatan, 682 PECS) to clearly distinguish the device feature from the platinum layers which serve as a protecting mask during the ion-milling process. The specific section of interest that is adjacent to the critical contact spot was thinned by focused ion beam milling (Hitach, FB-2100) and lifted-out (FEI, Nova-200) to form a TEM lamellae. The TEM investigation was performed on a high resolution electron microscope (JEOL, JEM-3011 HR). The images were analyzed using a commercial software (Gatan, DigitalMicrograph).

ToC IMAGE

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at

DOI:

Fabrication Process; Resistivity Extraction; A One-dimensional (1-D) simplified Model; Three-dimensional (3-D) Finite-element-method (FEM) Simulation; Electrical Measurement Method; High-resolution magnified transmission-electron-microscopy images (PDF)

AUTHOR INFORMATION

Corresponding Author

*E-mail : jbyoon@kaist.ac.kr

Present Address

† Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125, USA.

Author Contributions

J.O.L. conceived the idea and planned the experiments. M.-H.K. fabricated the device. J.O.L. and K.-W.C. performed the measurements and the model analysis. J.O.L., S.-J.C. and M.-H.S. participated in TEM measurements. J.O.L., S.-J.C. and I.-D.K. performed the TEM analysis. J.-B.Y. inspired the research with guidance and participated in data analysis with K.Y. The manuscript was written by J.O.L. with comment and assistant from I.-D.K., K.Y. and J.-B.Y. All authors discussed the results and commented on the manuscript.

ACKNOWLEDGEMENTS

This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as “Global Frontier Project” under Grant CISS-2012054187 and by the National Research Foundation of Korea (NRF) under the Ministry of Education (NRF-2013R1A6A3A03026384). We acknowledge the helpful discussions we had with Hyungsoon Choi and Heung-Sun Sim, and the support from Hyuck Choo.

REFERENCES

1. Rebeiz, G. M. *RF MEMS: Theory, Design, and Technology*; John Wiley & Sons, 2004.
2. Ekinici, K. L.; Roukes, M. L. Nanoelectromechanical Systems. *Rev. Sci. Instrum.* **2005**, 76, 061101.
3. Yan, D.; Khajepour, A.; Mansour, R. Design and Modeling of a MEMS Bidirectional Vertical Thermal Actuator. *J. Micromech. Microeng.* **2004**, 14, 841-850.
4. Zhu, Y.; Corigliano, A.; Espinosa, H. D. A Thermal Actuator for Nanoscale *in situ* Microscopy Testing: Design and Characterization. *J. Micromech. Microeng.* **2006**, 16, 242-253.
5. Jain, A.; Qu, H.; Todd, S.; Xie, H. A Thermal Bimorph Micromirror with Large Bi-Directional and Vertical Actuation. *Sens. Actuators, A* **2005**, 122, 9-15.
6. Bargatin, I.; Kozinsky, I.; Roukes, M. L. Efficient Electrothermal Actuation of Multiple Modes of High-Frequency Nanoelectromechanical Resonators. *Appl. Phys. Lett.* **2007**, 90, 093116.
7. Rahafrooz, A.; Pourkamali, S. High-Frequency Thermally Actuated Electromechanical Resonators with Piezoresistive Readout. *IEEE Trans. Electron Dev.* **2011**, 58, 1205-1214.
8. Jun, S. C.; Huang, X. M. H.; Manolidis, M.; Zorman, C. A.; Mehregany, M.; Hone, J. Electrothermal Tuning of Al-SiC Nanomechanical Resonators. *Nanotechnology* **2006**, 17, 1506-1511.

9. Ekinici, K. L. Electromechanical Transducers at the Nanoscale: Actuation and Sensing of Motion in Nanoelectromechanical Systems (NEMS). *Small* **2005**, 1, 786-797.

10. Usama, Z.; Gianluca, P. Sub-1-Volt Piezoelectric Nanoelectromechanical Relays with Millivolt Switching Capability. *IEEE Electron Dev. Lett.* **2014**, 35, 669-671.

11. Jang, W. W.; Lee, J. O.; Yoon, J.-B.; Kim, M.-S.; Lee, J.-M.; Kim, S.-M.; Cho, K.-H.; Kim, D.-W.; Park, D.; Lee, W.-S. Fabrication and Characterization of a Nanoelectromechanical Switch with 15-nm-Thick Suspension Air Gap. *Appl. Phys. Lett.* **2008**, 92, 103110.

12. Jang, J. E.; Cha, S. N.; Choi, Y. J.; Kang, D. J.; Butler, T. P.; Hasko, D. G.; Jung, J. E.; Kim, J. M.; Amaratunga, G. A. Nanoscale Memory Cell Based on a Nanoelectromechanical Switched Capacitor. *Nat. Nanotechnol.* **2008**, 3, 26-30.

13. Shavezipur, M.; Harrison, K.; Lee, W. S.; Mitra, S.; Wong, H. S. P.; Howe, R. T. Partitioning Electrostatic and Mechanical Domains in Nanoelectromechanical Relays. *IEEE J. Microelectromech. Syst.* **2014**, 24, 592-598.

14. Chong, S.; Lee, B.; Mitra, S.; Howe, R. T.; Wong, H. S. P. Integration of Nanoelectromechanical Relays with Silicon nMOS. *IEEE Trans. Electron Dev.* **2012**, 59, 255-258.

15. Loh, O. Y.; Espinosa, H. D. Nanoelectromechanical Contact Switches. *Nat. Nanotechnol.* **2012**, 7, 283-295.

16. Feng, X. L.; Matheny, M. H.; Zorman, C. A.; Mehregany, M.; Roukes, M. L. Low Voltage Nanoelectromechanical Switches Based on Silicon Carbide Nanowires. *Nano Lett.* **2010**, 10, 2891-2896.

17. Kam, H.; Liu, T.-J. K.; Stojanović, V.; Marković, D.; Alon, E. Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic. *IEEE Trans. Electron Dev.* **2011**, 58, 236-250.
18. Song, Y. H.; Ahn, S. J.; Kim, M. W.; Lee, J. O.; Hwang, C. S.; Pi, J. E.; Ko, S. D.; Choi, K. W.; Park, S. H.; Yoon, J. B. High-performance Hybrid Complementary Logic Inverter Through Monolithic Integration of a MEMS Switch and an Oxide TFT. *Small* **2015**, 11, 1390-1395.
19. Kam, H.; Lee, D. T.; Howe, R. T.; King, T.-J. A New Nano-Electro-Mechanical Field Effect Transistor (NEMFET) Design for Low-Power Electronics. *IEDM Tech. Dig.* **2005**, 463-466.
20. Jeon, J.; Pott, V.; Kam, H.; Nathanael, R.; Alon, E.; King Liu, T.-J. Seesaw Relay Logic and Memory Circuits. *IEEE J. Microelectromech. Syst.* **2010**, 19, 1012-1014.
21. Völklein, F.; Reith, H.; Cornelius, T. W.; Rauber, M.; Neumann, R. The Experimental Investigation of Thermal Conductivity and the Wiedemann–Franz Law for Single Metallic Nanowires. *Nanotechnology* **2009**, 20, 325706.
22. Cahill, D. G.; Braun, P. V.; Chen, G.; Clarke, D. R.; Fan, S.; Goodson, K. E.; Koblinski, P.; King, W. P.; Mahan, G. D.; Majumdar, A.; Maris, H. J.; Phillpot, S. R.; Pop, E.; Shi, L. Nanoscale Thermal Transport. II. 2003–2012. *Appl. Phys. Rev.* **2014**, 1, 011305.
23. Hochbaum, A. I.; Chen, R.; Delgado, R. D.; Liang, W.; Garnett, E. C.; Najarian, M.; Majumdar, A.; Yang, P. Enhanced Thermoelectric Performance of Rough Silicon Nanowires. *Nature* **2008**, 451, 163-167.

24. Zhang, G.; Wang, W.; Li, X. Enhanced Thermoelectric Properties of Core/Shell Heterostructure Nanowire Composites. *Adv. Mater.* **2008**, 20, 3654-3656.
25. Bell, L. E. Cooling, Heating, Generating Power, and Recovering Waste Heat with Thermoelectric Systems. *Science* **2008**, 321, 1457-1461.
26. Lee, M. C.; Barsatan, R.; Chan, M. OTP Memory for Low Cost Passive RFID Tags. *EDSSC, Conference on IEEE* **2007**, 633-636.
27. Rodriguez-Andina, J. J.; Moure, M. J.; Valdes, M. D. Features, Design Tools, and Application Domains of FPGAs. *IEEE Trans. Ind. Electron.* **2007**, 54, 1810-1823.
28. Monmasson, E.; Cirstea, M. N. FPGA Design Methodology for Industrial Control Systems – A Review. *IEEE Trans. Ind. Electron.* **2007**, 54, 1824-1842.
29. Annunziata, R.; Zuliani, P.; Borghi, M.; Sandre, G. D.; Scotti, L.; Prelini, C.; Tosi, M.; Tortorelli, I.; Pellizzer, F. Phase Change Memory Technology for Embedded Non Volatile Memory Applications for 90 nm and Beyond, *IEDM Tech. Dig.* **2009**, 200, 97–100.
30. Shum, D.; Tilke, A. T.; Pescini, L.; Stiftinger, M.; Kakoschke, R. Highly Scalable Flash Memory with Novel Deep Trench Isolation Embedded into High Performance CMOS for the 90nm Node & beyond, *IEDM Tech. Dig.* **2005**, 344-347.
31. Cha, H. K.; Yun, I.; Kim, J.; So, B. C.; Chun, K.; Nam, I.; Lee, K. A 32-KB Standard CMOS Antifuse One-time Programmable ROM Embedded in a 16-bit Microcontroller. *IEEE J. Solid-State Circuits* **2006**, 41, 2115-2124.

32. Ng, K. P.; Lee, M. C.; Kwong, K. C.; Chan, M. Diode Based Gate Oxide Anti-Fuse One Time Programmable Memory Array in Standard CMOS Process. *EDSSC, Conference on IEEE* **2009**, 457-460.

33. Rueckes, T.; Kim, K.; Joselevich, E.; Tseng, G. Y.; Cheung, C.-L.; Lieber, C. M. Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing. *Science* **2000**, 289, 94-97.

34. Davidson, B. D.; Seghete, D.; George, S. M.; Bright, V. M. ALD Tungsten NEMS Switches and Tunneling Devices. *Sens. Actuators, B* **2001**, 166, 269-276.

35. Watanabe, M.; Mumm, D. R.; Chiras, S.; Evans, A. G. Measurement of the Residual Stress in a Pt–Aluminide Bond Coat. *Scripta Materialia* **2002**, 46, 67-70.

36. Ohring, M. *Materials Science of Thin Films*; Elsevier, 2001.

37. Han, S.; Hong, S.; Ham, J.; Yeo, J.; Lee, J.; Kang, B.; Lee, P.; Kwon, J.; Lee, S. S.; Yang, M. Y.; Ko, S. H. Fast Plasmonic Laser Nanowelding for a Cu-Nanowire Percolation Network for Flexible Transparent Conductors and Stretchable Electronics. *Adv. Mater.* **2014**, 26, 5808-5814.

38. Yao, Y.; Fu, K. K.; Zhu, S.; Dai, J.; Wang, Y.; Pastel, G.; Chen, Y.; Li, T.; Wang, C.; Li, T.; Hu, L. Carbon Welding by Ultrafast Joule Heating. *Nano Lett.* **2016**, 16, 7282-7289.

39. Graf, M. J.; Yip, S.-K.; Sauls, J. A.; Rainer, D. Electronic Thermal Conductivity and the Wiedemann-Franz Law for Unconventional Superconductors. *Phys. Rev. B* **1996**, 53, 15147-15161.

40. Stojanovic, N.; Maithripala, D. H. S.; Berg, J. M.; Holtz, M. Thermal Conductivity in Metallic Nanostructures at High Temperature: Electrons, Phonons, and the Wiedemann-Franz Law. *Phys. Rev. B* **2010**, 82, 075418.
41. Tritt, T. M. *Thermal Conductivity: Theory, Properties, and Applications*; Springer Science & Business Media, 2005.
42. Lee, J. O.; Song, Y. H.; Kim, M. W.; Kang, M. H.; Oh, J. S.; Yang, H. H.; Yoon, J. B. A Sub-1-Volt Nanoelectromechanical Switching Device. *Nat. Nanotechnol.* **2013**, 8, 36-40.
43. Nishi, Y. *Advances in Non-Volatile Memory and Storage Technology*; Elsevier, 2014.
44. Grupp, L. M.; Caulfield, A. M.; Coburn, J.; Swanson, S. Characterizing Flash Memory: Anomalies, Observations, and Applications. *Proc. Int. Symp. Microarchit.* **2009**, 24-33.
45. Song, Y. J.; Jeong, G.; Baek, I.-G.; Choi, J. What Lies Ahead for Resistance-Based Memory Technologies? *Computer* **2013**, 46, 30-36.
46. Zhao, C.; Zhao, C.; Taylor, S.; Chalker, P. Review on Non-Volatile Memory with High-k Dielectrics: Flash for Generation Beyond 32 nm. *Materials* **2014**, 7, 5117-5145.
47. Lee, S. H.; Park, H. C.; Kim, H. W.; Choi, M. R.; Lee, H. G.; Seo, J. W.; Kim, S. C.; Kim, S. G.; Hong, S. B.; Lee, S. Y.; Lee, J. U.; Kim, Y. S.; Kim, K. S.; Kim, J. I.; Lee, M. Y.; Shin, H. S.; Chae, S. J.; Song, J. H.; Yoon, H. S.; Oh, J. M. *et al.* Highly Productive PCRAM Technology Platform and Full Chip Operation: Based on 4F² (84nm pitch) Cell Scheme for 1 Gb and Beyond. *IEDM Tech. Dig.* **2011**, 3.3.1-3.3.4.

48. Wong, H.-S. P.; Ahn, C.; Cao, J.; Chen, H.-Y.; Eryilmaz, S. B.; Fong, S. W.; Incorvia, J. A.; Jiang, Z.; Li, H.; Neumann, C.; Okabe, K.; Qin, S.; Sohn, J.; Wu, Y.; Yu, S.; Zheng, X.; Stanford Memory Trends **2016**, <https://nano.stanford.edu/stanford-memory-trends>
49. Kim, I. S.; Cho, S. L.; Im, D. H.; Cho, E. H.; Kim, D. H.; Oh, G. H.; Ahn, D. H.; Park, S. O.; Nam, S. W.; Moon, J. T.; Chung, C. H. High Performance PRAM Cell Scalable to Sub-20nm Technology with Below $4F^2$ Cell Size, Extendable to DRAM Applications. *VLSI Technology, Symposium on IEEE* **2010**, 203-204.
50. Wong, H. S.; Salahuddin, S. Memory Leads the Way to Better Computing. *Nat. Nanotechnol.* **2015**, 10, 191-194.
51. Lacaita, A. L.; Redaelli, A. The Race of Phase Change Memories to Nanoscale Storage and Applications. *Microelectron. Eng.* **2013**, 109, 351-356.
52. Wouters, D. J.; Waser, R.; Wuttig, M. Phase-Change and Redox-based Resistive Switching Memories. *Proc. IEEE* **2015**, 103, 1274-1288.
53. Ebrard, E.; Allard, B.; Candelier, P.; Waltz, P. Review of Fuse and Antifuse Solutions for Advanced Standard CMOS Technologies. *Microelectr. J.* **2009**, 40, 1755-1765.
54. Kulkarni, S. H.; Pae, S.; Chen, Z.; Hafez, W.; Pedersen, B.; Rahman, A.; Tong, T.; Bhattacharya, U.; Jan, C.-H.; Zhang, K. A 32nm High-k and Metal-Gate Anti-Fuse Array Featuring a $1.01\mu\text{m}^2$ 1T1C Bit Cell. *VLSI Technology, Symposium on IEEE* **2012**, 79-80.
55. Tsai, Y.-H.; Chen, H.-M.; Chiu, H.-Y.; Shih, H.-S.; Lai, H.-C.; King, Y.-C.; Lin, C. J. 45nm Gateless Anti-Fuse Cell with CMOS Fully Compatible Process. *IEDM Tech. Dig.* **2007**, 95-98.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60

56. Hsiao, W. Y.; Peng, P. C.; Chang, T.-S.; Chih, Y.-D.; Tsai, W.-C.; Chang, M.-F.; Chien, T.-F.; King, Y.-C.; Lin, C.-J. A New High-Density Twin-Gate Isolation One-Time Programmable Memory Cell in Pure 28-nm CMOS Logic Process. *IEEE Trans. Electron Dev.* **2015**, 62, 121-127.

57. Nilsson, H.-E.; Andersson, H. A.; Manuilskiy, A.; Unander, T.; Hammarling, K.; Siden, J.; Gulliksson, M. Printed Write Once and Read Many Sensor Memories in Smart Packaging Applications. *IEEE Sens. J.* **2011**, 11, 1759-1767.

58. Onlaor, K.; Thiawong, T.; Tunhoo, B. Electrical Switching and Conduction Mechanisms of Nonvolatile Write-Once-Read-Many-Times Memory Devices with ZnO Nanoparticles Embedded in Polyvinylpyrrolidone. *Org. Electron.* **2014**, 15, 1254-1262.

59. Leppaniemi, J.; Mattila, T.; Eiroma, K.; Miyakawa, T.; Murata, K.; Alastalo, A. Printed Low-Voltage Fuse Memory on Paper. *IEEE Electron Dev. Lett.* **2014**, 35, 354-356.

60. Singh, P.; Li, C. G.; Pitchappa, P.; Lee, C. Tantalum-Nitride Antifuse Electromechanical OTP for Embedded Memory Applications. *IEEE Electron Dev. Lett.* **2013**, 34, 987-989.

Table 1. Performance comparison of non-volatile memories

	NAND Flash ⁴³⁻⁴⁶	PCM ^{*47-52}	Anti-fuse OTP ^{**53-56}	WORM ^{***57-59}	Mechanical OTP ⁶⁰	This work
Principle	Floating gate	Phase change material	oxide breakdown	conductivity change, printable organic materials	mechanical encoding, electrostatic	mechanical encoding, electro-thermal
Programming Number	10 ⁵	10 ⁸	1	1	1	1
Programming Voltage (V)	15-20 V	4.6 V	4.5 V	3.2 V	6 V	0.75 V
Programming Power (W)	20-50 mW	1.2 mW	-	96 mW	6 mW	0.9 mW
Programming Time (sec)	20-200 μ s	50-100 ns	200 μ s	130 ms	700 ns	60 ns
Temperature	< 200 °C	< 200 °C	150 °C	120 °C		400 °C
Programming Energy (Joule)	100pJ -1 nJ	10-100 pJ	1.5 nJ	10 -15 mJ	4.2 nJ	54 pJ

* PCM: phase change memory

** OTP: one-time programmable memory

*** WORM: write-once read many-times memory, typically indicates one-time programmable memory built by organic material technologies

Figure 1. Nanomechanical device and operating principles. (a) An SEM image of the fabricated device. (b) As fabricated, electrical current cannot flow across the air gap between the top electrode and the bottom electrode. This configuration corresponds to the un-programmed ("0") state. (c) Thermal expansion induced by the Joule heating process results in downward buckling. Once the buckled structure makes physical contact with the bottom electrode, the device is in the programmed ("1") state. The programmed state of the memory device can be read by measuring the current flowing from the top electrode to the bottom electrode. (d) A schematic of the lateral view of a device before the sacrificial layer removal. (e) Air gap formation after the sacrificial oxide removal.

53x16mm (300 x 300 DPI)

Figure 2. Nano-thermomechanical switching and programming characteristics. (a) I-V curves for the two operation modes, which correspond to a one-time-programmable memory operation (the dashed black line) and a reversible switching operation (the solid red line). (b) The operation voltage V_{TH} relative to the device dimensions. The blue dots and red dots correspond to the V_{TH} values measured for devices with widths of 300 nm and 200 nm, respectively. The error bars represent standard deviations (the total number of measurements = 85). The dashed blue line ($W = 300$ nm) and the solid red line ($W = 200$ nm) correspond to the one-dimensional simplified model in which the concentrated electrothermal energy of the nanostructure, which originates from electron and phonon scattering, is considered. (c) TEM images of the device in the OFF/ON states.

102x130mm (300 x 300 DPI)

Figure 3. Temperature simulation and the influence of thermal conductivity on the nano-thermomechanical encoding process. (a) Temperature distribution at the turn-on voltage ($V_{PG}=0.75 \text{ V}$). Colored curves indicate beam profile and displacement. (b) The maximum beam displacement as a function of input electrical power. Note that touch-down occurs when the displacement exceeds about 20 nm. The device with the enhanced thermal property (red line, $\sigma = 26 \text{ Wm}^{-1}\text{K}^{-1}$) shows efficient actuation in comparison with the bulk thermal property (blue line, $\sigma = 175 \text{ Wm}^{-1}\text{K}^{-1}$). (c) FEM-simulated temperature with respect to the input electrical power.

80x35mm (300 x 300 DPI)

Figure 4. Nano-thermomechanical encoding process and the contacting interface. (a) A SEM image of the nanomechanical device after the encoding process. (b) The cross-sectional TEM image of the contact structure after the nano-thermomechanical programming process. The scale bar is 100 nm. (c) A magnified TEM image of the contact interface indicated by the dotted box in (b). The periodic line pattern between the dotted lines indicates the low-density crystalline tungsten. (d) Rearrangement of the tungsten crystal at the critical contact spot. (e) The preferred crystal direction [210] alignment of the reoriented tungsten lattice at the critical contact spot (insets: FFT patterns). This local rearrangement of the crystal structure is evidence of the influence of high temperatures during the thermomechanical programming process.

100x56mm (300 x 300 DPI)

Figure 5. I-V characteristics of the programmed device and the programming speed. (a) The device-to-device variation of the programmed state and the un-programmed state. On/off ratio exceeds 10^9 . Data were measured for 10 identical devices with the same dimensions. The solid gray line is a representative curve, and the error bars represent the mean standard deviation ($n = 10$). (b) Our programming-time measurement. The programming process was investigated by modulating the pulse width of the programming voltage. The minimum pulse width needed to activate a permanent contact corresponds to the programming time. For instance, a permanent contact was not activated by a pulse width below 50 ns. In addition to the highly consistent and controllable electrical property, the thermomechanical programming process offers rapid programming speed with efficient energy consumption. The thermomechanical programming of this device can be achieved within 60 nanoseconds (ns), including the mechanical motion and the thermal-assisted bonding process. The programming time was assessed by modulating the pulse width of a programming voltage; the minimum pulse width which activates the permanent contact corresponds to the minimum programming time.

51x29mm (300 x 300 DPI)

Figure 6. High-temperature stability of the programmed data. The upper panel contains histograms of the read currents from the samples prior to baking, and the solid lines represent fits to the experimental data with a normal Gaussian distribution. The read voltage V_{RD} was 0.3 V. The lower panel contains histograms of the read currents from the samples after baking. The thermal baking was performed in ambient N_2 at 400 °C for 30 min. The data were acquired from 60 different devices.

92x96mm (300 x 300 DPI)