

# Light-emitting Nanolattices with Enhanced Brightness

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## ABSTRACT

Three-dimensional (3D) photonic crystals have potential in solid state lighting applications due to their advantages over conventional planar thin film devices. Periodicity in a photonic crystal structure enables engineering of the density of states to improve spontaneous light emission according to Fermi's golden rule. Unlike planar thin films, which suffer significantly from total internal reflection, a 3D architected structure is distributed in space with many non-flat interfaces, which facilitates a substantial enhancement in light extraction.

We demonstrate the fabrication of 3D nano-architectures with octahedron geometry that utilize luminescing silicon nanocrystals as active media with an aluminum cathode and indium tin oxide anode towards the realization of a 3D light emitting device. The developed fabrication procedure allows charge to pass through the nanolattice between two contacts for electroluminescence. These initial fabrication efforts suggest that 3D nano-architected devices are realizable and can reach greater efficiencies than planar devices.

**Keywords:** nanolattice, photonic crystal, octahedron, 3D LED, nanofabrication

## 1. INTRODUCTION

Incandescent and fluorescent lighting together have dominated the lighting industry for over a century. Incandescent lighting is limited to 17 lm/W by a filament temperature that can reach up to about 3000 K, where emission is primarily in the invisible infrared regime as predicted by blackbody radiation theory. Fluorescent lighting is limited to 90 lm/W by the loss of energy incurred when an ultraviolet photon is converted to a photon in the visible range.<sup>1</sup> Inefficiencies like these present significant limitations given that lighting accounted for approximately 25% of energy usage in the United States in 2011.<sup>2</sup> Unlike these light sources, where most energy is converted to heat and very little becomes visible light, solid-state lighting—namely the light emitting diode (LED)—is able to provide a direct transfer of electrical energy into visible light, allowing for much greater luminous efficacies that do not suffer from any of the same fundamental limitations. Because of the large capital cost of producing LEDs, they must be efficient enough to offset this additional cost before they can fully replace other forms of lighting. Investment in solid-state lighting sources has potential for enormous energy savings. As estimated by the U.S. Department of Energy (DOE), 400 million terawatt hours of electricity can be saved annually by 2030 through the development of novel LED products, equivalent to \$40B annually.<sup>3</sup> This amount of energy is greater than two times the amount of energy produced by wind power or 20 times greater than the amount of energy produced by solar power in 2030, as predicted by the Energy Information Administration.<sup>3,4</sup> The DOE further predicts that these energy savings also present indirect advantages through the partial replacement of fossil fuel power-generation leading to a reduction in carbon emissions and help pave the way for renewable sources to become competitive by creating infrastructure that is energy-efficient enough that it can be self-sustainable by producing as much energy as it draws.<sup>5</sup>

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Modern day LEDs, which are made from semiconductor materials, are efficient when considering the amount of energy supplied that is directly converted into visible radiative emission (i.e. they can reach high internal quantum efficiencies). One of the main problems currently plaguing these devices is their inefficient ability to extract this generated light and radiate it into free space due to the large index difference between the device and air.<sup>6</sup> Instead, this light becomes trapped inside the device where it is eventually dissipated as heat. Common attempts to overcome the light-trapping problem and improve this extraction efficiency include the use of surface roughening, patterning, and 2D photonic crystals.<sup>6-9</sup> Research in LEDs has generally been limited to planar structures likely because of the difficulties associated with nanofabrication in three dimensions; a 3D LED device presents many potential advantages over its planar counterpart.

In this work, we introduce the fabrication of 3D nanolattices that (in principle) exhibit electroluminescence, i.e. nano-architected 3D LEDs. The point of departure from the emergent vibrant field of nano-architected materials is that the nanolattices in this work are active devices. The fabrication procedure requires the deposition of multiple layers of materials with different functionalities, which has not been extensively explored.

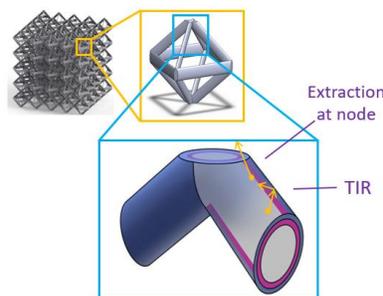


Figure 1. Zoomed in schematic CAD image of an octahedron nanolattice beam. Increased light extraction is obtained as light trapped within the structure reaches the node at an angle more favorable towards its escape. Additionally, nanolattice beams are elliptical or circular due to their fabrication method, which provides an another route for light escape.

These nanolattices can improve light efficiencies in two ways. Firstly, they serve as 3D photonic crystals, or structures that have a periodic refractive index. This periodicity creates a photonic band gap, or a range of frequencies over which light cannot propagate. At the edges of these band gaps, a greater density of states is available for light to couple into. By Fermi's golden rule, a greater density of states results in a greater rate of spontaneous emission. Even at frequencies away from the photonic band gap, a non-homogeneous periodic structure should lead to some variation in the density of states. Additionally, the geometry of nanolattices has no flat surfaces or interfaces and lattice beams are circular, which helps to minimize total internal reflection and to allow more light to escape the structure (Figure 1). Beyond these advantages, the nanolattices are open cellular solids and are homogeneously distributed in 3D, which should lead to a lower probability of reabsorption. Interesting future possibilities in creating actively tunable devices also exist because of their optical response to mechanical strain.<sup>10</sup>

## 2. DEVICE STRUCTURE

In conventional LED devices, the deposited semiconductor material must be free of defects because defects act as efficient non-radiative recombination centers.<sup>11</sup> To circumvent the challenges associated with deposition of single-crystalline semiconductor material onto an amorphous 3D structure, we chose to deposit silicon nanocrystals (SiNC's) as the candidate for the active material in the nanolattice devices.<sup>12,13</sup> Deposition of SiNC's is conducted in a non-thermal plasma reactor at room temperature,<sup>14</sup> and the particles possess an inherent size-dependent spectral tunability.<sup>15</sup> Unlike other common quantum dot systems, such as CdSe and PbS, SiNC's are relatively non-toxic and silicon is a much more abundant element.<sup>16</sup> While bulk silicon is an indirect band gap material where phonon-assisted electron decay would imply non-radiative transitions, SiNC's exhibit appreciable luminescence enabled by quantum confinement and wave-vector broadening, which facilitates more "direct-like" band transitions. We used an aluminum (Al) cathode and indium

tin oxide (ITO) anode in conjunction with the SiNC active layer, where confinement and recombination occur. Figure 2 shows a cross-section of this device stack that surrounds each individual polymer beam in the nanolattice. In this initial proof of concept part of this research, no additional device microstructure such as multiple quantum wells or electron blocking layers are incorporated and will be considered in the future. By the nature of a nanocrystal device and their associated small active region volume, the use of quantum wells significantly reduces carrier overflow and optical intensity saturation and thus improves device performance.<sup>11</sup>

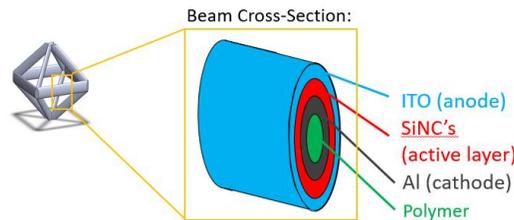


Figure 2. Cross-section of the device stack.

Figure 3 shows the schematic of the fabrication process. First, a silicon substrate undergoes wet oxidation at 1000 °C to form an electrically insulating layer of SiO<sub>2</sub> (>1 μm). It then serves as a substrate underneath a 3D nanolattice, which is written using two-photon lithography (TPL) direct laser writing in a professional photonic lithography system. An IR laser and ultraviolet sensitive resist are utilized in this system. The resist only polymerizes in the focal spot volume, or a voxel, when two photons of near-IR light are absorbed simultaneously, allowing for writing any arbitrary prescribed geometry at any depth in the resist without a mask. We chose to work with an octahedron geometry initially, though it represents a simple cubic analogue and therefore does not exhibit a full photonic band gap. Using this fabrication methodology, these octahedral nanolattices cannot be fabricated with a pitch sufficiently small to lie in the visible regime, though it is relatively open leading to easy deposition.

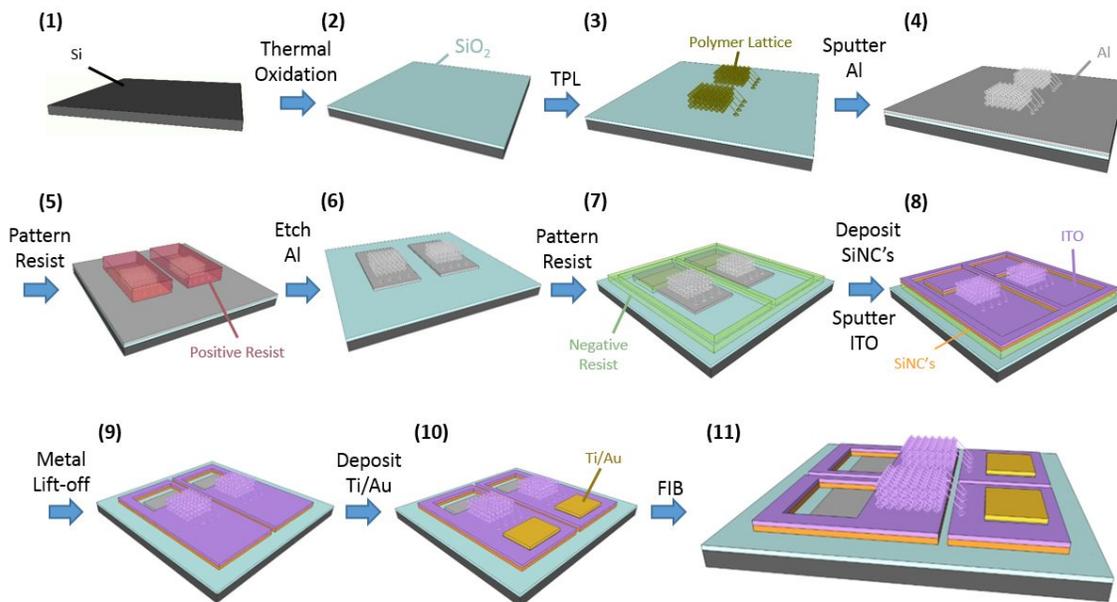


Figure 3. Schematic of the fabrication procedure which utilizes additional beams as bridges across a non-conductive “moat” to force charge through the lattice structure.

To take advantage of the structure's ability to enhance light emission, recombination must occur within the lattice rather than in the underlying substrate. The tortuosity of the nanolattice and the tendency of charge carriers to travel through the path of least resistance makes it challenging for the charge carriers to enter and recombine in a free standing nanolattice if an available path for recombination on the planar device is available. Device contacts must be placed on the underlying substrate because the nanolattice is fragile and cannot withstand the applied force required to connect a bond to a contact placed on the structure. We carefully designed these devices such that the only conductive path between electrodes is through the nanolattice. This is accomplished by patterning beams that extend from the top of the nanolattice down to the substrate at an angle (Figure 4).

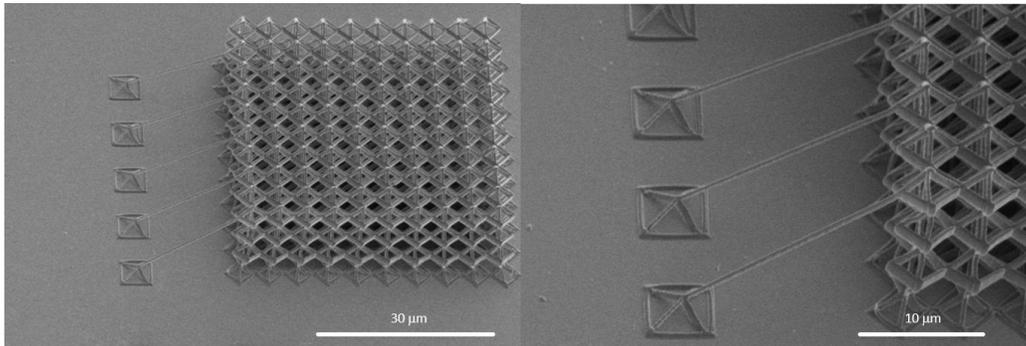


Figure 4. A representative nanolattice fabricated with beams extending from its top down to the substrate to allow charge to pass through the nanolattice only. The substrate electrically insulates the base of the beams from the rest of the structure making the only possible path for charge to pass between each contact to be through the beam bridges. In these images, the lattices are polymer and have not yet been coated.

After the polymer nanolattices are printed, the device stack fabrication begins with a 50nm thick Al cathode that is sputtered onto the nanolattice and the underlying substrate. To protect the Al on the nanolattice, as well as a region that will eventually serve as the external Al contact, we spun  $\sim 20 \mu\text{m}$  of positive resist, AZ4620K, over the entire substrate. The rest of the sample is then exposed through a photomask in a MA6 Karl Suss mask aligner. Several challenges exist at this step that require careful optimization. The spinning speed must be sufficiently slow to ensure that the resist covers the entire nanolattice and that it is not destroyed in the spin process. At the same time, the resist must be sufficiently thin to be exposed all the way throughout the layer to the substrate while minimizing proximity effects during lithography. An appropriate resist and developer system for this step and any following lithography steps must be selective against Al so that it will not be etched away. After successfully spinning the desired thickness of positive resist and completing lithography, wet etchant is used to remove Al from the unmasked substrate surface (Figure 5a and 5b) to ensure that the full device stack does not exist on the planar substrate. Following removal of the positive resist, the sample is coated with AZ 5214, used as a negative photoresist, and the Al contact region, as well as an electrically insulating boundary, are patterned into the resist in the mask aligner (Figure 5c and 5d). The device stack is completed with a 100 nm SiNC and 100 nm ITO layer deposited via a non-thermal plasma and sputterer, respectively.

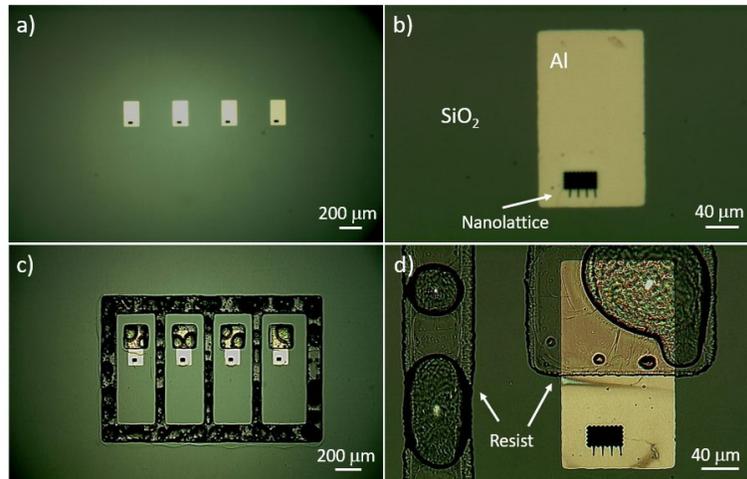


Figure 5. Optical microscope images of various fabrication steps. (a) and (b) After initial lithography step once resist and undesired Al have been removed. The Al that remains coats the structure or will be protected for a contact on the Al side. (c) and (d) After the negative resist has been deposited and patterned to protect a region of Al for the contact and to electrically insulate devices from one another, prior to deposition of SiNC's and ITO.

After removing negative resist, we used AZ4620K again to lithographically pattern the contact on the ITO side. To improve adhesion of the contact, we gently cleaned the sample with oxygen plasma to remove excess photoresist from the surface followed by a dilute ammonium hydroxide clean to etch away the thin native oxide layer. Immediately after, a Ti/Au contact is deposited using electron beam evaporation onto the ITO layer. A lift-off process removes deposited metal from the rest of the mask/substrate and exposes the surface. The negative resist is then removed.

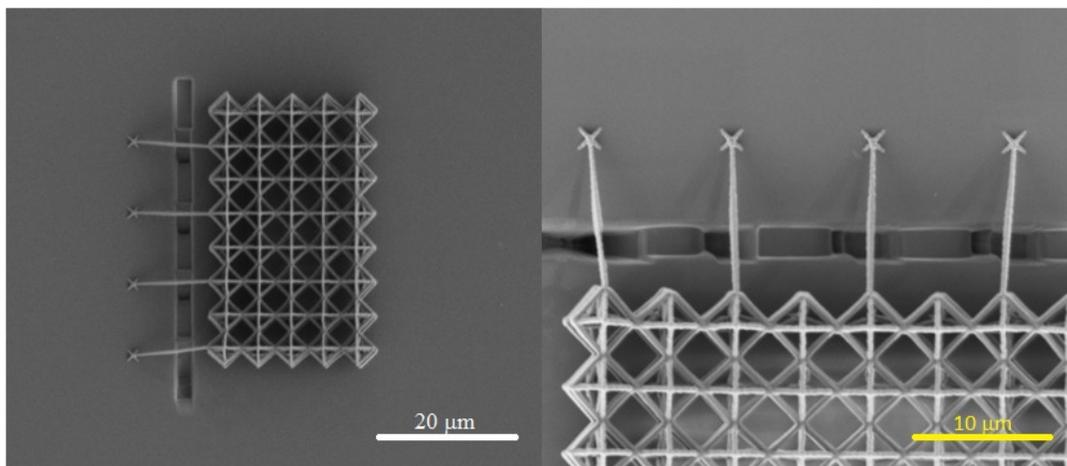


Figure 6. By carefully utilizing a FIB at various tilt angles, an electrically insulative gap down to the oxide layer can be created underneath the beam bridges.

We used a focused ion beam (FIB) to create an electrically insulating gap between the Al and ITO sides (Figure 6). This gap is positioned underneath the bridge and extends down to the insulating SiO<sub>2</sub> layer such that the only way for charge to pass from one contact to the other is through the bridge towards the nanolattice. In a final step, we used a Westbond wire bonder to bond a gold wire to the ITO and Al contacts.

The performance of these devices will be quantified via the external quantum efficiency (EQE), which is a figure of merit independent of the emission area. The EQE is calculated from the total optical power from the device, measured in an integrating sphere, and from the injected current.

### 3. CONCLUSION

Conventional planar LEDs suffer from the loss of light associated with having TIR occurring between a semiconductor material and air interface. Existing research often focuses on modifying this surface but only utilizes methods in two dimensions. This work aims to produce a novel, 3D active light-emitting device by utilizing nano-architected materials. These devices promise to improve light emission enabled by enhanced spontaneous emission via coupling to photonic band gap edges and other regions that exhibit an increased density of states, as well as increased extraction through the non-flat interfaces and lower reabsorption probability of a more open structure. The fabrication procedure to create such a device is challenging and goes far beyond what has been commonly done in the field of nano-architected materials. We demonstrate a successful fabrication of nano-architected 3D LEDs by utilizing multiple lithography steps to selectively deposit material and create a charge bridge that forces the charge to pass through the nanolattice. Because of the difficulties associated with deposition of single-crystalline material onto a 3D amorphous substrate, SiNC's are chosen as the device's active emitting material.

Future work on these devices following fabrication will focus on the measurement of their luminescence. Other routes include optimization of their optical and electronic properties by varying parameters such as structure, device microstructure, and active layer material/properties. Band gap tunability in these devices may be possible by mechanically straining the structure, first because the strain build up within the active layer leads to exciton localization, which shifts the electronic band gap, and second because mechanical strain changes the periodicity within the photonic crystal, which causes a shift in the optical band gap. Additionally, heat dissipation in these structures as well as active tunability via mechanical strain may also be explored.

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