Utilization of $NiSi_2$ as an Interconnect Material for VLSI

M. BARTUR AND M.-A. NICOLET, MEMBER, IEEE

Abstract—**The applicability of $NiSi_2$ as an interconnect material was investigated using narrow (5 μm- × 2600-μm) lines. 2500-Å-thick silicide lines were thermally oxidized to form a passivation layer of SiO_2 for the next metallization level. Isolation of more than 50 V for 2200-Å SiO_2 is achieved. The interconnect resistivity following the oxidation is 1.2–1.4 Ω/□. The maximum current capability of the lines was found to be > 5 × 10^6 A/cm^2 and their stability under prolonged high current densities was demonstrated. We propose a scheme to increase the local metallization-level density using $NiSi_2$ as an interconnect.**

I. INTRODUCTION

UTILIZATION of refractory metal silicides as an interconnect line for VLSI was demonstrated for $TiSi_2$, $TaSi_2$, WSi_2, and $MoSi_2$ [1]. The attractive properties of silicides are their low resistivity (at least one order of magnitude less than highly doped Si) and the possibility to form thermal SiO_2. In this context, it is of interest to know whether a near-noble metal silicide such as $NiSi_2$ (not refractory, melting temperature 993°C, lowest eutectic temperature 966°C) can be utilized as an interconnect material. The eutectic temperature of 966°C limits subsequent processing to a temperature of about 900°C. This limit is no hindrance since the metallization step comes after the completion of all the junction formation steps, and it is then desired to keep process temperatures low in order to minimize further diffusion.

We chose $NiSi_2$ because of its high oxidation rate [2], [3], its low resistivity (~35 μm·Ω·cm), and low formation temperature of the Ni-rich phase ($NiSi_2$, 250°C). Nickel is the dominant moving species in the formation of Ni silicides [3]-[5], which has been predicted to be advantageous [4]. These two factors (low temperature formation and metal being the dominant moving species) are not shared by the refractory metal silicides. Ni_2Si is also representative of a family of similar silicides (Co, Pt, Pd) that have not been explored yet as interconnection material. In this study, we explore the effect of oxidation on the resistivity of a narrow interconnect line, the applicability of the thermally grown SiO_2 as dielectric isolation, the current handling capability, and the long-term stability of $NiSi_2$ interconnect lines.

Manuscript received November 14, 1983; revised January 9, 1984. This work was supported in part by Mr. Arnold Applebaum, President of Solid-State Devices, Inc.

The authors are with California Institute of Technology, Pasadena, CA 91125.

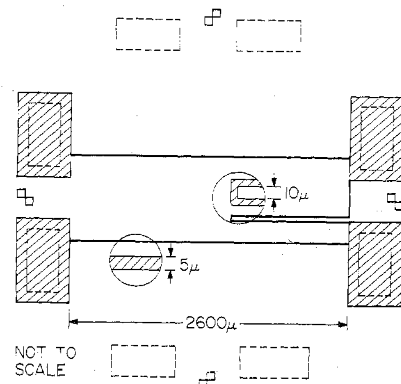

Fig. 1. Schematic description of our test pattern. The silicide area is shaded. The dashed lines are the contact opening in the thermally grown SiO_2 after oxidation. The top and bottom contacts are for the second-level pattern that can be deposited at a right angle to the first level.

II. EXPERIMENTAL

Narrow silicide lines (5 μm wide, 2600 μm long) were generated by delineating about 4000-Å thick-layers of evaporated Si on a SiO_2 substrate (using liftoff) in the form of a special test pattern (Fig. 1). About 700 Å of Ni was then deposited everywhere and a low-temperature (400°C) annealing step followed to form a NiSi layer over the Si lines (see Fig. 2). The low formation temperature effectively eliminates the lateral growth of the silicide. Some excess Si remained in the core of the line, but all the Ni was consumed above the line. The unreacted Ni between the lines was then removed by a selective etch (1 : 8 H_2O : HNO_3). A final high-temperature (650-800°C) vacuum annealing cycle transformed the silicide into $NiSi_2$, which at this high temperature mixes with the remaining Si. At this point, about 1500-Å Si remains as a supply for the SiO_2 formation. The amount of SiO_2 grown determines the final average ratio of Ni to Si in the electrically conducting film.

Oxidation was performed in wet oxygen at 750°C for 4.5 h or at 900°C for 0.5 h, which produces about 2200 Å of oxide. The oxide was selectively etched (using 1 : 6 HF : H_2O) from the contact windows (dashed lines in Fig. 1). To evaluate the passivation properties of the grown SiO_2, the same test pattern was laid down, at a right angle (perpendicularly) to the first one (Fig. 3), using either evaporated Au (2000 Å thick) or $NiSi_2$ deposited and patterned exactly as the first layer. (The dashed rectangles on the top and bottom of Fig. 1

0741-3106/84/0300-0088$01.00 © 1984 IEEE

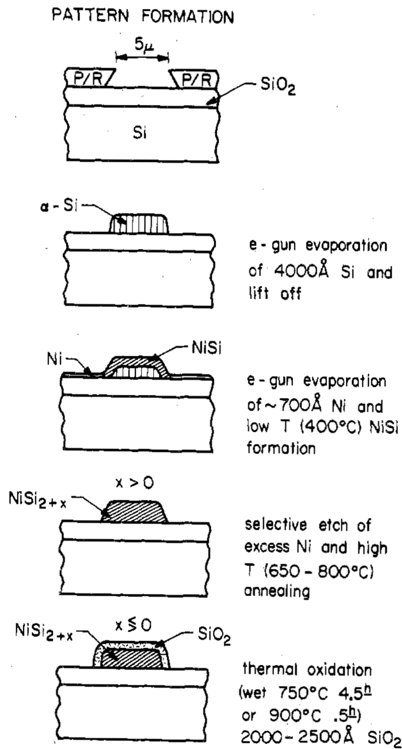

Fig. 2. Preparation sequence of the $NiSi_2$ interconnect pattern.

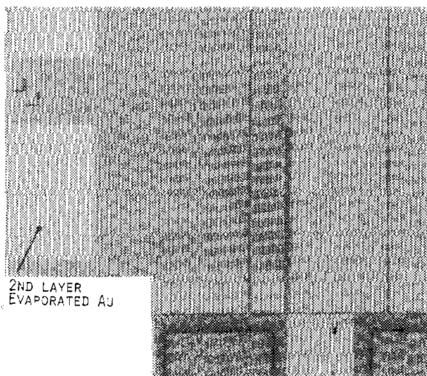

Fig. 3. Photograph of second-level Au metallization over an oxidized $NiSi_2$ interconnect pattern. There are eight intersection points. This structure was used to evaluate the dielectric strength of the thermally grown SiO_2. (Note the opened contact windows in the $NiSi_2$ pads.)

are the window openings for the second-layer metallization pads.)

To determine the temperature of the interconnect line during high-current stressing, the temperature coefficient of resistivity (TCR) of the lines was measured. To this end, the resistivity was measured using a four-point probe arrangement under low-current conditions. The sample with the contacting probes was placed in a temperature-controlled furnace and in about 1 h was allowed for stabilization at each temperature. The resistivity versus temperature curve for the temperature range of 25-350°C was obtained and from it the TCR was derived.

III. RESULTS

1) The resistivity of the lines before oxidation was about 700 Ω per line, or about 1.4 Ω/□. After oxidation at either 900°C or 750°C, similar results were obtained, and the integrity of the line was maintained—no open lines were found. The resistivity dropped to about 650 Ω per line, which may be due to grain growth during the oxidation process. The overall range of the line resistivity following oxidation was 1.2-1.4 Ω/□.

2) The critical current density, about which the lines were destructively opened after few minutes of current stressing, is higher than 5×10^6 A/cm². This to about 2.4 W per line! (The failure mode is probably due to melting after thermal runaway in our setup.) For comparison, a critical product of strip length (L) and current density (J), above which strip failure becomes inevitable, is about 2500 A/cm for Al films at 100°C [6]. We get a $J \times L$ product of about 10^6 A/cm at temperatures which are above 450°C.

3) The TCR was found to be $1 \pm 0.05 \times 10^{-3}$ °C^{-1} in the temperature range of 25-350°C.

4) Long-term stability was demonstrated by flowing 60 mA through the narrow-line structure. This current corresponds to a current density of about 3×10^6 A/cm². Out of the eight lines evaluated, none failed following 1 week (170 h) current stressing. From the resistivity at this current level and the TCR, we estimate the average line temperature to exceed 400°C.

5) Using Au as the second-layer metallization (Fig. 3), the isolation provided by the thermally grown SiO_2 at the eight intersection points holds more than 50 V (for both polarities). This bias corresponds to an electric field of $\sim 2.3 \times 10^6$ V/cm for our oxide thickness. This field value is higher than the previously reported one for the dielectric strength of SiO_2 grown on $NiSi_2$ [5]. The field-induced breakdown of the oxide is only one parameter controlling the desired SiO_2 thickness. In practice, the parasitic capacitance of a crossover (about 4 fF per cross in our case) dictates the oxide thickness.

6) Following oxidation, the surface of the test pattern becomes very rough as previously observed [5]. The narrow lines show the same surface characteristics as the large contact area. In fact, if the oxidation at 900°C was conducted for 1 h instead of 1/2 h, the patterns exhibited microcracks and yielded erratic electrical data due to discontinuities in the pads. Microcracks were not observed in the narrow lines. This surface roughness is an undesirable feature of oxidized $NiSi_2$.

7) The step coverage capabilities of the $NiSi_2$ line were evaluated with the same pattern and deposition procedure for a second metallization level (as in number 5 above). We find that most of the steps were broken after the high-temperature $NiSi_2$ formation step. A possible reason is the stress due to thermal mismatch between the $NiSi_2$ line and the SiO_2 substrate, however, our modest processing capabilities, the poor step coverage of the evaporated Si, and surface cleanliness problems, might be the real source of the problem.

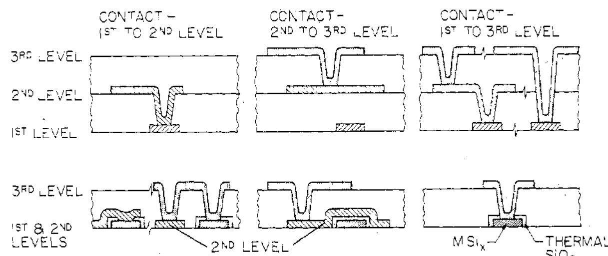

Fig. 4. Schematic demonstration of the advantages of an oxidized silicide line used as an interconnect. Third-level metallizations can be produced using only one step of thick dielectric deposition and one via opening step. (The white areas are the deposited and planarized dielectric—usually SiO_2.)

IV. CONCLUSIONS

In current technology, the dielectric isolation between metallization layers is made of either sputter- or CVD-deposited SiO_2. Prior to a subsequent metallization, the isolation layer is planarized either by reflow of phosphorus glass or by sputter etching. The final thickness of such dielectric isolation schemes is large, requiring deep contact windows (via's) to be etched accurately to the desired level thickness for interlayer connections. Currently, such processing is typically limited to three levels.

The present result suggests the very attractive possibility of double the metallization levels by using thin SiO_2 layers grown thermally on silicide over Si-(polycide) as dielectric isolation. After planarization, a first metallization level of silicide is deposited and oxidized for passivation, and then a second metallization level is applied on the first one. These metallization layers are at the same level, except at cross points, and are accessed by the same via etch process (Fig. 4). Conceptually, the procedure upgrades a three-level metallization to six levels, if the metal on SiO_2, protected by the deposited SiO_2, can sustain the high temperature required for thermal oxidation of $NiSi_2$. Even if only the first level is made of a silicide, the multilevel scheme is simplified drastically, as shown in Fig. 4.

We have demonstrated that $NiSi_2$ can be used as an interconnect and can serve for first-level metallization on planar surfaces. The low resistivity and the good long-term stability are very promising. Further topics that should be explored are the contact to the devices on the Si substrates (probably a diffusion barrier has to be employed) and the feasibility of using $NiSi_2$ as gate material for MOS technology.

ACKNOWLEDGMENT

The authors wish to thank Dr. D. Rutledge (Caltech) for the use of his photolithographic facilities.

REFERENCES

[1] *Proc. Workshop Refractory Metal Silicides for VLSI* (San Juan Bautista, CA), Sept. 20–22, 1983, (Continuing Ed. Univ. California Extension, Berkeley, 1983).
[2] M. Bartur and M.-A. Nicolet, "Thermal oxidation of nickel disilicide," *Appl. Phys. Lett.*, vol. 40, pp. 175–177, 1982.
[3] M. Bartur, "Thermal oxidation of transition metal silicides: The role of mass transport," *Thin Solid Films*, vol. 107, pp. 55–65, 1983.
[4] F. M. d'Heurle, "Material properties of silicides and device technology applications," in *VLSI Science and Technology/1982*, C. Dell'Oca and W. M. Bullis, Eds. Pennington: The Electrochemical Society, 1982, pp. 194–211.
[5] M.-A. Nicolet and S. S. Lau, "Formation and characterization of transition-metal silicides," in *VLSI Electronics: Microstructure Science*, vol. 6, N. G. Einspruch, Series Ed., G. B. Larabee, Ed. New York: Academic Press, 1983, chap. 6, pp. 360–361.
[6] J. R. Lloyd and P. M. Smith, "The effect of passivation thickness on the electromigration lifetime of Al/Cu thin film conductors," *J. Vac. Sci. Technol.A*, vol. 1, pp. 455–488, 1983.
[7] M. Bartur and M.-A. Nicolet, "Properties of SiO_2 grown on Ti, Co, Ni, Pd, and Pt silicides," *J. Electron. Mater.*, vol. 13, pp. 81–94, 1984.