of 1 MHz. The C/V plot shows standard accumulation, depletion and inversion behaviour with a flatband voltage of about -1 V; the hysteresis is indicative of surface state trapping. When the voltage swing was reduced for the C/V measurement, ΔV_{FB} was observed to be somewhat reduced as well, indicating a reduction in surface trapping. From the relation of maximum to minimum capacitance, the average carrier concentration near the surface is estimated[3] to be 5×10^{15} cm^{-3}. Diode C/V measurements indicate a carrier concentration of 1×10^{16} cm^{-3}, which is in reasonable agreement with the surface result.

Fig. 4 shows the 77 K I/V characteristics of an enhancement mode HgCdTe m.i.s.f.e.t. This device was fabricated on the same HgCdTe wafer as the m.i.s. capacitor. The channel length is 2 mils and the width is 40 mils. The m.i.s.f.e.t. follows ideal characteristics; i.e. the drain current is proportional to the square of the difference between the gate voltage and the threshold voltage, as shown in Fig. 5. The threshold voltage is +0·5 V, and increases to +0·6 V at 195 K. Examination of the I/V curves in the linear region combined with m.i.s. C/V measurements allows one to determine the effective mobility in the conducting channel.[4] Results of the measurements at two temperatures and for two compositions are shown in Table 1.

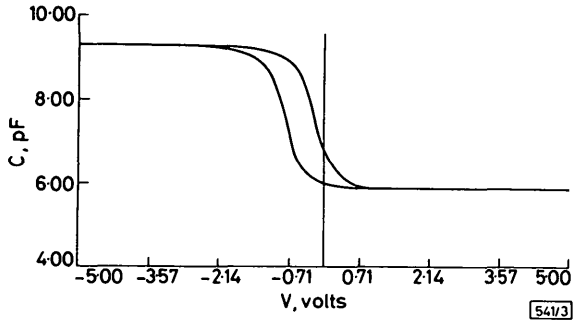

Fig. 3 *HgCdTe/CdTe m.i.s. C/V characteristics*
$T = 77$ K; $f = 1$ MHz

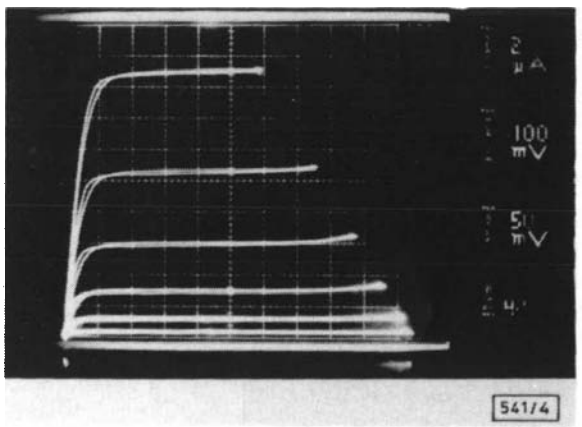

Fig. 4 *Current/voltage characteristics of enhancement mode HgCdTe/CdTe m.i.s.f.e.t.; T = 77 K*

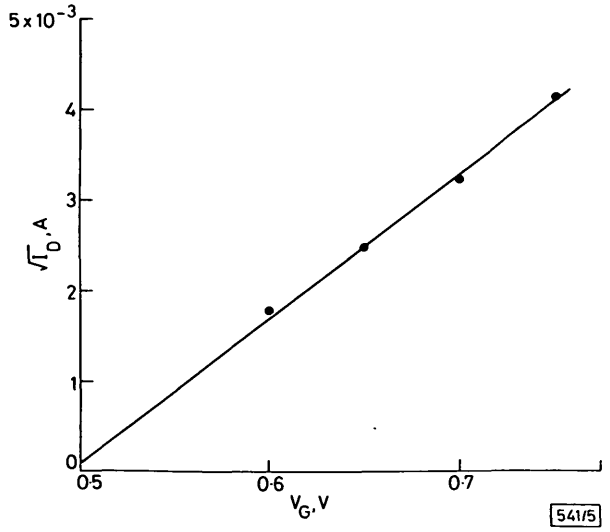

Fig. 5 *Drain-current/gate-voltage curve in saturation region of HgCdTe/CdTe m.i.s.f.e.t.*
$I_D = K(V_G - V_T)^2$
$K = \frac{1}{2}C_{ox}\mu W/L$
$T = 77$ K

Table 1 CHARACTERISTICS OF $Hg_{1-x}Cd_xTe$ M.I.S.F.E.T.s

x	T, K	μ_{eff}, cm^2/Vs	λ_c, μm
0·31	77	$6·9 \times 10^3$	4·4
0·39	77	$5·6 \times 10^3$	3·1
0·39	195	$4·4 \times 10^3$	3·0

The decrease in μ_{eff} with increasing CdTe/HgTe ratio is consistent with previously reported trends in bulk material;[5] furthermore, our surface mobilities are about one half bulk electron mobilities of $1–5 \times 10^4$ cm^2/Vs measured in epitaxial layers that have been converted to n-type by annealing.[6]

Conclusions: Conventional m.i.s. C/V data as well as planar n-channel enhancement mode m.i.s.f.e.t.s have been demonstrated in epitaxial $Hg_{0·7}Cd_{0·3}Te$. A logical extension of this work would be to fabricate an n-channel c.c.d. in HgCdTe that takes advantage of the ease of fabrication of n^+ on p junctions and utilises the high electron mobility available in this material.

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AlGaAs HETEROSTRUCTURE INJECTION LASER S.C.R.

Indexing terms: Lasers, Integrated optics

The operation of a gate-controlled p-n-p-n injection laser device has been demonstrated. The switching is accomplished by an electrical control signal. The threshold current of the laser incorporated into the device is about 100 mA, and its optical properties are similar to those of the Be-implanted laser reported recently.

In the many applications that call for pulsed operation of injection lasers, the semiconductor controlled rectifier (s.c.r.) is often used as the switching element in the driving circuit. This

type of device can also be used in detection and regeneration of light. Several GaAs and GaAlAs *p-n-p-n* light emitting devices have been reported recently.[1-6] However, all these are electrically two-terminal devices: they are either optically activated or they switch when the voltage imposed upon them exceeds their breakover value.

In this letter we report an AlGaAs heterostructure injection laser with the electrical operation of an s.c.r.; i.e. this is a three-terminal device where the switching is accomplished by applying a control signal to the gate electrode, in the usual method of operation of other s.c.r. devices.

A cross-section of the structure of the device is shown in Fig. 1*a*, and the schematic drawing of the device is shown in Fig. 1*b*.

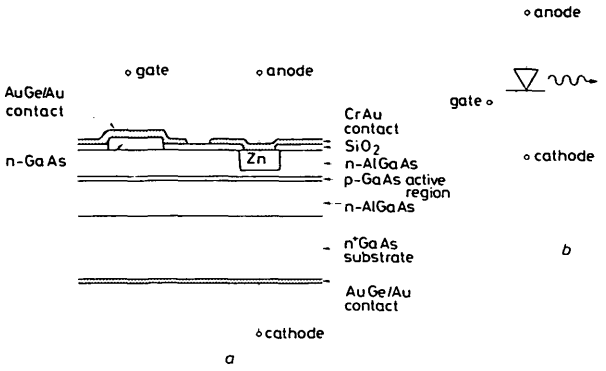

Fig. 1

a Cross-section of laser s.c.r.
b Schematic drawing of device

The four regions of the device have the following functions in the operation of the s.c.r. and the laser: the *n*-AlGaAs layer next to the substrate is the lower emitter of the s.c.r. and the lower cladding layer of the laser. The next *p*-GaAs layer is the lower base of the s.c.r. and the active region of the laser. The upper *n*-AlGaAs layer is the upper base of the s.c.r. and the upper cladding layer of the laser. The Zn-diffused region is the upper emitter of the s.c.r. The upper emitter-base junction of the device is a homojunction, formed by zinc diffusion in the $Al_{0.4}Ga_{0.6}As$ cladding layer. The lower emitter-base junction is the heterojunction at the interface of the active region, and the lower cladding layer. In the 'off' state, the current flowing in the device is mainly the leakage current of the heterojunction between the active region and the upper cladding layer, which is a reverse biased junction. Due to the low intrinsic carrier concentration in GaAs and AlGaAs, and the surface recombination currents, the current dependence on the voltage follows approximately an exp $(qV/2kT)$ law up to quite high injection levels. This lowers the overall sensitivity of the device, since it takes more current to obtain the 'on' voltage on a junction. In the 'on' state, all the junctions of the device are forward biased. Electrons are injected into the active region at the heterojunction from the lower emitter, and holes are injected from the upper emitter and flow through the upper cladding layer. This is basically a remote junction structure. Recombination of holes in the upper cladding layer is negligible because the carrier concentration in that layer is lower than in GaAs by a factor of exp $(-\Delta E_g/kT)$.

Fabrication of the device starts with the growth of four layers on an n^+-GaAs substrate by l.p.e. Typical layer thicknesses are: 3 μm (lower *n*-$Al_{0.4}Ga_{0.6}As$ layer), 0·25 μm (*p*-GaAs active region), 2 μm (upper *n*-$Al_{0.4}Ga_{0.6}As$ layer) and 0·7 μm (*n*-GaAs contact layer). The contact layer is removed in the region where the Zn is to be diffused. After deposition of 2500 Å of SiO_2 on the wafer, it is coated with photoresist in which stripes of width of 7 μm are opened. After etching the SiO_2 in these openings and removal of the photoresist, Zn is diffused in vacuum at 640°C for 20 min, followed by an annealing of the wafer at 800°C for 30 min. This results in diffusion of the Zn down to a distance of 0·5 μm above the active region, according to the results of Reference 7. During the Zn diffusion, the stripes widen up to 10 μm because of undercut below the SiO_2 layer. An evaporation of CrAu, etching the SiO_2 above the GaAs contact layer, and an evaporation of AuGe/Au, form the anode and the gate contacts, respectively, of the s.c.r. The gate contact is separated from the anode contact by etching the metal contact between them in a 10 μm stripe. The substrate is subsequently lapped and the *n*-type substrate is deposited with AuGe and Au, followed by alloying at 380°C. Typical lengths of individual devices are about 300 μm.

The anode-current/anode-cathode-voltage curve is shown in Fig. 2, a typical s.c.r. curve. As the magnitude of the gate current pulse is increased, the device switches at lower voltages. (The loops in the left-hand side of the origin in Fig. 2 are an artefact of the measurement technique.) Threshold currents of the lasers were about 100 mA, and their optical properties, including near field and far field patterns, are very similar to those of the Be-implanted lasers,[8] leading to the conclusion that they are gain guided. Operation in a single transverse mode was obtained up to about 1·5 I_{th}.

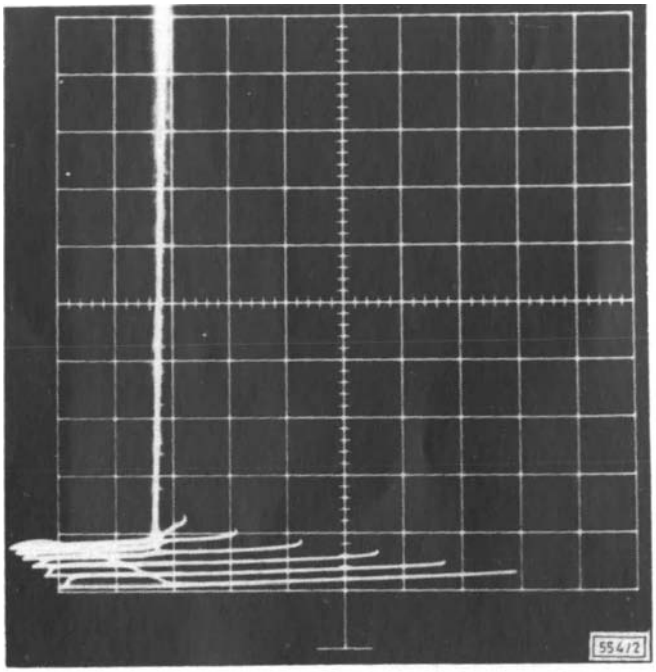

Fig. 2 *I/V curve of the laser s.c.r.*

Horizontal scale, 1 V/div;
Vertical scale, 1 mA/div; gate current, 200 μA/step)

In conclusion, we have demonstrated the operation of a gate-controlled *p-n-p-n* injection laser device (laser s.c.r.). This device may be useful in applications where the laser is operated in a pulsed mode. Fabrication of this device on semi-insulating GaAs substrates can also be done by growing an additional *n*-type layer immediately on the substrate and contacting this layer after an appropriate etching.

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ELIMINATION OF EMITTER EDGE DISLOCATIONS IN SILICON PLANAR *n-p-n* TRANSISTORS

Indexing terms: Bipolar transistors, Crystal defects

It is shown that the conventional method for elimination of emitter edge dislocations, which consists of a low concentration emitter phosphorus diffusion, has two disadvantages: it increases reverse emitter–base current and reduces current gain at low currents. Also, it is shown that the mentioned disadvantages can be successfully avoided by a new method for elimination of emitter edge dislocations, which consists of a high concentration emitter phosphorus diffusion followed by an additional shallow boron diffusion.

Introduction: It is well known that emitter phosphorus diffusion normally used in fabrication of planar *n-p-n* transistors may create two kinds of dislocations:[1] diffusion induced dislocations (d.i.d.), which appear inside diffused emitter areas, and emitter edge dislocations (e.e.d.), which appear around the planar edges of these areas. Of these dislocations e.e.d. represent one of the main causes of the reduced yield and reliability of planar *n-p-n* transistors,[2,3] and so several different methods for their elimination have been developed to date.[1,4,5] The conventional method for e.e.d. elimination consists of a low concentration emitter phosphorus diffusion from $POCl_3$ at about 1100°C in an open tube furnace. This letter deals with a new method which shows considerably improved properties compared to those of the conventional method; it consists of a high concentration emitter phosphorus diffusion followed by an additional shallow boron diffusion.

Experiment: In order to study the methods for e.e.d. elimination, four different lots of planar *n-p-n* transistors were fabricated starting from dislocation-free Si epitaxial wafers (*n*-type, orientation [111] and resistivity 4–6 Ωcm). Wafers were processed through a standard AF planar *n-p-n* transistor fabrication routine up to the emitter diffusion stage. Wafers were then divided into four lots and each of them was subjected to phosphorus diffusion from $POCl_3$ at 1100°C in the open tube furnace, but with different gas flow rates in the diffusion system. Gas flow rates were adjusted to provide conditions for two different phosphorus diffusions:[3,4] low concentration (lots 1 and 2) and high concentration phosphorus diffusion (lots 3 and 4). Prior to the emitter oxidation the wafers from lot 4 were subjected to an additional boron diffusion from boron nitride at 950°C in N_2 ambient, for 15 min. Emitter oxidation was performed at 950°C in water vapour ambient. After the emitter oxidation the wafers from lot 2 were subjected to an additional gettering process using phosphorus glass.[6] Finally, after aluminium metallisation of emitter and base contacts and gold plating of the collector side, the transistors were mounted on TO-18 headers and encapsulated in dry N_2.

Results and discussion: Fig. 1 shows the typical Sirtl etch[7] patterns of control wafers from different lots. It is obvious that transistors 1 and 2, corresponding to the conventional method for e.e.d. elimination, are free of both d.i.d. and e.e.d. On the other hand, in transistor 3 a high density of d.i.d. and a large number of e.e.d. are obtained. Finally, in transistor 4, corresponding to the new method, a high density of d.i.d. and no e.e.d. is obtained. From these results it is clear that both methods can successfully prevent the creation of e.e.d. There exist two possible mechanisms to explain the elimination of e.e.d. in the new method, which have been described in our

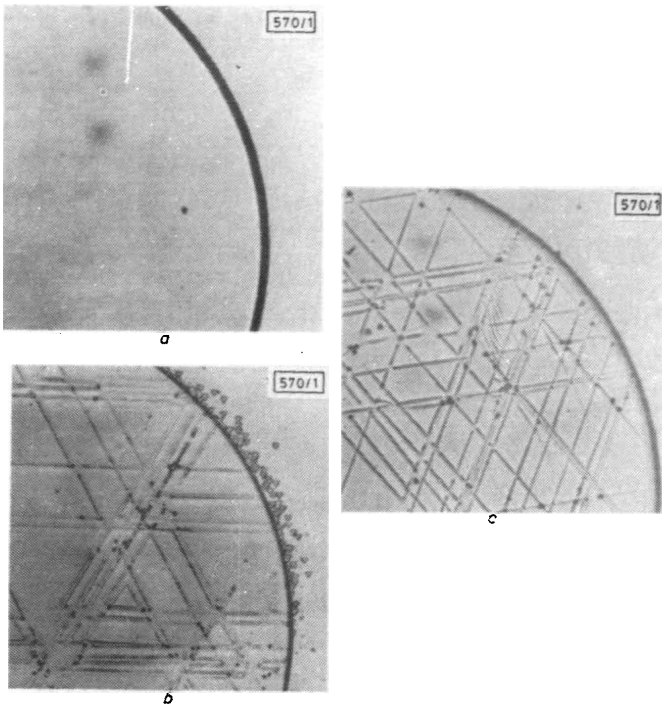

Fig. 1 *Typical Sirtl etch patterns of control wafers from different lots (× 330)*
a lots 1 and 2
b lot 3
c lot 4

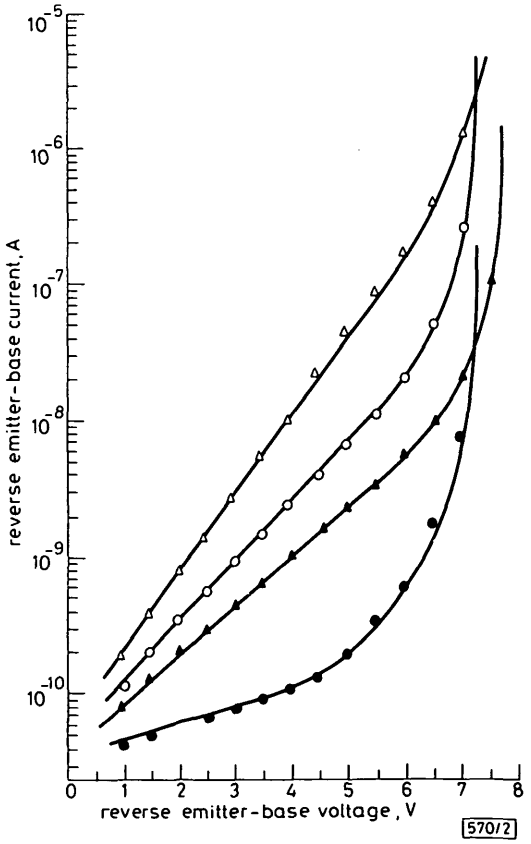

Fig. 2 *Typical reverse emitter–base characteristics of transistors from different lots*
△ transistor 1 ○ transistor 3
▲ transistor 2 ● transistor 4