

## AN INTEGRATED SERIAL TO PARALLEL CONVERTER FOR TELETEXT APPLICATION

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### 1. INTRODUCTION

Teledata systems implemented as either television add-ons or new set features will require relatively complex integrated circuits. Consumer acceptance of these systems will be a sensitive function of their price. Thus, the various IC technologies must be evaluated with respect to achieving adequate performance at minimum cost. We have investigated the feasibility of N-channel MOS for teledata serial-to-parallel conversion.

### 2. FEATURES OF THE NMOS TECHNOLOGY

The NMOS process is well-suited to consumer electronics applications for three general reasons. First, it allows for very high logic functional densities in comparison to bipolar technologies. Second, while power consumption per gate is considerably greater than in complementary MOS (CMOS) processes, NMOS is still superior to bipolar in this area. Finally, NMOS is

cheap. Early purchasers of scientific calculators have witnessed considerable erosion in the value of their investments.

NMOS integrated circuits have already been applied to functions analogous to those in teledata decoders. The latest generation of CRT controllers<sup>1</sup> are close to the complexity required for decoder output circuitry. NMOS random access memories will almost certainly store teledata display character ASCII codes. MOS technologies are thus suitable for the elements of the decoder system block diagram shown crosshatched in figure 1.

### 3. NMOS INPUT CIRCUITS FOR TELEDATA

Historically, NMOS circuits have been applied to systems where high performance logic gates are unnecessary. The teledata byte rate of approximately 700 KHz is well within these historical limits. The key question in NMOS teledata input circuit design is whether or not the technology can support data

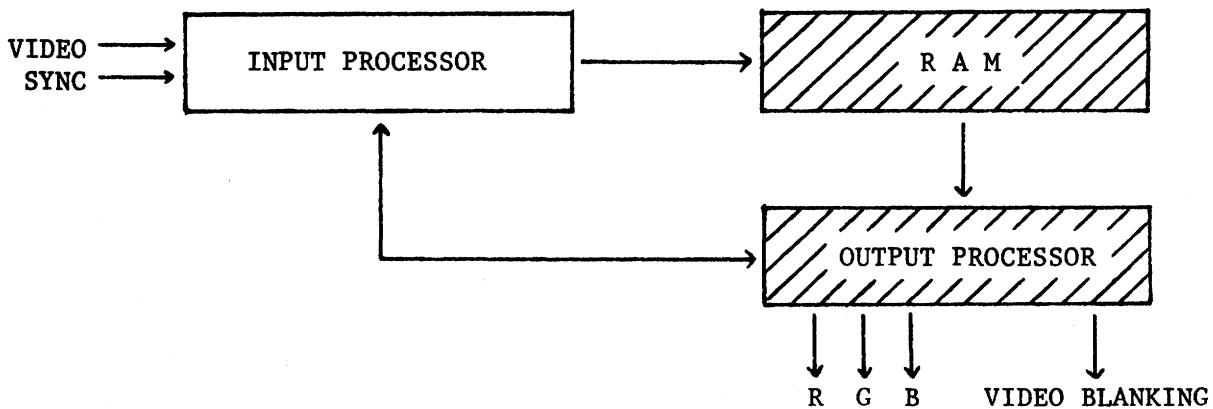


Figure 1 Teledata Receiving System

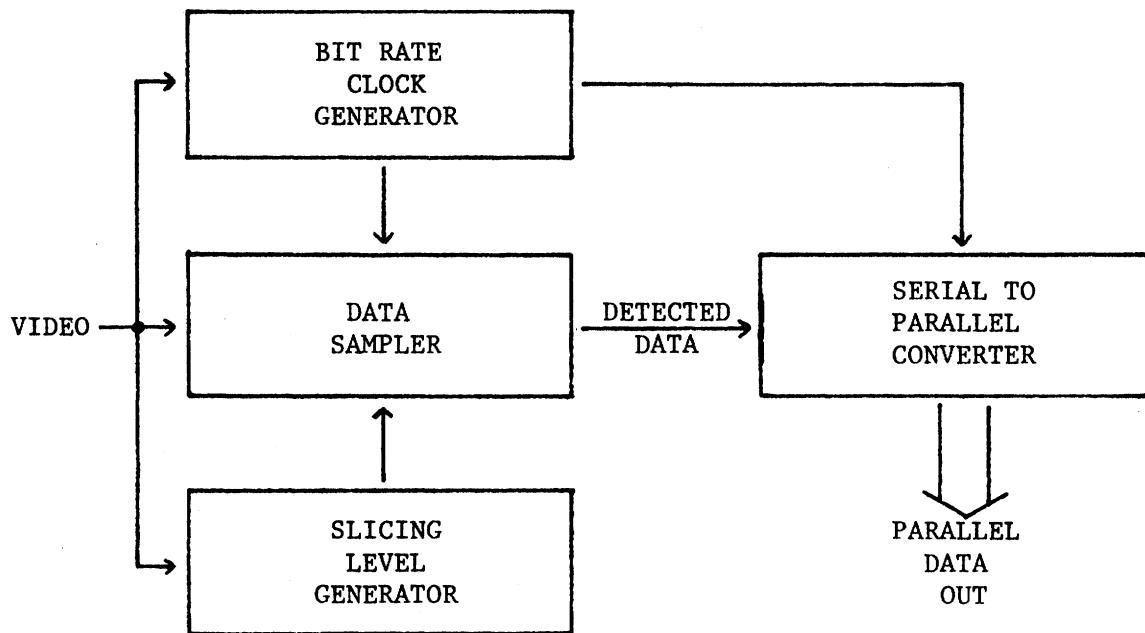


Figure 2 Teledata Input Circuits

detection and serial-to-parallel conversion functions at bit rates on the order of 5.5 MHz. A block diagram of teledata input circuits that must operate at the bit rate is illustrated in figure 2.

The bit rate clock generator must acquire bit synchronization during the 12 bit clock run-in period. Several schemes for data-derived bit synchronization are summarized in ref. 2. The Maximum A Priori (MAP) systems require a tapped delay line with a crystal-generated input signal. The various taps are compared with the phase of the clock run-in and the tap with best agreement is selected as the local bit clock. Extensive computer simulations of this type of bit synchronization system have demonstrated feasibility of their implementation in a commercial NMOS process.

Data detection can exploit some of the most sensitive analog circuits in MOS design—the dynamic RAM sense amplification circuits. These circuits can compare teledata signal levels to a slicing level reference stored on a MOS capacitor. Appropriate charge routing logic can update the reference

level to adapt to signal amplitude distortion. The performance of both sense amplifiers<sup>3</sup> and pass transistor charge transfer logic are more than adequate for teledata bit rates.

The conversion of detected teledata bits into a byte format for subsequent processing is normally accomplished by a shift register-based circuit. Simulations of shift register circuits indicate practical NMOS shift registers can operate at clock rates in excess of 50 MHz. We have recently completed the layout of an integrated serial-to-parallel converter to examine the details of operation of this portion of the decoder input system. To minimize fabrication costs, we have not utilized the full processing complexity available to the IC manufacturer producing the chip.

#### 4. CONCLUSIONS

Our investigation of teledata receiver systems indicates that NMOS performance is currently adequate for detector integrated circuits. Thus, NMOS should offer the most cost-effective technology for consumer teledata decoders. An attractive additional consideration is that

technology evolution may allow for a single chip decoder circuit by the time broadcast standards for U.S. teledata are adopted.

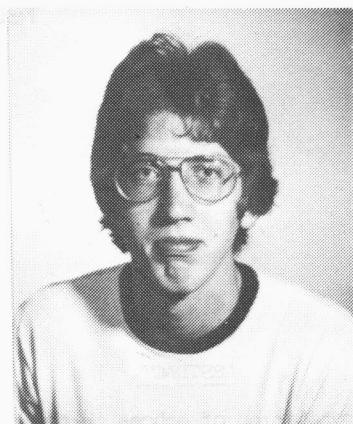
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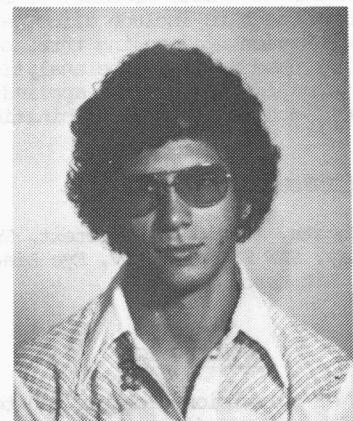
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#### BIOGRAPHIES



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