gain against frequency exhibits evenly spaced peaks. The axial modes tend to lock in clusters around these peaks, but coherence cannot be maintained among clusters because of spontaneous emission noise.[4] A bandwidth limiting element inside the resonator selects one gain peak so that only one coherent mode cluster is excited. Such an element is incorporated in the system reported here.

The laser system is shown in Fig. 1. The diode laser is of the stripe-geometry type, c.w. at room temperature. One of the cleaved faces is antireflection-coated with a single layer of SiO, the light output from that face is collimated by a microscope objective (n.a.: 0.85) and is reflected back to the diode by a plane gold mirror. This arrangement allows intracavity elements and is more stable against mechanical perturbations. Although the antireflection coating is imperfect (a few percent reflectivity is left), it succeeds in eliminating the familiar noise spike,[5] around 700 MHz in this case, which would interfere with the modulation of the laser. An etalon is inserted in the cavity to limit the oscillation to one single longitudinal mode of the diode subcavity. Such modes are separated by about 2 Å. The laser centre frequency is near 0·84 μm. The etalon is made by coating a quartz slab to a bandwidth of about 1·4 Å and has a free spectral range of about 9 Å. The overall cavity round-trip frequency is about 430 MHz. Modelocking is achieved by modulating the d.c. drive current of the laser diode by an r.f. source, an amateur radio transceiver which puts out 0·5 W at 433·188 MHz. No impedance matching is attempted. Fine tuning is accomplished by adjustment of the cavity length at fixed oscillator frequency. With the r.f. off, the threshold is 190 mA; the r.f. reduces it to about 180 mA. The pulse width is measured by the conventional method of second harmonic generation in $LiIO_3$. The measurement arrangement setup is standard. Fig. 2 shows a trace of the second harmonic. The contrast ratio is close to 3:1 as expected of coherent pulses.[6]

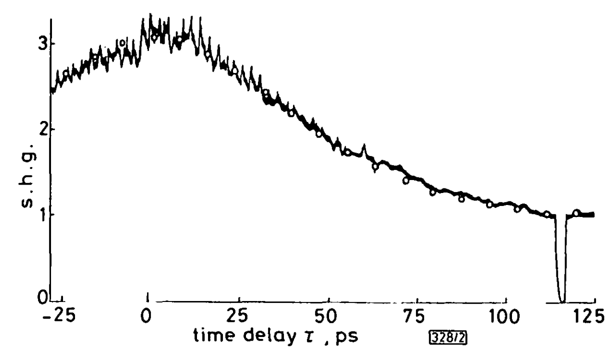

Fig. 2 *Intensity autocorrelation trace*
63·6 ps f.w.h.m. at 186 mA

The 25 mm movement of the moving arm of the Michelson interferometer limits the total delay to 167 ps. The circles are a Gaussian fit, $\exp\{-(\tau/\tau_0)^2\}$, with $\tau_0 = 54$ ps, which corresponds to pulses of 63·6 ps f.w.h.m. This is to be compared with the theoretical value[7]

$$\ln 2\,\{\sqrt[4]{M}\,\sqrt{(\omega_m \omega_g)}\}^{-1} \approx 80 \text{ ps}$$

where $M \approx 0{\cdot}1$ is the modulation depth, ω_m the modulation frequency and $\omega_g = 1{\cdot}4$ Å the bandwidth of the etalon.

When the laser output is detected by a fast photodiode, spectral analysis of the photocurrent reveals only components at the modulation frequency 433 MHz and its higher harmonics; subharmonics are not present. Pulses therefore occur at the modulation frequency and not at its submultiple as in a previous experiment.[3] Display on a sampling oscilloscope confirms this.

Measurement of the bandwidth with a grating spectrometer gives a resolution-limited value of 1 Å. More accurate measurement is prevented by the degradation of the laser diodes in stock. Some chirp may be expected, however, because of the etalon.

In conclusion, we have demonstrated the feasibility of generating coherent pulses with GaAs lasers by modelocking. The bandwidth-limiting element is crucial in obtaining coherent pulses. Its removal in our experiments leads to incoherent although somewhat shorter (40 ps) pulses. We believe that the generation of even shorter coherent pulses depends on a complete elimination of the cleaved face reflectivity.

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ELECTRICAL PROPERTIES OF SILICON-IMPLANTED FURNACE-ANNEALED SILICON-ON-SAPPHIRE DEVICES

Indexing terms: Bipolar transistors, Metal-oxide-semiconductor field-effect transistors, semiconductor diodes, Semiconductor epitaxial layers

The crystalline quality of s.o.s. layers can be improved near the silicon-sapphire interface by silicon implantation followed by recrystallisation. Device performance on such layers is markedly improved as to *n*-channel m.o.s.t. noise and leakage current, reverse diode current and lateral bipolar transistor gain. Minority-carrier lifetimes up to 50 ns are deduced.

Crystallographic defect formation occurring during the heteroepitaxy of silicon on sapphire (s.o.s.) is known to cause a significant degradation of some electrical characteristics of s.o.s. devices. The defect density is highest at the silicon-sapphire interface and decreases towards the silicon surface. It has been demonstrated recently by channelling techniques[1] that the interfacial silicon region can be substantially improved by silicon implantation and furnace annealing. M.O.S. transistors have been fabricated on such wafers preserving an as-deposited part of the layer as a reference. Before processing, silicon implantation along the ⟨100⟩ direction was carried out to amorphise the 0·6 μm thick silicon layer but preserving a thin ($\lesssim$ 50 Å) single-crystal surface region, as was verified by reflection electron diffraction (r.e.d.) measurements. Most of the Si ions were channelled, since the wafers were oriented within 1° of the incident beam and since the f.w.h.m. of the channelling dip in Si is 5·5 – 6° for Si ions having energies of 360–550 keV.[2] The beam currents were kept below 0·3 $\mu A/cm^2$ to avoid heating of the target. In a first experiment, the wafers were held at −70°C during the implantation. The energies and doses used were: 550 keV, $7 \times 10^{14} cm^{-2}$ and 360 keV, $3 \times 10^{14} cm^{-2}$ (*A*) or, alternatively, 450 keV, $2 \times 10^{15} cm^{-2}$ (*B*). For the second experiment, silicon ions were implanted at room temperature at 450 keV with doses of $2 \times 10^{15} cm^{-2}$ (*C*). Furnace annealing at 560°C for 2 h in vacuum or in a flowing helium atmosphere induced a solid phase epitaxial regrowth with a growth rate of about 100 Å/min. The lightly damaged surface region acts as a seed. The samples were analysed by 1·5 MeV He^+ channelling. The regrown layers have given an aligned backscattering yield at the silicon/sapphire interface χ_i about half as much as in the as-deposited layer, and the surface yield χ_0 is only slightly increased. The backscattering results are summarised in Table 1. Cross-sectional transmission electron microscopy analysis has shown previously on samples implanted at liquid-nitrogen temperature that only dislocations (but no twins) are present in the regrown layer.[1]

Table 1 1·5 MeV He^+ CHANNELLING ANALYSIS

Implantation conditions	Before anneal χ_i	χ_o	After anneal χ_i	χ_o
Unimplanted	0·53	0·08	0·53	0·08
A	1	1	0·27	0·10
B	1	1	0·31	0·15
C	1	0·17	0·34	0·08

Devices were fabricated using a low threshold voltage c.m.o.s. silicon gate process with a gate oxide thickness of 72 ± 2 nm. After processing, the silicon layer is 0·4 μm thick and threshold voltages are +0·3 V for *n*-channel m.o.s.t.s and −0·3 V for *p*-channel m.o.s.t.s. In the silicon-implanted part, both threshold voltages are shifted by +0·4 V and +0·8 V for implantations at low and ambient temperature, respectively. This shift may be attributed to (*a*) *p*-type doping due to aluminium atoms diffusing from the sapphire into the amorphised silicon layer during its recrystallisation, and (*b*) a reduction of the fixed positive surface-state charge Q_{ss} located near the silicon-sapphire interface. *p*-type doping due to a contaminated silicon beam seems very unlikely. Because of the threshold-voltage shift, the analysis of the electrical properties of the regrown silicon has been mainly performed on *p*-type layers.

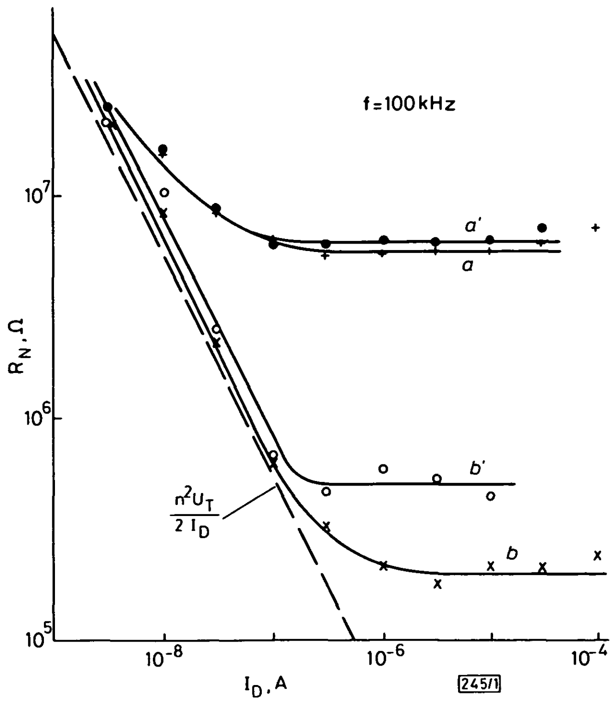

Fig. 1 *Noise equivalent gate resistance R_N against drain current I_D for n-channel s.o.s. m.o.s.t.s*

As-deposited s.o.s., *a*, *a'*; regrown s.o.s. after Si implantation at low (*b*) and ambient (*b'*) temperature

Noise in solid-state devices is generally considered to be a sensitive tool for the investigation of materials. Consequently, noise characteristics of *n*-channel m.o.s.t.s (width/length = 20 μm/10 μm) have been determined using measuring techniques described elsewhere.[3] M.O.S.T.s exhibit mainly two noise components: shot noise and flicker ($1/f$) noise. The former is dominant at low drain current or high frequency. For transistors operating in the saturated subthreshold region, i.e. $V_D \gg V_T = kT/q$, the low current asymptotic value of R_N is given by $n^2 V_T / 2I_D$, *n* being the slope factor of the weak inversion region for which $I_D \approx \exp(V_G/nV_T)$. The latter is dominant at high drain current or low frequency and is current-independent.

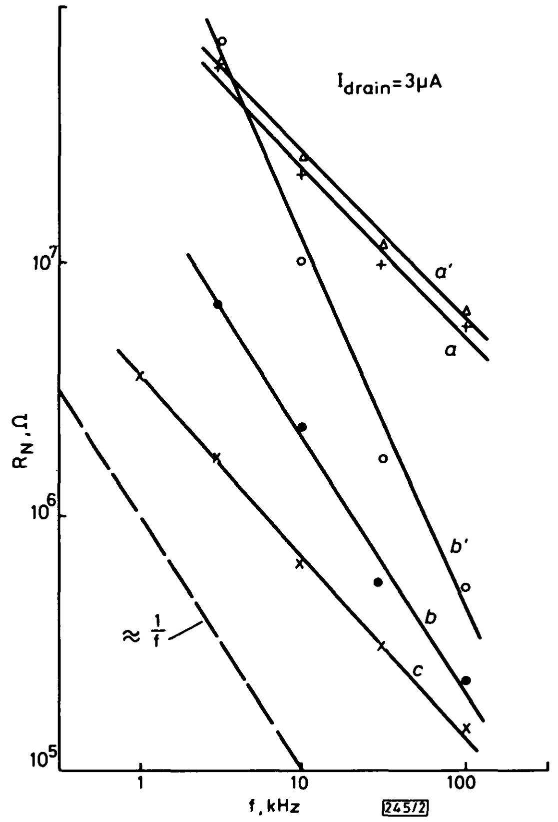

Fig. 2 *Noise power spectrum of n-channel m.o.s.t.s operating in strong inversion*

a, *a'*, *b*, *b'* as in Fig. 1; *c*, bulk silicon

Fig. 1 shows, at a frequency of 100 kHz for transistors operating in saturation, the equivalent input noise resistance referred to the gate R_N as a function of the drain current I_D. Curve *a* and *a'* correspond to the as-deposited part, curve *b* and *b'* to the regrown part of the wafer. It can be seen that the noise is reduced in the strong inversion region by a factor of 25 for the first experiment and by a factor of half as much for the second one. In Fig. 2, R_N is plotted as a function of frequency to verify the $1/f$ behaviour. Comparison of the as-deposited part (curve *a*) with the regrown part (curve *b*) of the layer shows that noise reduction occurs over the whole frequency range of measurements. In contrast to the implantation at low temperature, curve *b'* intercepts curve *a'* at about 3 kHz. Its behaviour is in $f^{-\alpha}$ with $\alpha > 1$. For comparison, the characteristics for a *n*-channel bulk silicon m.o.s.t. of the same oxide thickness, normalised to the same shape factor, i.e. the gate surface, are given (curve *c*).

These results can be directly related to the improved quality of the silicon layer if flicker noise is considered as a transport noise residing in the volume. At the same time the contribution to the noise of the silicon-sapphire interface[4] is probably also reduced, since the depletion layer reaches the interface at least in strong inversion.

Further evidence for the improved quality of the regrown silicon layer is observed as a drastic increase of the minority lifetime which is smaller than 0·1 ns for s.o.s. films thinner than 1 μm.[5] For the first time, lateral bipolar s.o.s. transistors having a significant current gain β have been realised. Only mesa-type bipolar s.o.s. transistors have been reported up to now.[6]

Bipolar transistors with an annular base (perimeter = 100 μm, width = 3 μm) have been measured. Fig. 3 demonstrates the performance of such *n-p-n* devices. Assuming an average effective base width of at least 6 μm, a minority-carrier lifetime up to 50 ns is determined. It has thus to be concluded that the recombination rate has been reduced by about 3 orders of magnitude.

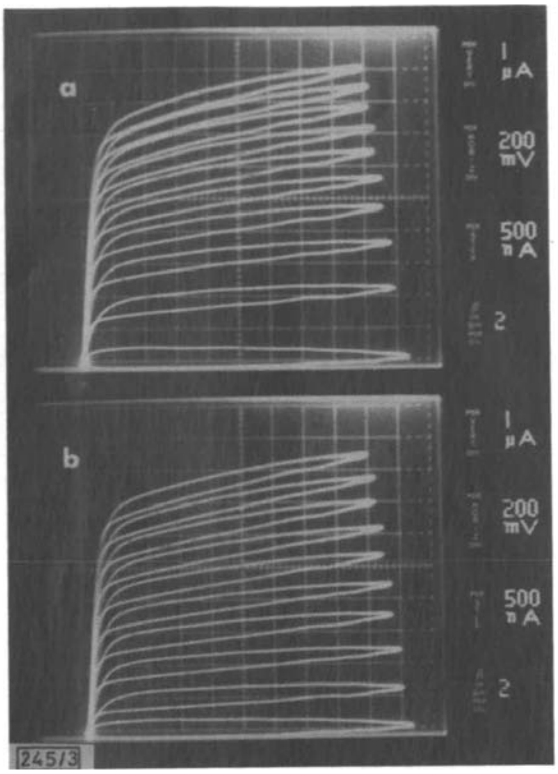

Fig. 3 *S.O.S. lateral bipolar transistor in a regrown layer after Si implantation at low (a) and ambient (b) temperature*

Finally, another additional consequence is the reduction of the reverse-biased drain junction leakage current at 1·5 V from 0·3 pA/μm width to less than 0·01 pA/μm for *n*-channel m.o.s.t.s. n^+-p and p^+-n closed structure gated controlled diodes (perimeter = 320 μm) were also investigated. Table 2 shows reverse currents at 1·5 V reverse voltage for $V_G = 0$. The data present no significant difference for all implantation conditions. Most of the large generation current occurring in s.o.s. is usually attributed to the defects occurring in the silicon layer. The observed dramatic reduction of the number of defects in the regrown layer is in agreement with the improved crystalline quality revealed by channelling analysis.

In conclusion, silicon-implanted furnace-annealed s.o.s. wafers have revealed *n*-channel noise similar to that of bulk silicon *n*-channel m.o.s.t.s. They have allowed the realisation of lateral bipolar transistors and a significant reduction of leakage currents. These new results open new possibilities for analogue applications. In addition, the reduction of the static current consumption of s.o.s. circuits leads to a more competitive technology. The improvement of the silicon-sapphire interface should render possible the scaling down necessary for a v.l.s.i. technology. Further work is in progress to find less stringent and most efficient implantation conditions and to control threshold voltages.

Table 2 REVERSE CURRENTS OF G.C. DIODES

	n^+-p g.c.d.	p^+-n g.c.d.
As-deposited s.o.s.	600 pA	500 pA
Regrown s.o.s.	5–10 pA	70 pA

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MINIMISATION OF MODAL NOISE IN OPTICAL-FIBRE CONNECTORS

Indexing terms: Optical couplers, Optical fibres

Modal noise has recently been recognised as a source of interference in multimode optical-fibre systems involving coherent sources and misaligned connectors. This letter describes a technique whereby the effects of fibre misalignment may be minimised by the appropriate design of the connector. The essential principle is that far-field rather than near-field coupling is utilised. A significant reduction in modal noise due to misalignments can be expected using this principle, and the estimated losses are comparable to those in conventional connectors.

Modal noise has recently been recognised as a source of interference in multimode optical-fibre systems.[1] The effect only occurs when the coherence time of the optical source is greater than the dispersion time of the fibre, and when the fibre system includes some form of misaligned joint. The misalignment may occur at a fibre splice or connector or at the final photodiode. A mechanical or thermal disturbance acting on the fibre will then shift the geometrical distribution of the mode pattern at the end of the fibre, and thus the optical power coupled through the misalignment will be altered. Similar effects also occur if source frequency is changed, as is observed at the beginning of semiconductor laser pulses. This alteration in coupled power is termed modal noise and may cause significant deterioration in the error rate of a digital system, and catastrophically large amplitude variations in analogue systems.

This letter proposes a technique whereby a connector may be designed to minimise noise due to misalignment. This is effected by reducing the actual possible shift in the mode pattern which may be induced by mechanical variations acting on the fibre. There are, of course, other techniques for reducing modal noise, namely increasing the fibre dispersion or increasing the source linewidth. However, there are other penalties to pay for such a solution, mainly concerned with the eventual system bandwidth.

Principles of connector design: The principle of the fibre connector design is based on the observation that modal noise has not, as yet, been observed on systems using incoherent sources.