SESSION XIII: Charge-Coupled Devices and Applications

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THPM 13.1: Charge Transfer in Buried-Channel Charge-Coupled Devices*

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PREVIOUS THEORETICAL work[1-12] on the operation of change transfer devices has focused upon surface charge-coupled devices and integrated circuit versions of the bucket-brigade shift registers. Another type of charge transfer device, namely buried-channel charge-coupled devices[13], is known to have several advantages over the former two devices. However, up to the present, only a static two-dimensional model[14-15] of buried-channel charge-coupled devices has been considered. The static model has not been incorporated in dynamic charge transfer description, and, consequently, our understanding of the device operation has been quite qualitative.

In this paper the results of a detailed numerical simulation of the charge transfer process in an overlapping gate buried channel CCD[16] will be presented. The general set of partial differential equations describing charge transfer and the electrostatic potential are reduced to a set of two partial differential equations involving a single spatial dimension and the time. To accomplish this a simple capacitance network model[17] has been used to reduce the appropriate two dimensional Poisson's equation into a second-order differential equation in a single spatial dimension. The resulting equation relates the signal charge and the minimum channel potential under all the relevant electrodes and interelectrode regions. A diffusion equation describing the charge transfer is coupled to this equation. The resulting coupled differential equations have been solved numerically by a modified box scheme[18].

It is shown that the charge-transfer process in buried-channel CCD devices can be divided into three distinct stages similar to surface channel; Figure 1. In the first stage, the charge is confined under the source storage gate and spreads itself according to the rapidly changing clock voltages. During the second stage, the charge transfer occurs in a manner analogous to the operation of a buried channel IGFET[19]. The storage electrodes act as source and drain, and the transfer electrode acts as the control gate. In the final stage, the charge transfer process is characterized by transfer induced by the relatively large fringing fields. The residual charge decays exponentially

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with a final characteristic time constant of the order of a nanosecond; Figure 2[11].

In light of these reliable numerical results, the entire charge transfer process has been reviewed analytically. Approximate analytic expressions for the charge-transfer efficiency which are sufficiently accurate to be used in optimizing CCD array design with respect to voltage waveform and clocking scheme will be presented.

The numerical results for the charge transfer in the buried channel CCD are presented as a motion picture which illustrates graphically the distinct features in the operation of a buried channel CCD, under several clocking schemes.

Figure 1*(a)* plots the minimum potential, charge profile and current density at t = 0.221 ns. At t = 0, the transfer and drain gate voltages start dropping to the final value (-12 V) from the initial value (8 V). The plot is shown at the gate voltages of -10 V. The barrier and source gate voltages are set to be 8 V throughout the transfer process.

Charge is normalized by 935 electron charges/μ^2. Sheet current density is normalized by 23.4 electron charges/μ•ns. The length L of one unit cell of the device is 48 μ consisting of two polysilicon gates and two aluminum gates.

In Figure 1*(b)*, t = 0.443 ns. Note the current density under the transfer gate is almost constant. The charge transfer in this stage can be described quite accurately by buried channel IGFET[19].

In Figure 1*(c)*, t = 1.05 ns. Note the slope of the current density indicates that the net charge under the transfer gate is still decreasing. The charge transfer in this final stage is characterized by the powerful field-aided transfer[11].

In Figure 2 (top), sheet current density is normalized by 23.4 electron charges/μ•ns. Time is normalized by t = (0.001) L^2/D = 1.92 ns with L = 48 μ and D = 12 cm^2/s. The lines (a), (b), and (c) present the net charging, charging and discharging of the transfer gates,respectively.

In Figure 2 (bottom), charge is shown as a percentage of the total signal charge of 45,000 electron charges/μ. The lines (a), (b), and (c) represent the total residual charge under the source and transfer gates, the charge under the source gate, and the charge under the transfer gate respectively. Note the lines eventually become straight, implying the exponential decay characteristics of the powerful field-aided transfer. The final slope (hence, the characteristic time constant) is 0.765 ns for lines (a) and (c), and 0.165 ns for line (b).

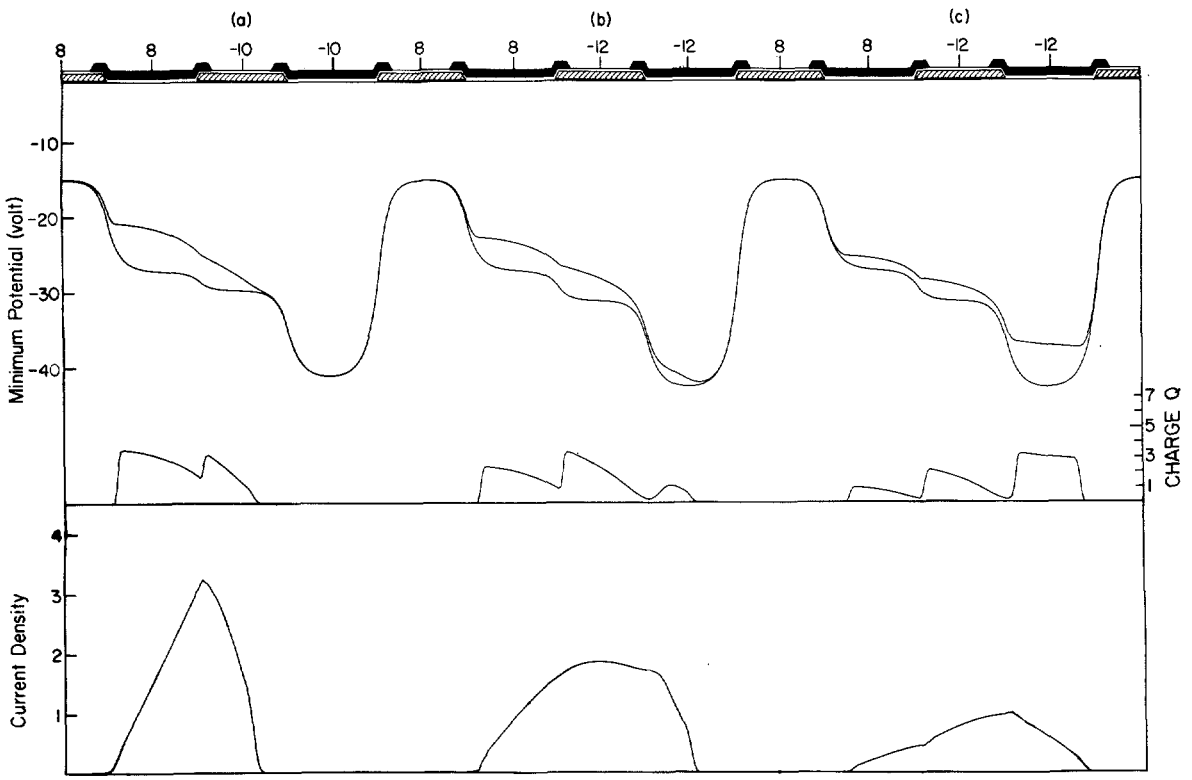

FIGURE 1—Plots of the minimum potential; charge profile and current density at different stages of the charge transfer.

[See page 245 for Figure 2.]

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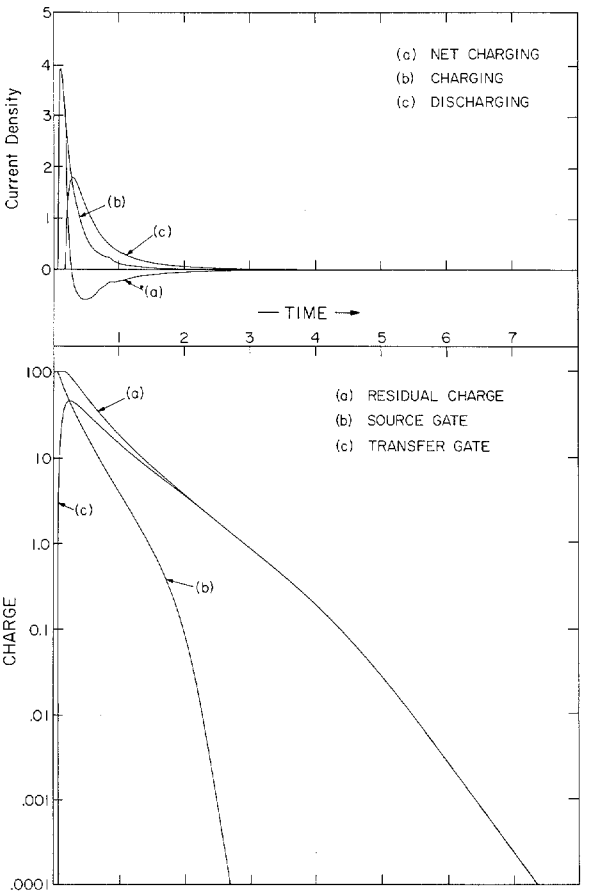

FIGURE 2—Current density and remaining charge as functions of time.

A Wideband Low-Noise Analog Delay Line

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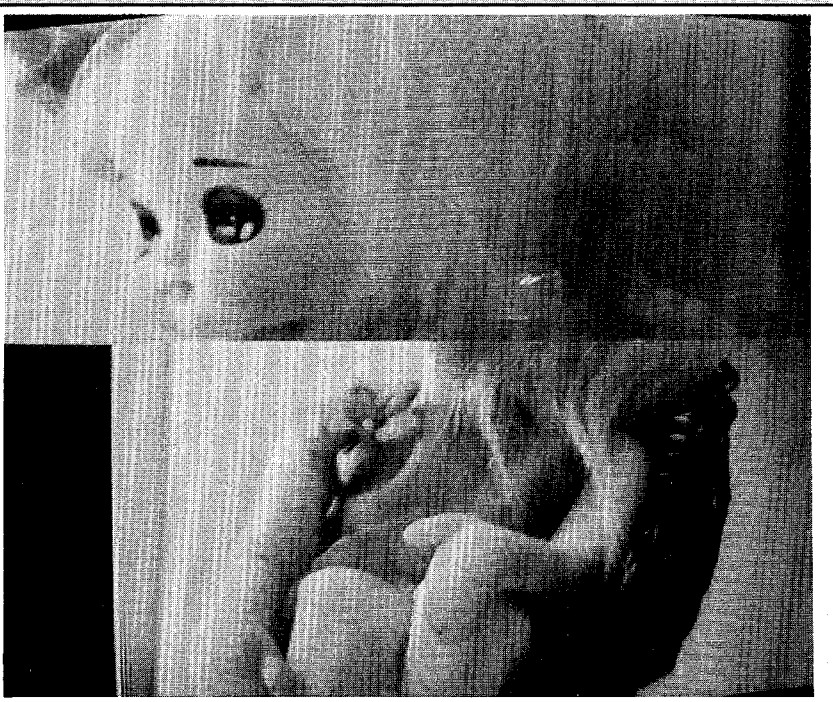

FIGURE 5—A B/W commercial TV image (lower portion) delayed through the 128-bit array; f = 12 MHz, V = 10 V.