where the probability-density function of β is:

$$p(\beta) = \frac{1}{B} \exp(-\beta/B) \qquad 0 < \beta < \infty$$

where B denotes the second moment of the channel gain. This average error probability is minimised, subject to the rate constraint

$$\bar{r} = \int_0^\infty r(\beta)\, p(\beta)\, d\beta = 1 \quad \ldots\ldots\ldots \quad (2)$$

by adjoining eqns. 1 and 2 with a Lagrange multiplier λ, and setting

$$\frac{\partial \bar{P}_e}{\partial r(\beta)} + \lambda \frac{\partial \bar{r}}{\partial r(\beta)} = 0$$

and solving for λ, using eqn. 2. This leads to

$$r(\beta)\frac{\partial P_e}{\partial r(\beta)} + P_e + \lambda = 0 \quad \ldots\ldots\ldots \quad (3)$$

Examination of the error probabilities[2] for noncoherent and coherent a.s.k., f.s.k. and coherent and differentially coherent p.s.k. systems reveals that the first term on the left-hand side of eqn. 3 is of the form

$$r(\beta)\frac{\partial P_e}{\partial r(\beta)} = g[P\beta/N_0 R_{av} r(\beta)]$$

where the actual dependence of $g[\cdot]$ depends on the system under consideration. Thus, eqn. 3 may be rewritten as:

$$g[P\beta/N_0 R_{av} r(\beta)] + f[P\beta/N_0 R_{av} r(\beta)] = \text{constant}$$

which has the solution

$$r(\beta) = k\beta \quad \ldots\ldots\ldots\ldots\ldots \quad (4)$$

where $k = 1/B$, from eqn. 2. Use of eqn. 4 in eqn. 1 yields

$$\bar{P}_e = f(PB/N_0 R_{av})$$

It is observed that this is exactly the error probability of a straight system operating in a steady channel with the same energy/noise ratio.

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OVERLAPPING-GATE BURIED-CHANNEL CHARGE-COUPLED DEVICES

Indexing term: Charge-coupled devices

In this letter the advantages of the overlapping-gate buried-channel charged-coupled devices over the 3-phase metal-gate and resistive-gate buried-channel c.c.d. are discussed and pertinent design considerations for the overlapping-gate c.c.d.s are presented.

The two levels of metallisation technologies have provided a desirable realisation of surface-channel charge-coupled devices (c.c.d.s) with overlapping gates; this letter describes overlapping-gates buried-channel charge-coupled device structures. Pertinent design considerations for such buried-channel structures are discussed.

One of the major factors causing the buried-channel device[1] to differ from the surface-channel device[2] is illustrated by the relationship of the gate–oxide capacitance to the depth of the potential well produced by that gate. Given two identical gate electrodes at the same potential, in a surface-channel device the gate with the larger oxide capacitance will produce the deeper well at the interface. In a buried-channel device, the gate with the smaller oxide capacitance will produce the deeper well in the depleted channel. This argument may be used to show that the effect of a gap between adjacent electrodes is quite different for a buried-channel than for a surface-channel device. In a buried channel c.c.d., the effective channel capacitance under the gaps is very small, and very deep potential wells result. These undesirable potential wells in buried-channel devices tend to interfere with the potential wells under the gate electrodes, which consequently cannot properly control the storage and transfer of charge. Better control of the interelectrode gaps can be achieved by resistive-gate structures,[3] or by using undercut isolation[4] or overlapping-gate techniques which have been developed for surface c.c.d.s.[5] Resistive-gate devices help, but

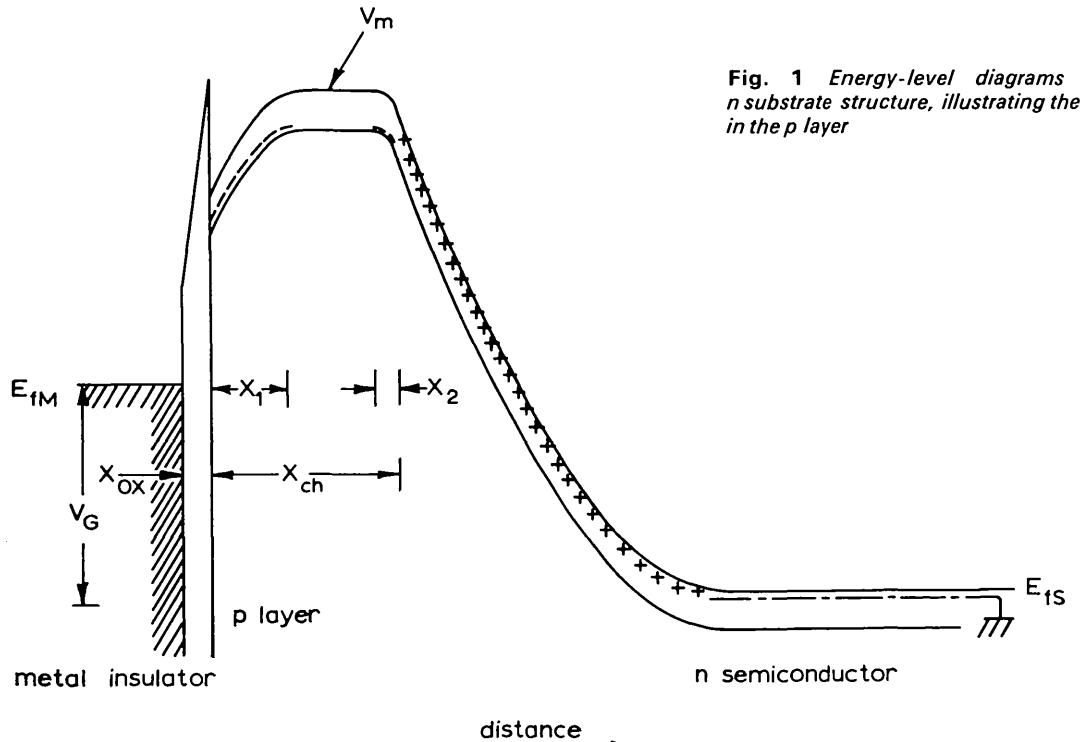


Fig. 1 *Energy-level diagrams of a metal–oxide p layer n substrate structure, illustrating the formation of a potential well in the p layer*

they are limited by relatively slow charging of the high-resistance regions. On the other hand, overlapping-gate structures provide a very simple way to reduce gaps to within an oxide thickness.

The energy-band diagrams of a metal–SiO_2–p–n structure are shown in Fig. 1. The p layer is partially filled with majority carriers and the n substrate is at ground potential. Assuming a uniform doping concentration N_A in the p layer, the solution of the 1-dimensional Poisson's equation, using the standard depletion approximation, gives:

$$V_M = V_G - \phi_{MS} - \frac{eN_A X_1^2}{2\varepsilon_S} - \left(\frac{eN_A X_1}{C_0} - \frac{Q_{ss}}{C_0}\right) \quad (1a)$$

$$E_S = \frac{eN_A X_1}{\varepsilon_s} \quad (1b)$$

$$Q_B = eN_A(X_{ch} - X_1 - X_2) \quad (1c)$$

$$X_2 = \sqrt{\left(\frac{N_D 2\varepsilon_s(V_M + V_D)}{N_A e(N_D + N_A)}\right)} \quad (1d)$$

where ϕ_{MS} is the work-function difference between the gate electrode and the p layer, Q_{ss} is the fixed interface charge, C_0 is the oxide capacitance, N_D is the donor concentration of the substrate, e is the electronic charge, ε_s is the dielectric constant of silicon, V_D is the built-in voltage of the p–n junction and Q_B is the mobile majority-carrier concentration per unit area in the buried channel. The other symbols are defined in Fig. 1.

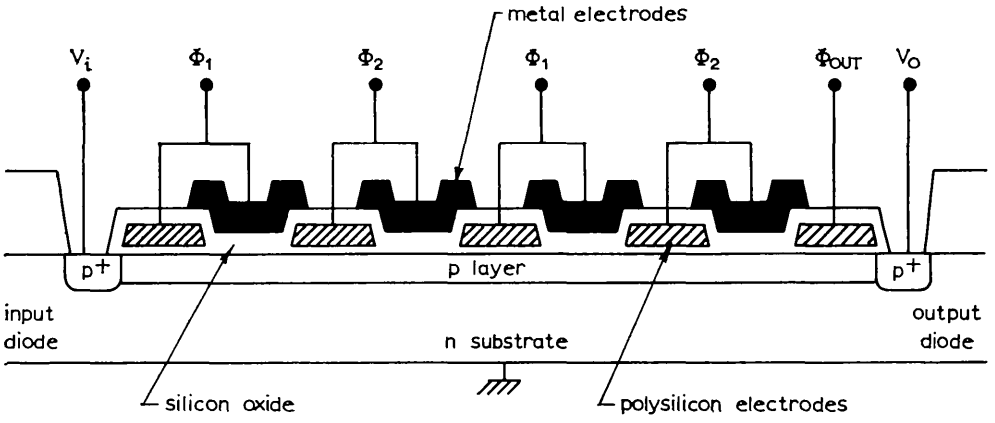
From eqns. 1a–1d, it can be shown that, in the buried-channel c.c.d., the maximum signal charge Q_{BMAX} is limited by avalanche breakdown at the silicon surface. In surface c.c.d.s, the maximum signal charge Q_{SMAX} is physically limited by the breakdown in the silicon oxide. It can be also shown that, for the same clock-voltage swing, the ratio R of the maximum signal charge that can be stored in the surface c.c.d. to that in the buried-channel c.c.d. is given, approximately, by

$$R = 1 + \frac{C_0}{2\varepsilon_S/X_{ch}} = 1 + \frac{\varepsilon_0 X_{ch}}{2\varepsilon_S X_{0x}} \quad (2)$$

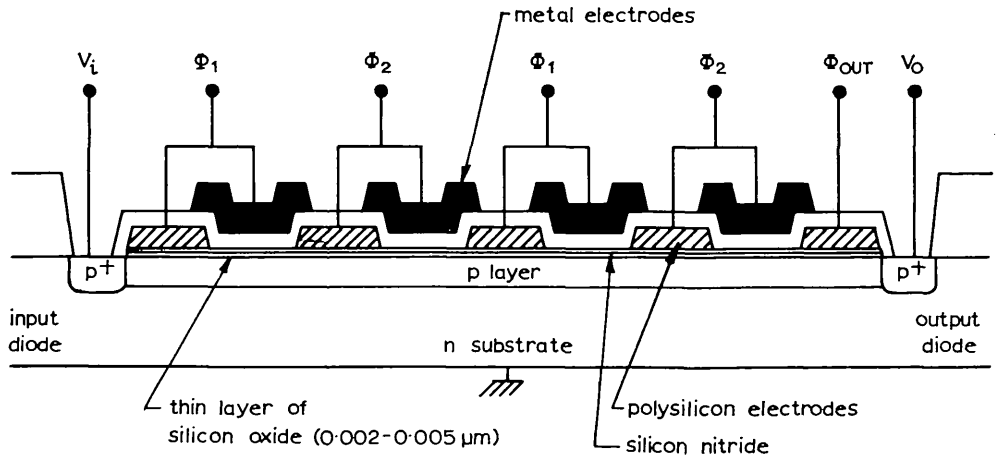
where X_{0x} is the oxide thickness and ε_0 is the oxide relative permittivity (typically, $X_{ch} = 1\ \mu m$, $R \simeq 2{\cdot}5$).

In a buried-channel c.c.d., the signal charge packets can be stored and transferred in the buried channel without interacting with the interface states; and while some trapping can occur in bulk-defect states, this latter effect is usually much smaller.[6] In addition, the larger fringing fields and the higher carrier mobility in the buried channel lead to more efficient charge transfer at all frequencies. Thus the signal degradation, owing to incomplete charge transfer, is considerably reduced in the buried-channel c.c.d. Also, larger signal dynamic range and signal/noise ratio are expected. However, in buried-channel c.c.d.s, the entire insulator–semiconductor interface is always depleted of carriers; hence, the interface-states generation currents are larger than in surface c.c.d.s. Thus, in the buried-channel c.c.d., the maximum delay time is smaller.

In Figs. 2a and 2b, structures of buried-channel c.c.d.s with overlapping gates are shown. The buried p channel is usually achieved by ion implantation. The electrode separation in these structures is reduced to an oxide thickness. Thus the effective channel capacitance in the interelectrode regions



a



b

Fig. 2 *Structure of the overlapping-gate buried-channel charge-coupled devices*
a Single dielectric layer
b Double dielectric layer

is defined by the oxide capacitance, and the active channel is sealed from any external ion contaminations and instabilities. The minimum potential V_m in the depleted buried channel under the interelectrodes regions varies uniformly from under one electrode to another, and can follow the rapid variation of the clock voltages.

In Fig. 2*a*, the asymmetry in the potential wells is due to the different oxide thickness under the polysilicon and aluminum electrodes (for silicon-gate technology). According to eqn. 1*a*, the difference between the minimum potential under the aluminium electrodes, V_{mAl}, and the polysilicon electrodes, V_{mSi}, in the depleted buried channel is approximately given by

$$V_{MAl} - V_{MSi} = -(eN_A X_{ch} - Q_{ss})\left(\frac{1}{C_{OAl}} - \frac{1}{C_{OSi}}\right) \quad (3)$$

where C_{OAl} and C_{OSi} are the oxide capacitances under the aluminum and polysilicon gates, respectively. Since $C_{OAl} < C_{OSi}$ and $(eN_A X_{ch}) > Q_{ss}$, the deeper potential wells are under the aluminum electrodes.

A second ion-implantation step could be used, after the definition of the polysilicon electrodes, to selectively implant under the aluminum electrodes. If both implants are of the same type, the maximum signal charge that can be transferred is increased, resulting in a larger signal dynamic range and better charge-transfer characteristics. But, if the second implant is of opposite type, the polysilicon electrodes could then be used as storage gates and aluminum electrodes as transfer gates. In Fig. 2*b*, a double dielectric layer is incorporated over the active channel. The charge-storage properties of the double-dielectric structure can be used, in this case, to modify the effective interface charge under the aluminum and polysilicon electrodes, so as to increase the maximum signal charge that can be transferred.

In conclusion, we have presented structures for overlapping-gate buried-channel charge-coupled devices. We have shown that these structures have several advantages, and therefore are the most promising technically for the large-scale applications of buried-channel charge-coupled devices.

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REDUCTION OF NOISE IN HIGH-POWER CROSSED-FIELD AMPLIFIERS

Indexing terms: Travelling-wave tubes, Noise, Electron guns, Magnetic-field effects

The letter describes a method of reducing the broadband noise of a high-power injected-beam crossed-field amplifier by means of a nonuniform magnetic field in the electron-gun region. The noise reduction achieved is some tens of decibels, and also results in improvements in other characteristics of the tube.

The spontaneous generation of broadband noise at a level many tens of decibels in excess of shot noise has always been a characteristic feature of high-power crossed-field electron tubes. The phenomenon has hitherto prevented full realisation of the high gain combined with high efficiency predicted for the injected-beam crossed-field amplifier.[1] With careful suppression of electromagnetic feedback, useful performance has been achieved.[2] However, at gains in excess of about 17 dB, broadband noise reaches an unacceptable level, and is accompanied by other abnormal phenomena, making the tube difficult to use.

Many authors have described investigations into the origins of this excess noise in crossed-field devices, but their conclusions have been mainly negative.[3, 4] The main source of noise is believed to be located in the vicinity of the potential minimum adjacent to the space-charge-limited cathode. This view is supported by more recent cathode-tilting experiments,[5] in which a tilt of a few degrees was found to reduce the noise by some tens of decibels.

The experiments to be described were carried out using an experimental linear-format amplifier with pulse operation. The gun* was of the type described by Kino,[6] but truncated at the exit edge of the cathode, giving an abrupt entry into the interaction space. The cathode length was 30 mm, giving a normalised length of about 1500, using Kino's normalisation. The slow-wave circuit, giving a phase velocity of $c/8$, had a length of 4·4 slow wavelengths and an impedance of 70 Ω. It was coupled at each end to an external coaxial line by a matched transition, and the circuit attenuation was less than 1 dB. The sole-line distance was 6 mm, and the frequency was 3 GHz.

In a preliminary group of experiments, the effect of tilting the electron gun in a uniform magnetic field was explored. The electron beam was much more powerful than that described in the published work.[5] The optimum tilt was found to be about 1°, with the result shown in Fig. 1, where signal/noise ratio is plotted against the power of the r.f.-input signal. The optimum tilt was about an axis which resulted in a

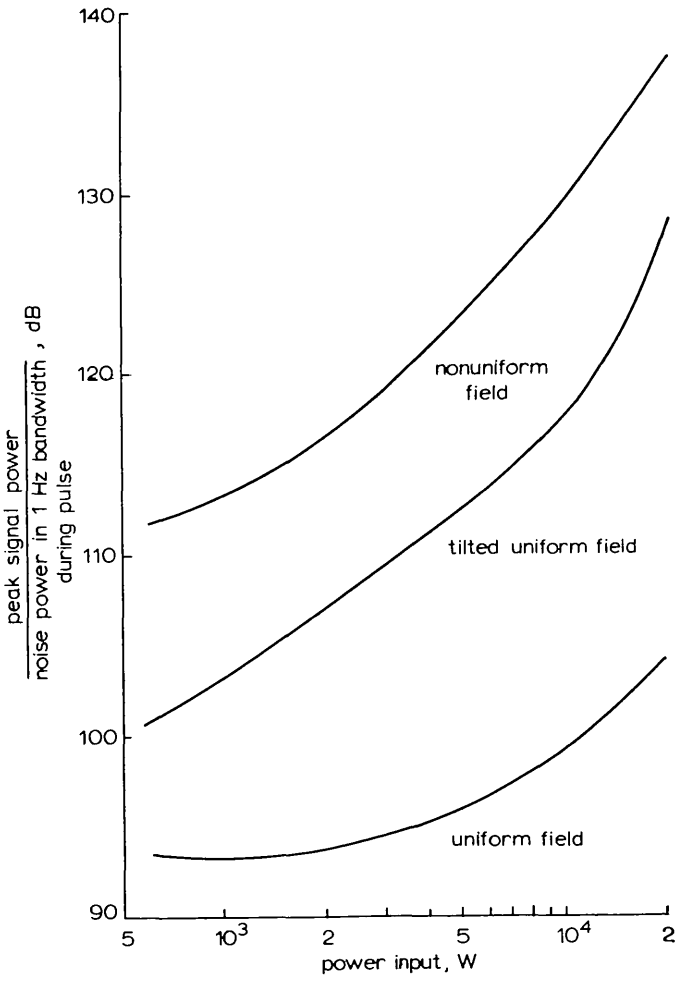

Fig. 1 *Effect of tilt and nonuniformity on signal/noise ratio*
Magnetic field = 0·161 T
Beam current = 10 A
Beam power = 250 kW

* The tube used in these experiments was manufactured by the M–O Valve Co.