

FAST NEURAL ALGORITHMS FOR DETECTING MOVING TARGETS IN HIGHLY NOISY ENVIRONMENTS

Jacob Barhen^{1,2}, Nikzad Toomarian¹, Michail Zak¹

California Institute of Technology
Pasadena, CA 91109

ABSTRACT

The detection of targets moving in an environment dominated by “noise” is addressed from the perspective of nonlinear dynamics. Sensor data are used to drive a Korteweg-deVries (soliton) equation, inducing a resonance-type phenomenon which indicates the presence of hidden target signals. The algorithm is implemented in terms of a novel neural architecture, which we have named “spectral network”, which can easily be implemented in optoelectronic hardware.

Key Words: target detection, driven solitons, spectral neural networks, optoelectronic implementation.

1. INTRODUCTION

Long-range detection of the motion of a target in an environment dominated by noise and clutter is a formidable challenge. Target detection problems are generally addressed from the perspective of the theory of statistical hypothesis testing[1]. So far, existing methodologies usually fail when the signal-to-noise ratio, in dB units, becomes negative, notwithstanding the sophisticated but complex computational schemes involved. In this paper, we propose to explore the possibility of using the phenomenology of nonlinear dynamics, not only to filter out the noise, but also to provide precise indication on the position and velocity of the target. Specifically, we introduce a new class of neural networks, to be referred to as “spectral” networks, which exhibit a remarkable spatial organization, and yield a dramatic enhancement of the signal to noise ratio. Rapid advances in analog VLSI technology in general, and in charge domain computing in particular, provide a strong incentive to implement the corresponding neural algorithms in electronic circuit architectures, to achieve unprecedented levels of performance for this hard signal processing problem.

2. SPECTRAL NETWORKS

To simplify the discussion, and with no loss of generality, we will consider in the sequel only motion in \mathfrak{R}^1 space. We have carried out the following computational experiment. An array of N motion-detector “neurons” is fed signals from an array of N sensors. Both arrays are linear, with equally spaced elements. Let $u_n(t)$ denote the temporal response of the n -th neuron. We will

⁽¹⁾ Jet Propulsion Laboratory, MS 303/310, 4800 Oak Grove Dr., Pasadena, CA 91109, USA. Phone (818)354-9218, FAX (818)393-5013; ⁽²⁾ Applied Physics Department, MS 128-95, Pasadena, CA 91125, USA

assume that two overlapping synaptic arrays, \mathbf{T}^c and \mathbf{T}^d , fully interconnect the network, which obeys the following system of coupled nonlinear differential equations

$$\dot{u}_n(t) = -asu_n(t) \sum_m T_{nm}^c u_m(t) - bs^3 \sum_m T_{nm}^d u_m(t) + S_n(t) \quad (1)$$

The nomenclature is as follows. Spatial organization will be considered over the interval $[0, 2\pi]$. The scaling factor $s = \pi/L$ relates the spatial variable $^s x$ in the detection interval $[-L, +L]$ to the spatial variable x in the computational interval via

$$x = s \quad [^s x + L] \quad (2)$$

The actual positions of neurons and sensors are given by the discrete values $x_n = n \Delta_x$ ($n = 0, \dots, N - 1$), with resolution $\Delta_x = 2\pi/N$. Thus, $u(x_n, t)$ is written as $u_n(t)$. For convenience, we will assume that N is even. The sensor inputs to the network are denoted by $S_n(t)$. Finally, a and b are constants, specified at the numerical implementation stage.

A critical feature of this novel neural network architecture is the form taken by the synaptic interconnections. The matrices \mathbf{T}^c and \mathbf{T}^d are defined as

$$\mathbf{T}^c \mathbf{u} = F^{-1} \{i\mathbf{k} * F[\mathbf{u}]\} \quad (3)$$

and

$$\mathbf{T}^d \mathbf{u} = F^{-1} \{-i\mathbf{k}^3 * F[\mathbf{u}]\} \quad (4)$$

In the above expressions, the symbol $*$ denotes the Schur-Hadamard product of the two $N \times 1$ matrices, while F and F^{-1} refer to the forward and inverse Fourier transforms. The matrix \mathbf{k} captures the spectral resolution. Initial conditions for the network are defined as $u_n(0) = 0$, for all neurons.

3. SIMULATIONS

The results of the experiment are illustrated in Figures 1-3. Each figure includes four plots. The lower left corner shows the sensors input to the network. Since data are simulated, the contributions from the target and background noise are plotted separately, for illustrative purposes, eventhough the network actually receives only their combined value. The Fourier spectrum of the total signal is given in the upper left corner. The network's output is plotted in the lower right corner. Finally, the solution in absence of noise is shown in the upper right side.

The results are plotted after 10 time steps (using $\Delta_t = 0.005$), and were obtained using a 64-element sensor array. Figure 1 indicates that when only noise is fed to the network, no spurious result emerges. Figure 2 illustrates the spectral network's detection capability for a target moving in a noise and clutter background characterized by a per pulse signal-to-noise (SNR) ratio of approximately -0dB. Conventional detection methods usually reach their breaking point in the neighborhood of such SNR ratios[2]. Finally, Figure 3 presents results for a case where the SNR drops below -10dB. We would like to emphasize that the above SNR is by no way the limit of our procedure, as can be inferred from the still excellent quality of the detection peak. Furthermore, multiple layers of the spectral neural architecture provide a "space-time" tradeoff for additional enhancement. Next, we attempt to provide a physical explanation of the detection phenomenon.

4. NEURAL NETWORKS WITH SPATIAL ORGANIZATION AND SOLITON DYNAMICS

Passing to the limit $\Delta_x \rightarrow 0$, we see that Eq. (1) can be rewritten in terms of the state variable $u(x, t)$ as

$$u_t + a u u_x + b u_{xxx} = S \quad (5)$$

where u_t and u_x denote partial derivatives with respect to time and space. If we select the constants a and b as taking the values 6 and 1 respectively, we recognize the left hand side of Eq. (5) as the Korteweg-de Vries (KdV) equation.

The discovery of solitons[3] - nonlinear solitary wave solutions to the KdV equation - has enabled many advances in areas such as plasma physics or fluid dynamics. The computational experiment described in this note reports on a new property for a *forced* KdV equation, namely its exploitation for information processing.

Applications of nonlinear dynamics phenomenology for information processing is a relatively new field. So far, the most powerful tools developed have been associated with finite-dimensional dissipative nonlinear dynamical systems, and, in particular, with the concept of attractors. Surprisingly, the driven KdV equation (which is non-dissipative) is found to possess a remarkable property: it allows one to detect a uniformly moving target in a noisy background.

How can we interpret the observed detection phenomenon? Let us assume that the sensor input to the network consists of two parts: (1) $\eta(x, t)$, space-dependent random oscillations; and (2) a "target" $\theta(x, t)$, the value of which is nonzero only over a few "pixels" of the sensor array. Notice that, since the KdV equations are non dissipative, and energy is pumped into the system via the $S(x, t)$ term, active steps have to be taken to avoid unbounded growth of the solutions. Furthermore, if we denote by v the target's velocity, we have

$$\theta(x, t) = \theta(x - vt) \quad (6)$$

Thus, based upon the properties of the usual (i.e., homogeneous) KdV equation[4], we postulate that the target signal $\theta(x, t)$ "resonates" with the "eigen-solitons" of the homogeneous equation. Hence, it will be amplified, while the random components $\eta(x, t)$ will be dispersed. Furthermore, such a "resonance" should not depend on the target velocity, since the velocity of the "eigen-solitons" of the KdV equations are not prescribed. In other words, the proposed methodology can detect targets over a wide range of velocities. This has been confirmed through our computer experiments.

5. ELECTRONIC HARDWARE IMPLEMENTATION

In the above mathematical development, a formalism was proposed for detecting moving objects deeply buried in clutter with negative signal-to-noise ratios. A set of coupled nonlinear differential equations was obtained, which describes how the state variables of the motion detector neurons respond and change with time under the influence of the external stimuli induced by

targets. This formalism can be cast into the “language” of electronic neural networks by straightforward extension. Essentially, one possible idea would be to model the set of coupled differential equations by considering the analogous electrical circuit whose currents or voltages obeys the same set of differential equations. Typically, the array of motion detector neurons could be implemented by operational amplifiers, with feedback or feedforward variable strength connecting circuits consisting of wires, resistors, and capacitors organized to represent the architecture of the spectral network. Large scale analog neuroprocessor architectures can be directly synthesized by tapping into a library of VLSI “building block” chips developed at JPL by the Neuroprocessing and Analog Computing Devices group[5,6]. These building block chips include a wide spectrum of cascable, programmable, synaptic and neuronal chips with tailorable functional characteristics. The template for the synaptic chips consists of a fully connected 32 x 32 array of variable strength connection elements fabricated using standard 2 micron bulk CMOS process. The synaptic connections vary from simple binary to fully analog designs with a dynamic range exceeding 11-bits of resolution. In addition, a variety of high speed neuron chips have been fabricated, designed specifically to provide nonlinear functional transfer characteristics. The template for this family of chips consists of a 32 x 1 linear array of devices. A typical system configuration is illustrated in Fig. 4.

Concomitantly to the JPL effort, charge domain VLSI circuits are being developed at Caltech to perform high speed vector-matrix multiplications[7-9]. The vector-matrix multiplier consists of a matrix of CCD cells having an architecture inspired by charge injection device (CID) imager pixels, in that one of the cell’s gates is connected vertically from cell to cell forming a column electrode, while another gate is connected horizontally forming a row electrode. The charge stored beneath the row and column gates encodes the matrix, with the column and row electrodes representing the input vector and the output vector, respectively. In its most basic configuration, shown in Fig. 5, such a circuit computes the product of a binary input vector and an analog matrix of charge. The computation done by each CCD cell in the matrix is a multiply-accumulate in which the charge, Q_{ij} , is multiplied by a binary input vector element, U_j , encoded on the column line and this product is summed with other products in the same row to form I_i . Multiplication by a binary number is equivalent to adding or not adding the charge at a particular matrix element to its associated row line. Since all column electrodes are pulsed at the same time, and the associated voltage changes are then capacitively summed on the row lines in parallel, the entire vector-matrix multiplication is accomplished in one clock cycle. Many improvements have been incorporated into this basic structure, the most important being the ability to handle digital (instead of binary) input with 2^n levels, and digital output using novel, compact A/D designs. A 256x256 element circuit is currently being fabricated, which is expected to exceed 10^{12} operations/second/bit of precision.

It is important to realize that a number of open problems must be addressed, before a reliable microelectronic implementation of our target detection algorithms can be achieved. For instance, how can the intrinsic computational speed of the existing, low precision (typically 10-12 bit) devices be practically “traded” for more accuracy in the calculations? Furthermore, since current neural hardware simply involves a basic matrix-vector multiplication scheme, only linear partial differential equations can, at this stage, be considered for implementation. Thus, more advanced architectures, enabling the modeling of nonlinear terms such as the expression $u_i \sum_j T_{ij} u_j$,

which appears in the KdV equations, must be developed.

6. TARGET TRACKING

To provide precise indication on the position and velocity of the targets, one can build upon a unique new methodology we recently developed for supervised neural learning of time dependent trajectories[10-11]. It exploits the concept of adjoint operators[12-13] and teacher forcing. The resulting algorithms enable computation of the gradient of an objective functional with respect to the various parameters of the network architecture in a highly efficient manner. Specifically, it combines the advantage of dramatic reductions in computational complexity inherent in adjoint methods, with the ability to solve the equations forward in time. Not only is a large amount of computation and storage saved, but the handling of real-time applications becomes also possible. Our preliminary results[13] show that learning time is reduced by one to two orders of magnitude in comparison to the best previously published results, while trajectory tracking is significantly improved. Our methodology also makes hardware implementation of temporal learning very attractive.

7. CONCLUSIONS

A novel neural architecture, named "spectral network" is being proposed for detecting targets in motion in a cluttered background. In preliminary computer experiments, the method has proven successful at very negative signal-to-noise ratios, and over a wide range of target velocities. Results can be interpreted in terms of resonances in driven KdV equations. As a corollary, we have proposed a framework for solving an important class of partial differential equations efficiently using novel neural network architectures, which can easily be implemented in hardware.

8. ACKNOWLEDGMENTS

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology. Support for the work came from the Naval Weapons Center, China Lake, California, through an agreement with the National Aeronautics and Space Administration. We thank A. Agranat, C. Neugebauer and A. Yariv (Caltech), as well as R. Tawel and A. Thakoor (JPL) for enlightening discussions concerning possible hardware implementation of our algorithms.

9. REFERENCES

1. Whalen, A.C., *Detection of Signals in Noise*, Academic Press, New York (1971).
2. Levanon, N., *Radar Principles*, Fig. 3.4, p. 44, Wiley Interscience, New York (1988).
3. Drazin, P.G., et al., *Solitons*, Cambridge University Press, London UK (1986).
4. Zak, M., "Neurodynamics with Spatial Self-Organization", *Biol. Cybern.*, *65*, 121-127 (1991).
5. Eberhardt, S.P., Duong, T., and Thakoor, A.P., "Design of Parallel Hardware Neural Network Systems from Custom Analog VLSI Building Block Chips", *Proceedings of the International Joint Conference on Neural Networks*, pp. 183-190, IEEE Press 1989.

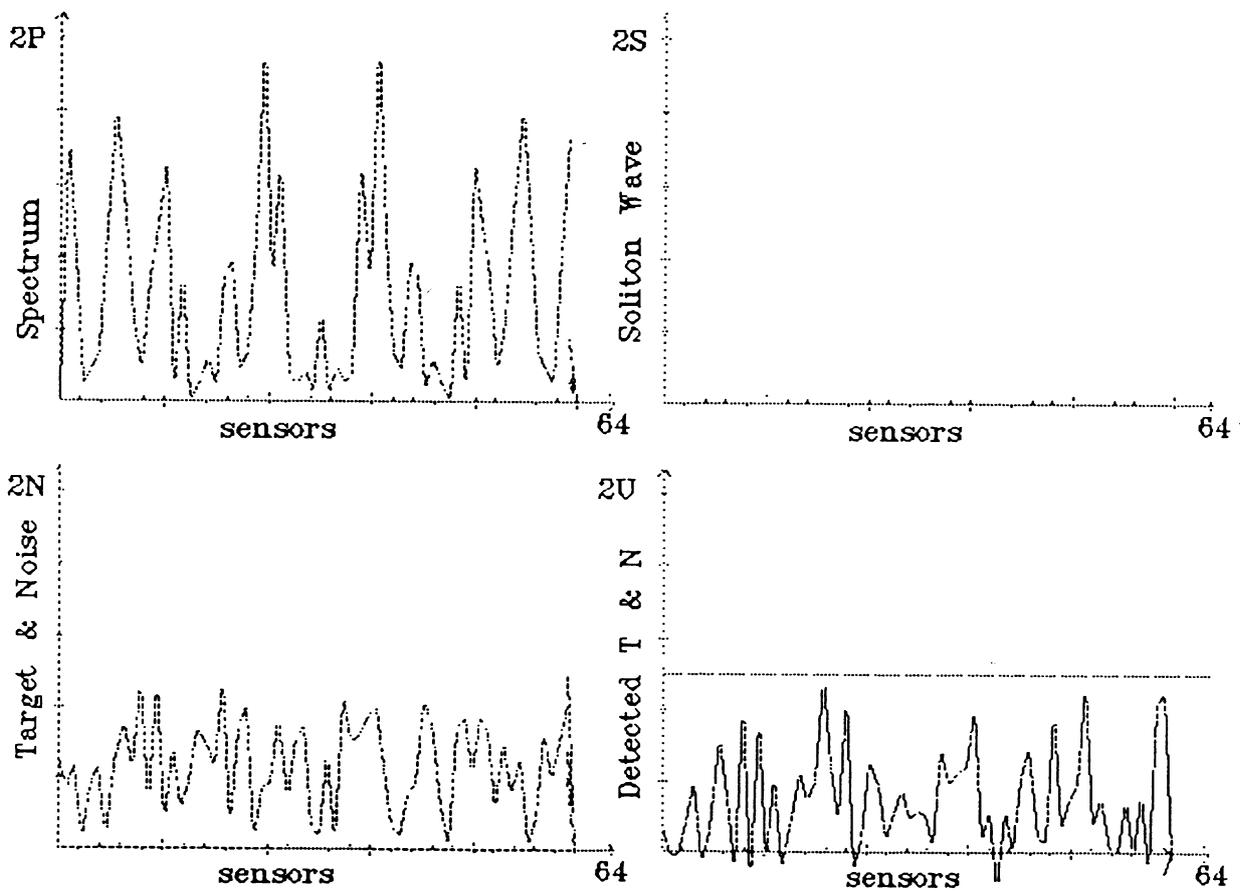


Figure 1. Spectral Network Response: Input is space-dependent noise only (no target)

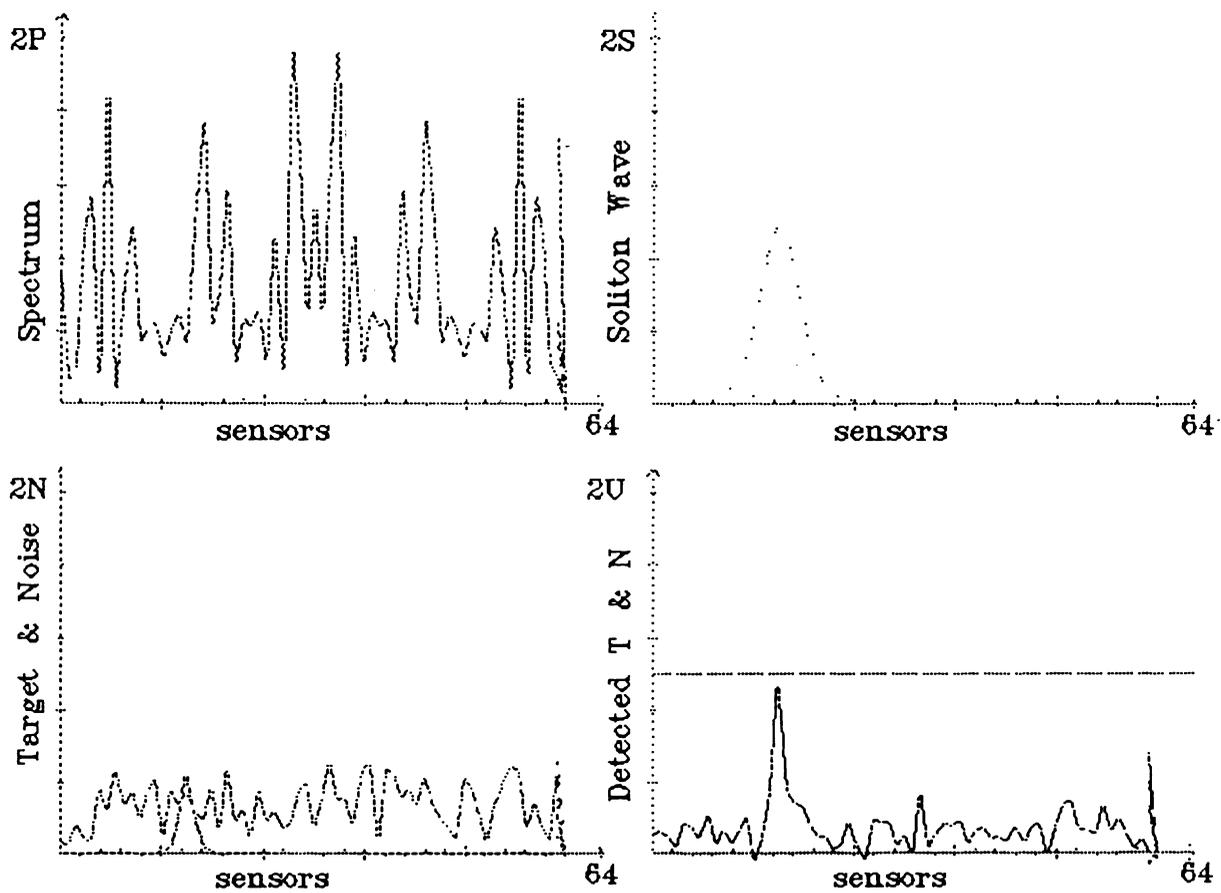


Figure 2. Spectral Network Response: Target Detection at $\text{SNR} \approx -0\text{dB}$

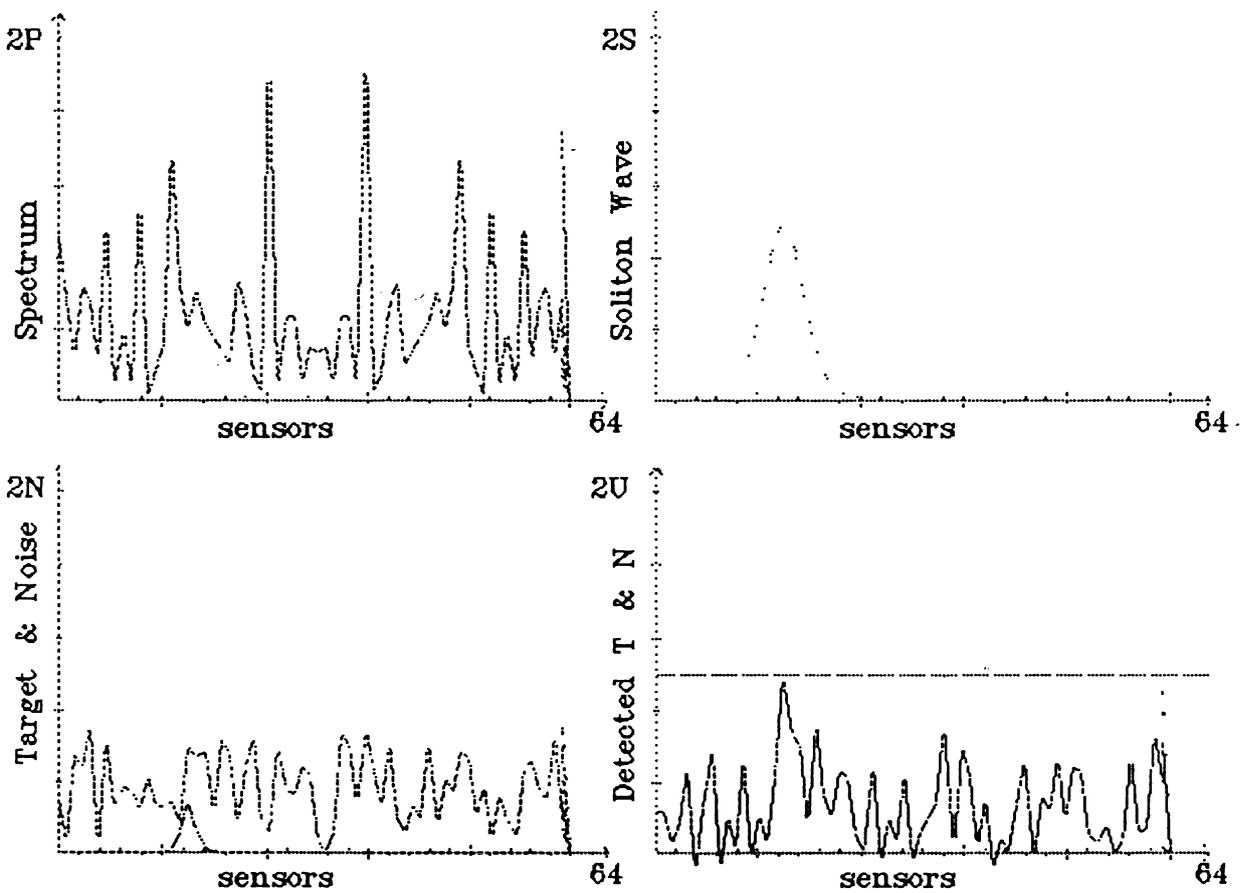


Figure 3. Spectral Network Response: Target Detection at $\text{SNR} \approx -10\text{dB}$

NEURAL ANALOG NETWORK BOARD (BASIC CONFIGURATION)

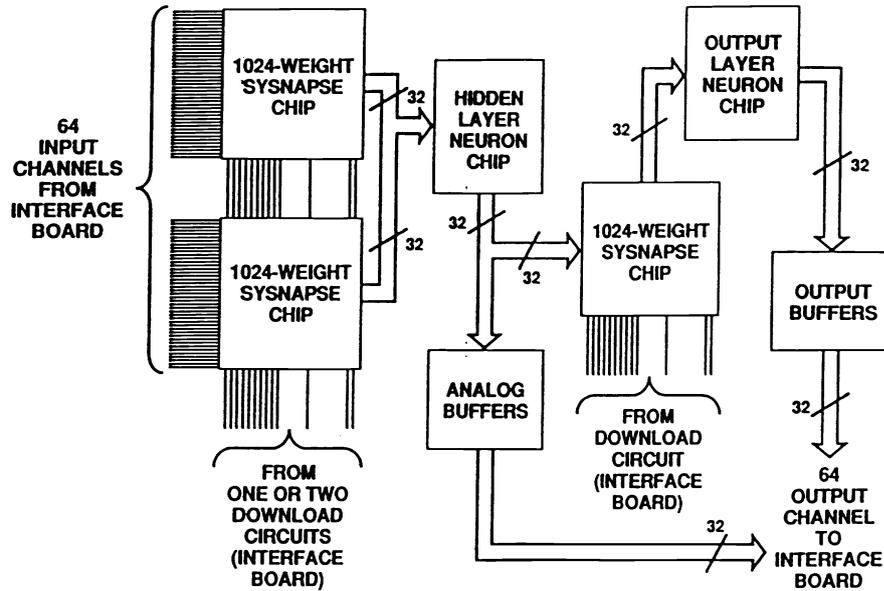


Figure 4. Neural Analog Network Board: basic configuration
(Courtesy: A. Thakoor, JPL)

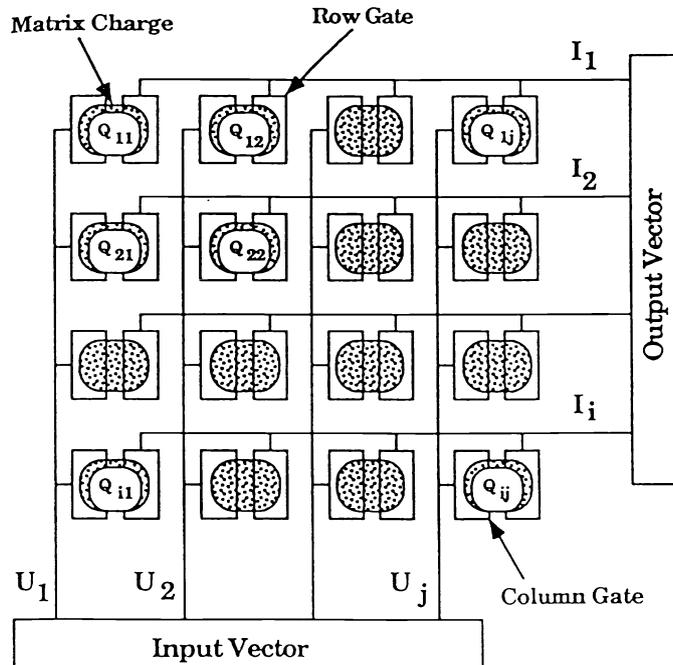


Figure 5. The CID architecture consists of an array of CCD elements that are connected together by row and column electrodes. The matrix values are encoded as charge packets that sit underneath these gates in the silicon substrate. The computation occurs when the charges are transferred from the column gates to the row gates which perform a capacitive sum operation. (Courtesy, C. Neugebauer, Caltech).

6. Eberhardt, S.P., Daud, T., Kerns, D.A., Brown, T.X., and Thakoor, A.P., "Competitive Neural Architecture for Hardware Solution to the Assignment Problem", *Neural Networks*, 4, 431-442, 1991.
7. Agranat, A., Neugebauer, C.F., Nelson, R.D., and Yariv, A., "The CCD Neural Processor: A Neural Integrated Circuit with 65 536 Programmable Analog Synapses", *IEEE Trans. Circ. Syst.*, 37, 1073-1075 (1990).
8. Neugebauer, C.F., and Yariv, A., "A Parallel Analog CCD/CMOS Neural Network IC", Proceedings IEEE International Joint Conference on Neural Networks, pp. 447-451, IEEE Press (1991).
9. Neugebauer, C.F., Agranat, A., Yariv, A., and Barhen, J., "A High Speed Linear Algebra VLSI Engine", in preparation (1991).
10. Barhen, J., Toomarian, N. and Gulati, S., "Adjoint Operator Algorithms for Faster Learning in Dynamical Neural Networks", *Advances in Neural Information Processing Systems*, 2, 498-508 (1990).
11. Barhen, J., Toomarian, N. and Gulati, S., "Application of Adjoint Operators to Neural Learning", *Applied Mathematics Letters*, 3 (3) , 13-18 (1990).
12. Toomarian, N. and Barhen, J., "Adjoint Operators and Non-Adiabatic Algorithms in Neural Networks", *Applied Mathematics Letters*, 4 (2), 69-73 (1991).
13. Toomarian, N. and Barhen, J., "Learning a Trajectory Using Adjoint Functions and Teacher Forcing", *Neural Networks*, in press (1991).