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Through-Silicon-Vias (TSVs) for 3D readout of ASIC for nearly gapless CdZnTe detector arrays

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ABSTRACT

Wirebonds, although proven for space application and perceived necessary for hybrid sensors like CdZnTe (CZT) detectors, introduce assembly complexity and undesirable gaps between detector units. Thus, they pose a serious challenge in building a low cost large area detector. We are developing Through-Silicon Vias (TSVs) to make all connections (both power and data) through ASICs, which will eliminate wirebonds and enable simple direct flip-chip bonding between the ASIC and a substrate electronics layer. TSVs also enable a more compact layout of the ASIC, which reduces the inactive area of the detector plane, and thus enables nearly gaplessly tilable detector arrays. We demonstrate the first successful TSV implementation on ASICs used for CZT detectors onboard the Nuclear Spectroscopic Telescope Array (*NuSTAR*) mission as part of our program to develop large area CZT imagers for wide field coded aperture imaging.

Keywords: Coded-aperture imaging, X-ray survey, Gamma-ray Burst, CdZnTe detectors

1. INTRODUCTION

A large array of closely tiled CdZnTe (CZT) detectors equipped with high spatial resolution can open up a wide range of new applications. As part of our program to develop High Resolution Energetic X-ray Imager (*HREXI*), a wide-field hard X-ray coded-aperture telescope utilizing a large array of CZT detectors with fine pixels, we are developing a 12U CubeSat Engineering Model (*HREXI*-EM). *HREXI*-EM is designed to localize transient events such as Gamma-ray Bursts (GRBs) within 2 arcmin. It is a prototype for a next generation SmallSat hard X-ray survey telescope that can localize transient sources within 10 arcsec. Such high angular resolution would eliminate the need for additional refinement of source position using a soft X-ray telescope, which otherwise is required for timely follow-up studies of the source with other longer wavelength telescopes with a relatively narrow field of view [Grindlay et al, in prep.]. A constellation of low-cost SmallSat high resolution hard X-ray survey telescopes can image the entire sky all the time, which is ideal for the study of all classes of elusive transient events in the sky. A key to realize such a system is to develop an efficient detector architechure and a low-cost process to assemble a large array of closely tileable CZT detectors with high imaging resolution.

We have been developing a large array of high resolution CZT detectors through a series of balloon-borne high-altitude experiments, culminating in two flights of *ProtoEXIST1* and then *ProtoEXIST2* [1, 2, 3,

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4]. The latest experiment *ProtoEXIST2* utilized the front-end detector readout system used in the Nuclear Spectroscopic Telescope Array (*NuSTAR*), the first focusing hard X-ray telescope in space. Each focal plane of two telescopes onboard *NuSTAR* has a 2 x 2 array of CZT crystals for detecting hard X-rays (Fig. 1) [5], and signals from each 2 x 2 cm^2 CZT crystal are read out by an Application Specific Integrated Circuit (ASIC). The *NuSTAR* ASIC (NuASIC) can process signals of 1024 channels in a 32 x 32 array, matching the anode pixel pattern (600 µm pixel pitch) of each crystal. Each *NuSTAR* ASIC has 87 input and output lines for power, control and signal along one side, and these lines are connected to a substrate board through 87 wirebonds.

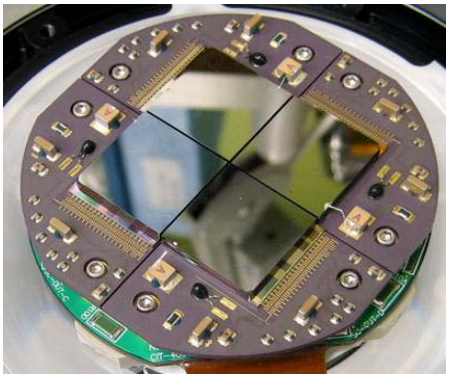

Fig. 1: 2 × 2 close-tiled array of CZT crystals (20.2 × 20.2 mm^2) in a focal plane module of *NuSTAR*, where each CZT crystal is bonded to its ASIC. The control, data and power inputs are accessible via pads on the upper surface of the ASIC (e.g. on the right side of the nearest ASIC shown) and are directly wire bonded to the carrier board. [5]

Surveying the sky for transient events with a focusing telescope of a relatively narrow field of view (< 1 sq. degree) is inefficient. Coded-aperture telescopes can image a relatively large field of view (> 100 sq. degrees) at a given time. The sensitivity of coded-aperture telescopes is directly proportional to the square root of the detector area, and thus building a large area detector plane is essential to achieve high sensitivity for coded-aperture telescopes. In *ProtoEXIST2*, we multiplex the 2 x 2 CZT array used in the *NuSTAR* focal plane into a 8 x 8 CZT array to build a large detector plane as shown in Fig. 2 [3, 4].

The signal, control and power lines of each NuASIC are read out or provided through wirebonds which connect the pads on the top side of the NuASIC to the matching pads on the top side of the substrate board (Fig. 1 and Fig. 2(b)). Wirebonds, although proven for space application and perceived necessary for hybrid sensors like CZT detectors, introduce assembly complexity and undesirable gaps between detector units as shown in Fig. 2(a) & (c). Subsequently, they pose a serious challenge in building a large area detector plane at low cost. Gaps between the detector units not only reduce the packaging efficiency of the detector plane but also introduce additional background counts from X-rays entering the side walls of each CZT, resulting in a non-uniform background pattern in the detector plane (Fig. 2(d)).

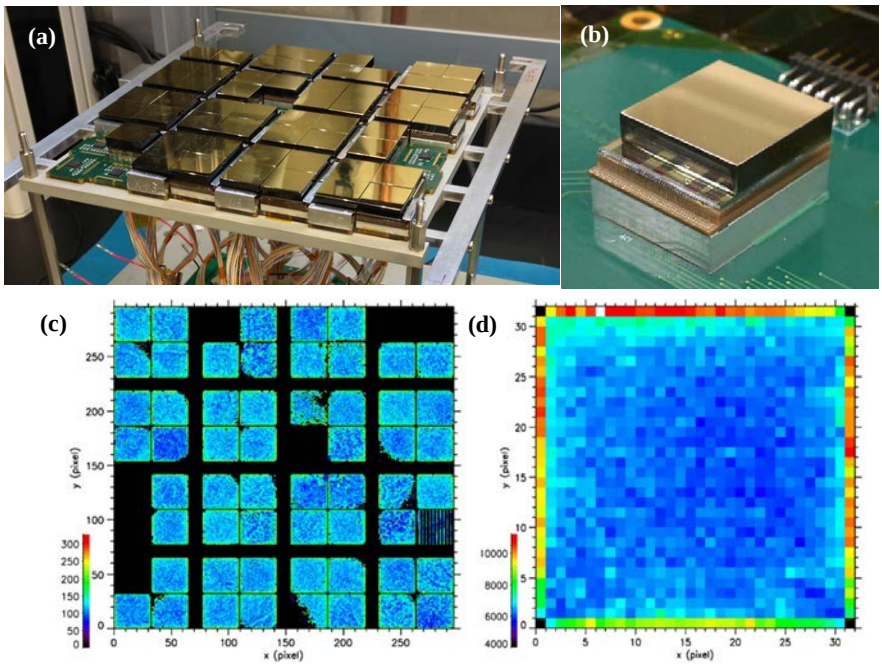

Fig. 2: (a) Detector plane of *ProtoEXIST2* during the assembly process. **(b)** Detector unit consisting of a 2x2 cm^2 CZT, the *NuSTAR* ASIC, and the ASIC carrier board. The unit is mounted on a test board for initial development. **(c)** Single pixel trigger event distribution in the detector plane during 2012 flight of *ProtoEXIST2*. **(d)** The same folded on the coordinate of a detector unit. [3, 4]

In this paper, we introduce

our effort to develop a new readout system using Through-Silicon Vias (TSVs), which eliminates the need for wirebonds, and consequently simplifies the detector architecture and integration and lowers the assembly cost.

2. THROUGH-SILICON-VIA (TSV) AND HREXI-EM DETECTOR PLANE

Fig. 3 illustrates the concept of TSVs, which enable a direct connection from the wirebond pads on the top side of a NuASIC to the flip-chip bonding pads on the backside, connected by TSVs through the ASIC. TSVs thus eliminate the need for the 87 wirebonds to control and readout the NuASIC and their complexity, fragility and extra space required to connect to a carrier board "sideways". In addition, unlike wirebonds, which have to be applied at a device level for each ASIC, TSVs can be implemented on all the devices in a wafer, which improves the processing efficiency and reduces the manufacturing and assembly cost in the long run. We collaborate with Tezzaron Semiconductor Corp. and its subsidiary Novati Technologies to develop the technology and wafer processing to insert TSVs on existing *NuSTAR* wafers to demonstrate the proof of the concept.

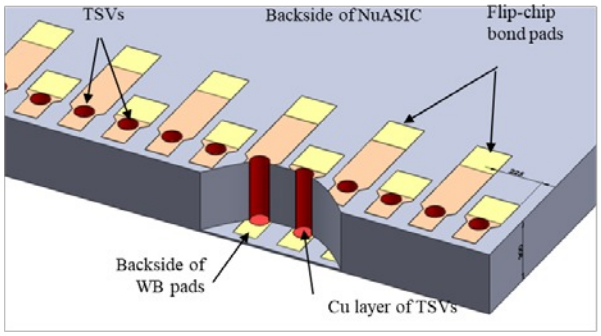

Fig. 3: Blind TSVs connect wirebond pads on the NuASIC topside to flip-chip bond pads on the NuASIC backside.

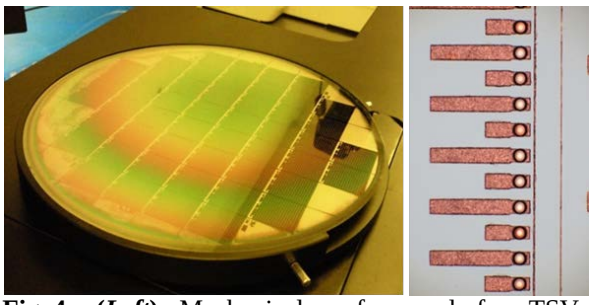

Fig. 4: **(*Left*)** Mechanical wafer used for TSV implementation, simulating the layout of *NuSTAR* wafers. **(*Right*)** Segment of the backside showing the TSVs and traces/pads for flip-chip bonding with a substrate board.

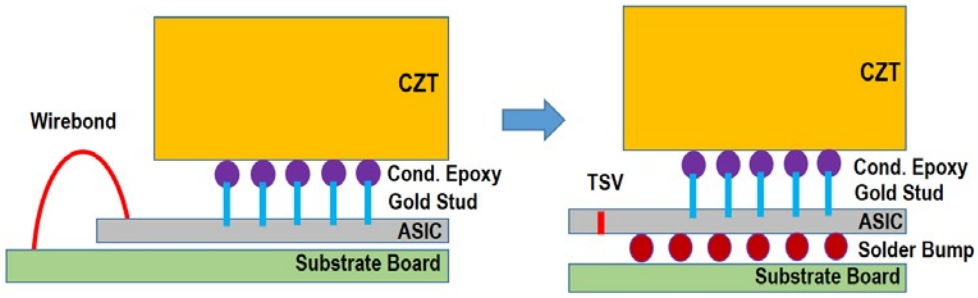

Fig. 5: Comparison of the detector crystal unit with wirebonds (***left***) versus TSVs (***right***). Each CZT crystal is bonded to a NuASIC through gold studs and conductive epoxy dots. The NuASIC and the substrate board can make electric connection through wirebonds, or in the case with TSVs, they are bonded through solder bumps, which provide both mechanical and electronical connections.

Fig. 4 shows Tezzaron prepared mechanical wafers for the initial development of the Si-etching and metal plating techniques. These mechanical wafers are essentially dummy Si-wafers but simulate the characteristics of the *NuSTAR* wafers with the metal/Si layer specification for the wirebond pads that the TSVs will connect to in *NuSTAR* wafers. Fig. 5 compares a single CZT detector unit assembly architecture using wirebonds versus TSVs. Each unit consists of a 2 x 2 cm^2 CZT crystal, bonded to a matching NuASIC with conductive epoxy dots for each of the 32 x 32 input pixels on the NuASIC, and a substrate backend

electronics board. When tiling these units to a larger detector plane, the former requires a relatively large gap beyond the active region of each CZT crystal for the row of wirebonds, while in the latter the gap is needed only as large as the extended region of the NuASIC. In addition, there are no exposed wires, which reduces the risk of damage and simplifies the subsequent assembly steps. For existing NuASICs, the gap between CZT crystals can be reduced to ~2 mm with TSVs from ~5 mm with wirebonds. Since the layout of existing NuASICs is not optimized in the digital section (beyond the active pixel region), we expect that the gap can be further minimized in our planned future ASIC design. In principle, the ASIC layout can be designed so that the ASIC footprint is only as big as CZT by implementing all the common circuitry below the metal layers where the individual pixel circuitry lies. Such ASIC layout optimization, when combined with TSVs, will enable truly gapless tiling of CZT detectors.

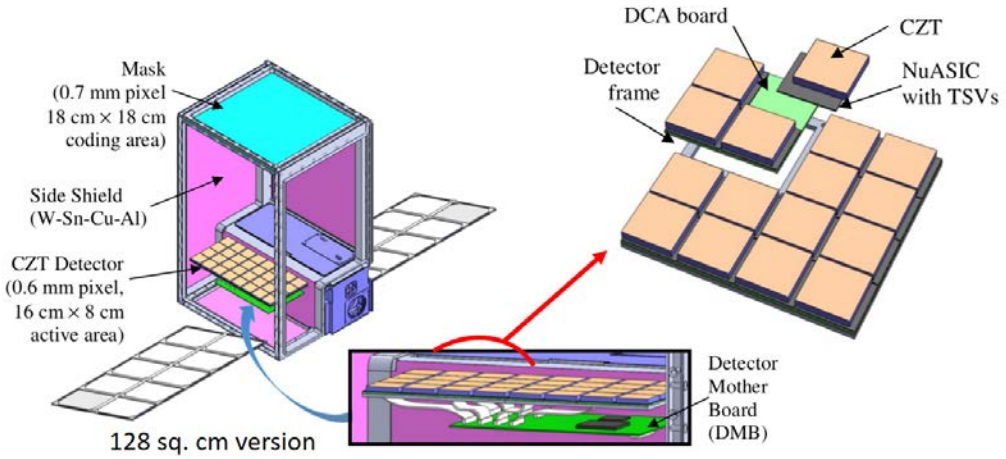

Fig. 6: Concept of 12U CubeSAT *HREXI*-EM configuration using Blue Canyon Technologies' 12U frame and 2U S/C system (blue). Key components are shown: Tungsten mask (cyan), side and rear shields (magenta), CZT detector plane (yellow blocks), and DMB (green). Each of 8 DCAs communicates with the DMB through a 36 pin cable. Detector area can be doubled (see text). Two side panels and the internal support structure are not shown for clear view. *Top-right* shows a simplified detector assembly architecture (2 x 2 DCAs) using TSVs.

In *ProtoEXIST2*, a Complex Programmable Logic Device (CPLD) is mounted in one of the substrate boards to control each NuASIC and read out its digital data (pixel position and pulse height for each event). With 3-D stacking capability using TSVs, if a backend processing ASIC is fabricated to perform the functionality of the CPLD used in *ProtoEXIST2*, all three major components – CZT crystal, a frontend readout ASIC and a backend control ASIC – can be directly stacked from top to bottom, which greatly simplifies the detector assembly with minimal gaps between the detectors.

Fig. 6 illustrates a design concept of 12U CubeSat *HREXI* and its detector plane architecture with a 128 cm^2 version of the detector plane. The 12U CubeSat form factor in 2 x 2 x 3U would allow as large as 256 cm^2 detector plane. In this architecture, we mount a 2 x 2 array of CZT crystals and matching four TSV-NuASICs onto a Detector Crystal Array (DCA) board. A total of 16 or 32 DCA modules can be mounted on a precision optical bench. The full array will be read out and controlled by a Detector Mother Board (DMB) containing a FPGA (as on *ProtoEXIST2*). This architecture uses only two stacks of substrate backend electronics boards (DCA and DMB), which is simplified from a three-board stack system in *ProtoEXIST2* [2].

3. IMPLEMENTING TSVS

Fig. 7 outlines the TSV implementation process. First, existing 700 µm thick 8 inch *NuSTAR* wafers are polished and thinned down to a 250 – 300 µm thickness. Typical aspect ratio (height versus diameter) of TSVs ranges from 2 to 3, although it can be as high as 5 in some applications. Since the wirebond pads on NuASICs, to which TSVs will make an electric connection, are 120 µm x 180 µm, we chose the diameter of TSVs for NuASICs to be 100 µm. Thus, the existing *NuSTAR* wafers are too thick (700 µm) to implement TSVs, so they have to be thinned down. In order to enable the subsequent steps in wafer processing after TSV insertion such as solder bumping, etc., while keeping the aspect ratio of TSVs reasonable low, we have settled to thin down the wafers to ~250 – 300 µm. For the TSV implementation itself, another carrier wafer is attached to each thinned *NuSTAR* wafer (to enable risk-free handling), and at the end of the TSV insertion and conductive plating processes, the carrier wafer is debonded from the *NuSTAR* wafer with TSVs. Second, a series of chemical etching and passivation steps are applied to form blind vias, to expose the metal layer in the wafer for electric connection (via plating) to the TSV and to insulate the Si substrate from the conductive Cu plating of the vias. Third, the inner surface of the vias, the backside traces and the pads for flip-chip bonding are plated and the backside of the wafer is passivated over all but the bonding pads. Finally, the carrier wafer is debonded from the *NuSTAR* wafer with TSVs.

The initial runs were performed to implement blind vias of a vertically straight cylinder shape profile on 300 µm thick mechanical and *NuSTAR* wafers. An SEM image in Fig. 8 shows a cross-sectional view of a TSV on a mechanical wafer during on one of the initial attempts, where chemical etching formed well-defined blind vias, but the subsequent metal plating processes failed to evenly coat the inner wall of the TSVs near the bottom 1/3rd, while the entrance of the TSVs were piled-up with the main plating material Cu. Changing the seed layer for plating from Cu to electroless Ni or changing plating parameters such as sputtering angles did not improve the uneven thickness of the plating layer. A conductivity test of TSVs on a mechanical dummy wafer revealed that 16 out of 49 devices in a wafer have more than 80 TSVs with good electric connection, indicating a yield of about 33%. While this yield is relatively low, we applied the same

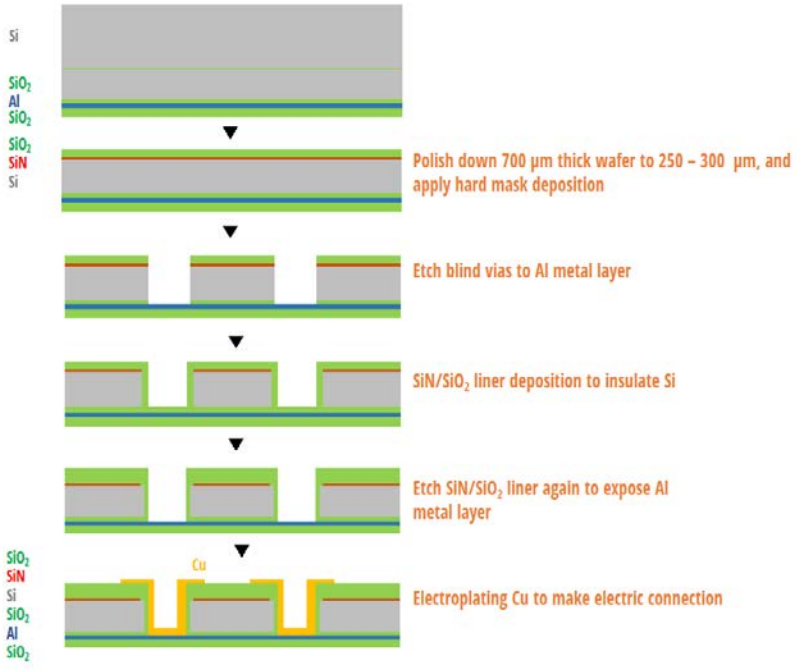

Fig. 7: Simplified TSV implementation processes illustrating thinning the wafers, etching & passivating TSVs, and electric plating TSVs.

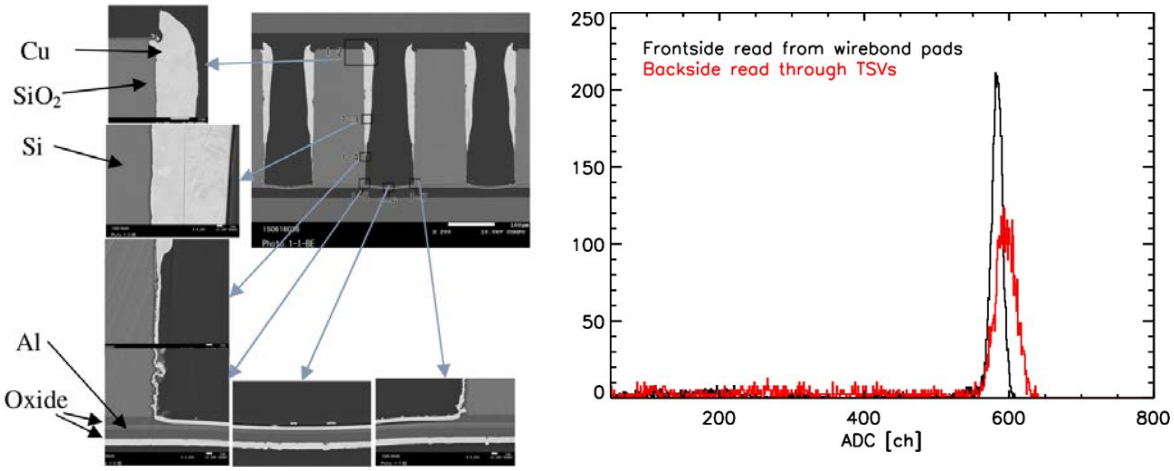

Fig. 8: (*Left*) SEM image of a TSV in a die with a good electric connection. The vertical etching profile of the TSV led to accumulation of sputtered Cu layer on the entrance (top), which in turn led to relatively thin coating near the bottom, lowering the overall yield to ~33% of electric connection. (***Right***) Internal pulser spectra of a NuASIC with TSVs measured through the wirebond pads (black), and through the TSVs (red).

approach on one of the thinned *NuSTAR* wafers to ensure the compatibility between the *NuSTAR* wafer and the TSV processes. About 5 out of 21 devices tested showed some functionality when operated through TSVs, but none of them functioned properly except for one.

Fig. 8 compares two internal pulser spectra of a NuASIC (die #47) with TSVs of a vertical etching profile: one from the frontside probe on the original NuASIC wirebond pads (black) and the other from the backside probed through TSVs (red). While the NuASIC appears to function, the pulser peak from the backside shows a larger spread and the NuASIC drew more current than normal NuASICs by a factor of three. In fact, this device was the only NuASIC with TSVs that could produce its onboard pulser spectra. The common failure mode of NuASICs from this first *NuSTAR* wafer with TSVs (including die #47), either from the frontside or backside probe, is an over-current draw instead of an open circuit, which we expected from the possible incomplete TSV electrical connection due to lack of the Cu plating material near the bottom of

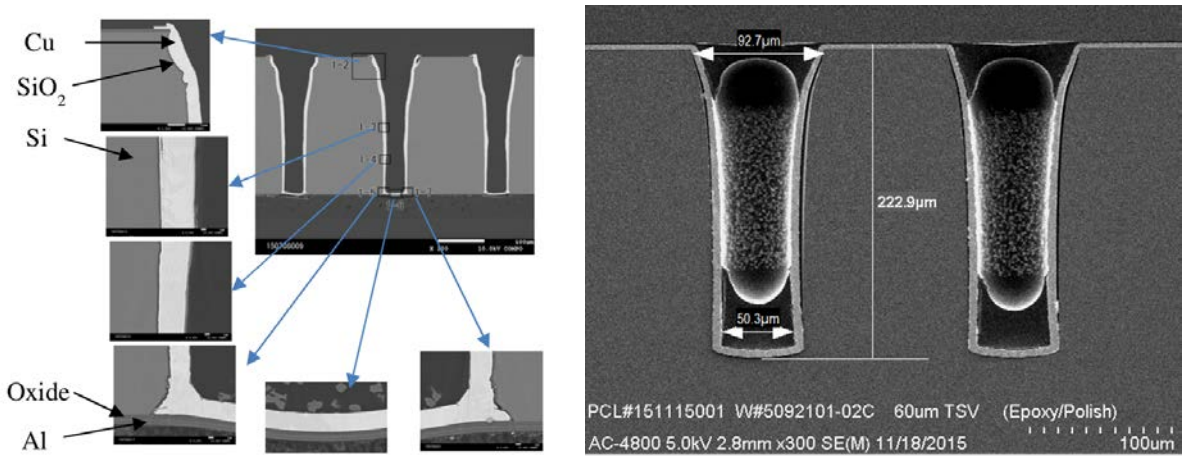

Fig. 9 SEM Image of a TSV with tapered etching profile. The Cu layer is evenly coated on the inner surface of the TSV, ensuring high yield of good conductivity. (***Left***) One of the first attempts of tapered TSVs on a 300 µm thick mechanical wafer. (***Right***) Taper TSVs implemented on a 250 µm thick mechanical wafer showing improved smoothness of the etching profile.

the TSVs in the case of the backside probe through TSVs. High resolution SEM images of one of the NuASICs in this run did not reveal any smoking gun or short (e.g., between the metal plating layer and the Si substrate), which could explain high current draw, but they did show that the etching and subsequent plating process left somewhat jagged shapes of a via profile, which can be prone to electric shorting between the metal plating layer and the Si substrate. Since each SEM image only shows one cross section of a few TSVs, it is plausible that shorting could occur on some other section.

4. TAPERED TSVS

In our next wafer processing run, we made several changes to improve the yield. First, to reduce the chance of shorting between the metal layer and the Si substrate, which we suspected to be the cause of high current draw, we quadrupled the insulation layer between the metal plating layer and the Si substrate. Second, to improve the conductivity of TSVs, we first changed the via shape through a multi-step etching process to a tapered geometry where the entrance of TSVs is wider (100 μm diameter) than the bottom side (70 μm diameter). Third, we thinned down the wafer to 250 μm to enable a smoother etching profile. Fig. 9 shows two SEM images of tapered TSVs implemented on 300 and 250 μm thick mechanical wafers, where the Cu layer is evenly plated and the etching profile is progressively smoother.

We have applied tapered TSVs on two *NuSTAR* wafers. Fig. 10 shows an SEM image and its close-up image of the bottom side of a tapered TSV from the NuASIC, which functioned successfully through TSVs. The Cu layer is relatively thick (> 10 μm) and evenly plated at the bottom side of the TSV. Fig. 11 shows the internal pulser spectra of 4 working devices, which exhibit a proper pulser resolution. We have conducted functional tests on 16 devices, and 11 devices operated perfectly through the TSVs without any degradation in the spectral resolution or high current draw. The overall yield of NuASICs with TSVs, therefore, is about 70% with the current process. This demonstrates the proof of the concept for TSVs, and it is a major breakthrough in our TSV development. Since *NuSTAR* wafers have a yield of about 90% for working devices, we estimate that the current TSV implementation process has a yield of >75% for successful insertion of TSVs.

5. SUMMARY AND FUTURE DEVELOPEMENT

We have successfully demonstrated the concept of the proof for TSVs that can be inserted into the existing NuASICs. This opens up a new CZT detector assembly architecture starting from a design of a new ASIC

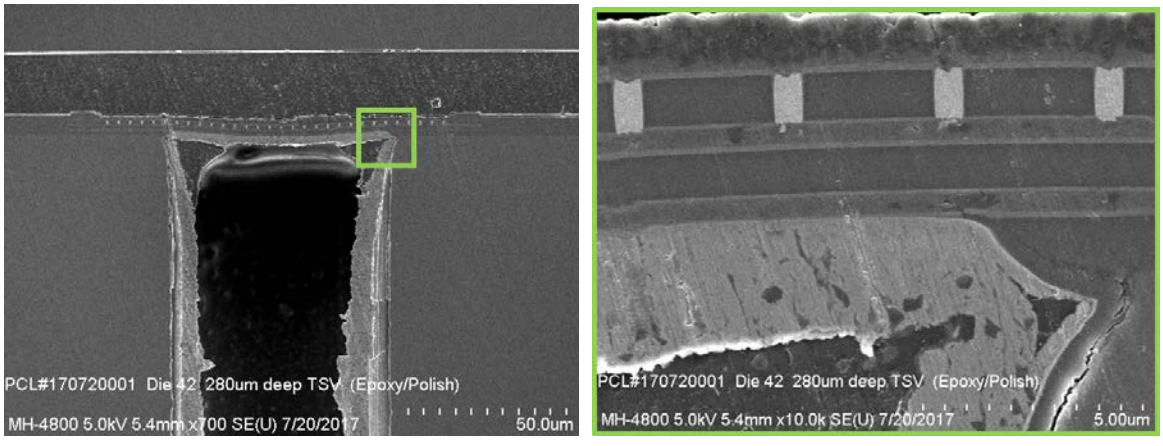

Fig. 10: SEM image of the bottom side of a TSV in a NuASIC (Die# 42) from the latest run, which shows relatively thick Cu plating. This NuASIC successfully functioned through TSVs. Note the orientation of this image is up-side down compared to the previous SEM images: the TSV entrance is on the bottom side here, whereas in the previous figures the TSV entrances are on the top side of the images.

layout which will include optimized locations for TSVs (and no wirebond pads) to the assembly of a large number of CZT detector units. In the short term, we plan to assemble a few dozen of working CZT detector units using TSV-NuASICs to further optimize the process and improve the yield for TSV insertion process. We are also in the process of designing the subsequent backend readout system for the 12U CubeSat *HREXI*-EM to take advantage of near gapless tiling of CZT detector units enabled by TSVs.

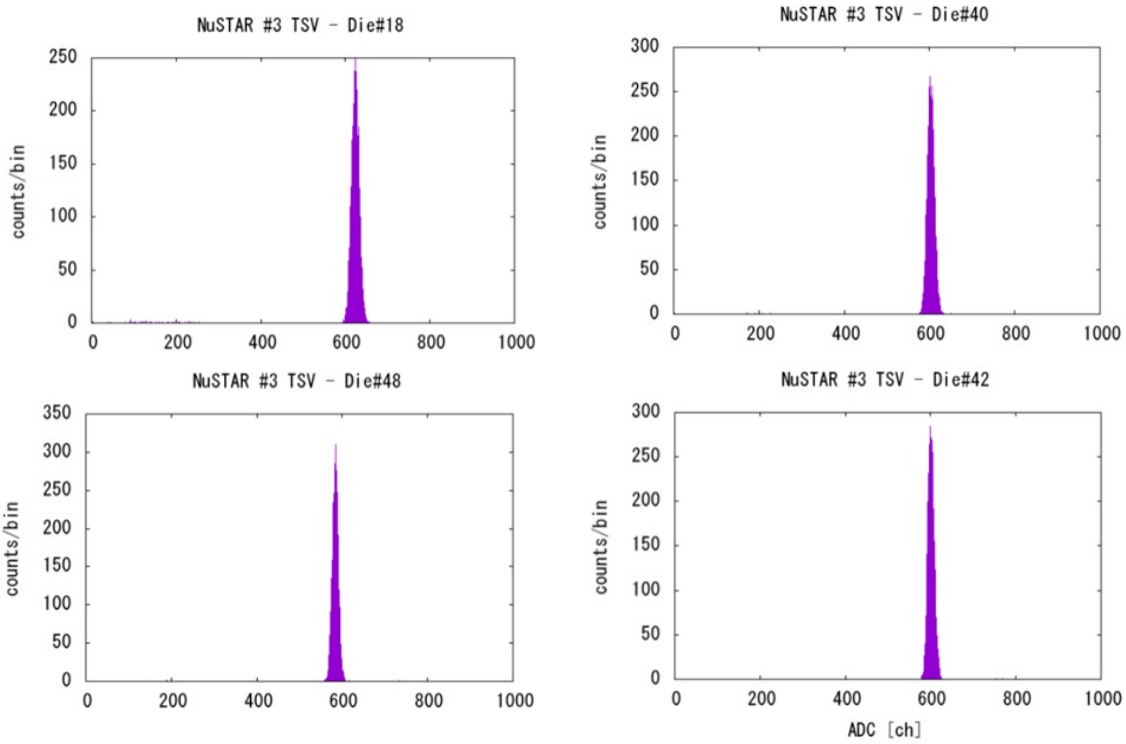

Fig. 11: Pulser spectra of four NuASICs with tapered TSVs from the probe test through TSVs. All show normal pulser response. The spectra are the stacked results of ~40 pixels for each ASIC.

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