DEVELOPMENT OF A HIGH EFFICIENCY MECHANICALLY STACKED MULTI-JUNCTION SOLAR CELL

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INTRODUCTION

Monolithic, 2-terminal, epitaxially grown multi-junctions represent the state-of-the-art in high efficiency photovoltaic space power. Their *in-situ* monolithic integration results in an elegant device structure with high efficiency, relatively high specific power, and a simple fabrication process. The monolithic, epitaxially grown nature of these devices also imposes materials and design restrictions which impede the march to significantly higher performance. These devices presently require lattice matched epitaxial templates (substrates) which limits the materials choices for integration. The barriers to producing high photovoltaic quality epitaxial materials on lattice mismatched templates have not been easy to surmount, despite extensive effort in the research community. Also, series interconnection of subcells is by far the most applicable connectivity approach for these monolithic devices, which further limits the connectivity design space.

In comparison, the mechanically stacked approach is advantageous because it relaxes or completely removes the material and design restrictions inherent in monolithic approaches. Device designers can conceivably integrate subcells of a chosen bandgap regardless of their lattice parameter, and in any connectivity arrangement. The benefits of alternative connectivity arrangements have been demonstrated [1].

In contrast to the elegance of monolithically integrated solar cells, mechanically stacked solar cells can be described as the “brute force” approach to higher performance. Mechanically stacked approaches have been investigated for over 25 years, but have been deployed in space only on small-scale experimental testbeds. Mechanically stacked approaches have historically been limited by several barriers. The cost associated with integrating devices on multiple substrates has been economically prohibitive. The substrates used as templates for III-V epitaxial solar cell structures comprise a very large fraction of the total cell cost. Techniques such as the CLEFT process [2] or epitaxial lift-off [3] have been developed to allow substrate removal and re-use, but they are difficult to implement cost-effectively in a production environment. *Ex-situ* integration is another barrier which increases the processing complexity and cost, and also results in performance losses associated with parasitic losses inherent to common interconnect schemes. Excessive weight also limits the practicality of these devices for space applications because of the multiple substrates and/or fixturing hardware used to stack the subcells together.

Here we present results of work performed on a new mechanically stacked solar cell approach for achieving very high efficiency and high specific power for space concentrator applications. This work addresses some of the cost and practicality limitations present in many historical mechanically stacked approaches, and is being funded by the NASA Office of Space Science through the Advanced Cross-Enterprise Technology Development Program. The goal of this project is to demonstrate the critical technology elements necessary for producing a 40% efficient, lightweight solar cell for concentrator arrays. A specific power of 1kW/kg is projected at the cell level.

DEVICE CONCEPT

The device structure being developed is shown in Figure 1. A high bandgap tandem based on the well-understood InGaP/GaAs materials combination is grown on an inactive GaAs or germanium substrate. By similarity, this tandem device structure capitalizes on the highly refined triple junction device structure already in high volume production at Emcore. Subsequent glass encapsulation provides a superstrate for mechanical support of the active solar cell, and a substrate selective removal process is used to decrease the weight of this high bandgap tandem.

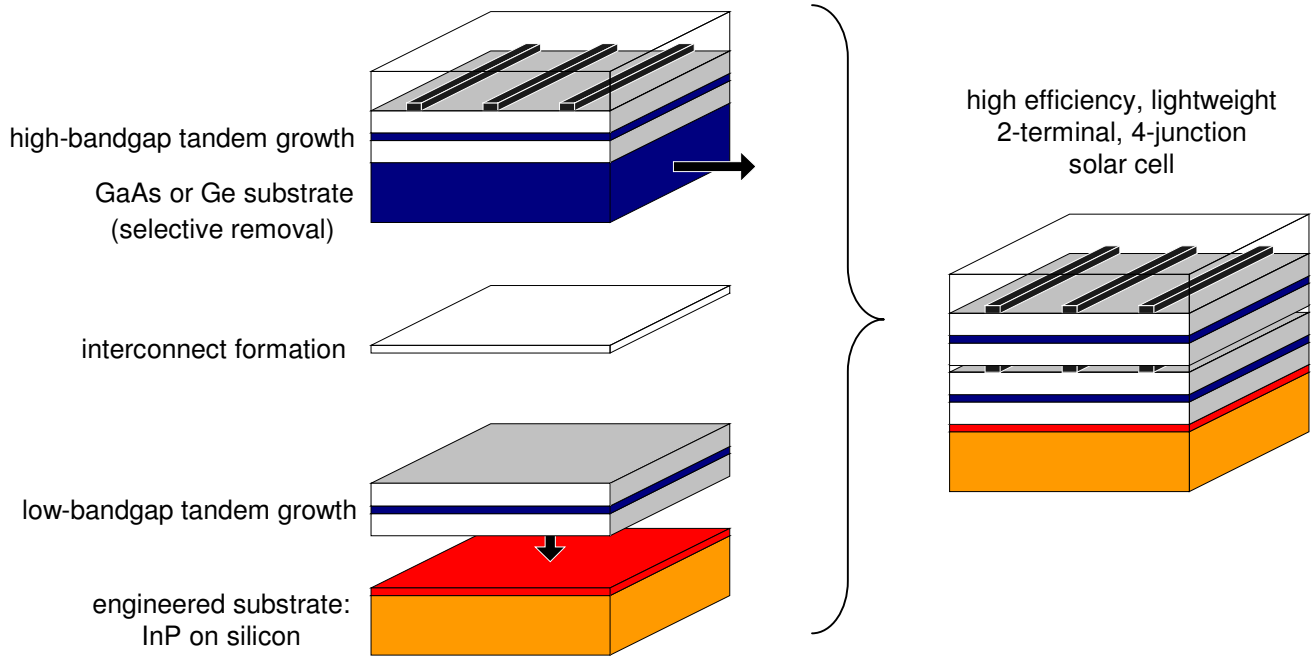


Figure 1 A schematic of the mechanically stacked 4-junction device integration scheme under development

Growth and processing of a low bandgap 1 eV InGaAsP / 0.74 eV InGaAs tandem is performed independently of the top tandem on an engineered InP-on-silicon substrate. The engineered substrate in this application is designed to provide an epitaxial template for active layers lattice matched to InP, while also benefiting from the lower weight, lower cost, and superior mechanical stability of silicon as compared to InP. Silicon's mass density is less than half that of InP, and the superior mechanical strength of silicon permits the use of thinner substrates. A thinner, lower density substrate allows a much higher power to weight ratio than would be possible with an InP substrate. A thin InP film, shown in red in Figure 1, is transferred to a silicon host substrate from a re-useable InP source wafer using a process that will be described in the next section.

A number of different schemes for mechanical and electrical interconnection of the two independently grown and processed devices are being considered. As shown in Figure 2, this combination of bandgaps is nearly ideal for a four junction series interconnected solar cell. This combination of bandgaps is therefore very compatible with two terminal, series interconnected integration, provided that the tandem interconnect is sufficiently transparent so as to transmit a near-theoretical spectral content to the bottom tandem. Achieving a highly transparent interconnect while also maintaining both a low electrical specific resistivity and good mechanical stability at the interconnection is critical to the success of this two terminal approach. Here we note that transmission loss through the tandem interconnect can be partially compensated for by reducing the thickness of the top tandem, thereby decreasing the fundamental, above-gap absorption in the top tandem.

ENGINEERED SUBSTRATES

The InP-on-silicon engineered substrate is being developed at Cal Tech using the Smart-cut process originally developed by Bruel *et al.* for silicon-on-insulator applications [4]. The process is illustrated schematically in Figure 3. An InP wafer is implanted with hydrogen ions to a controllable projected range. The implanted side of the InP

wafer is then bonded to the silicon host substrate using modern direct wafer bonding methods [5]. The InP/Si wafer pair is annealed in a controlled ambient at elevated pressure and temperature. The anneal simultaneously strengthens the direct bond and perforates the InP wafer at the implanted region. The released InP substrate can then be re-polished and repeatedly used in the layer transfer process. The engineered substrate can then in principle be used to grow a high quality low bandgap tandem solar cell.

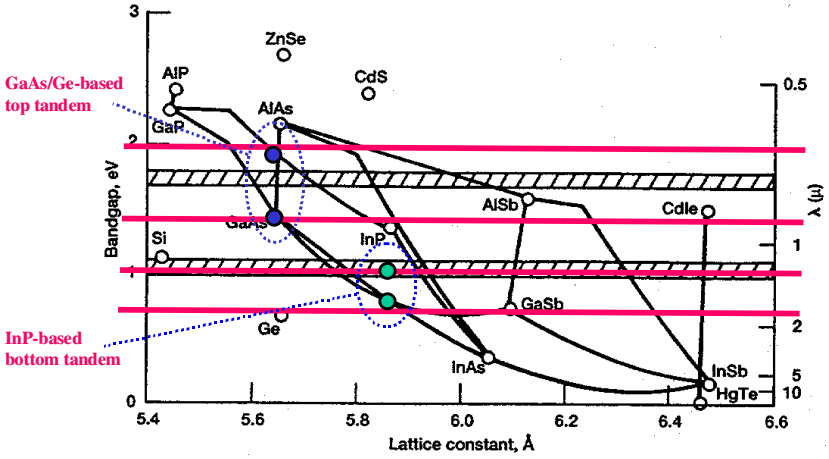
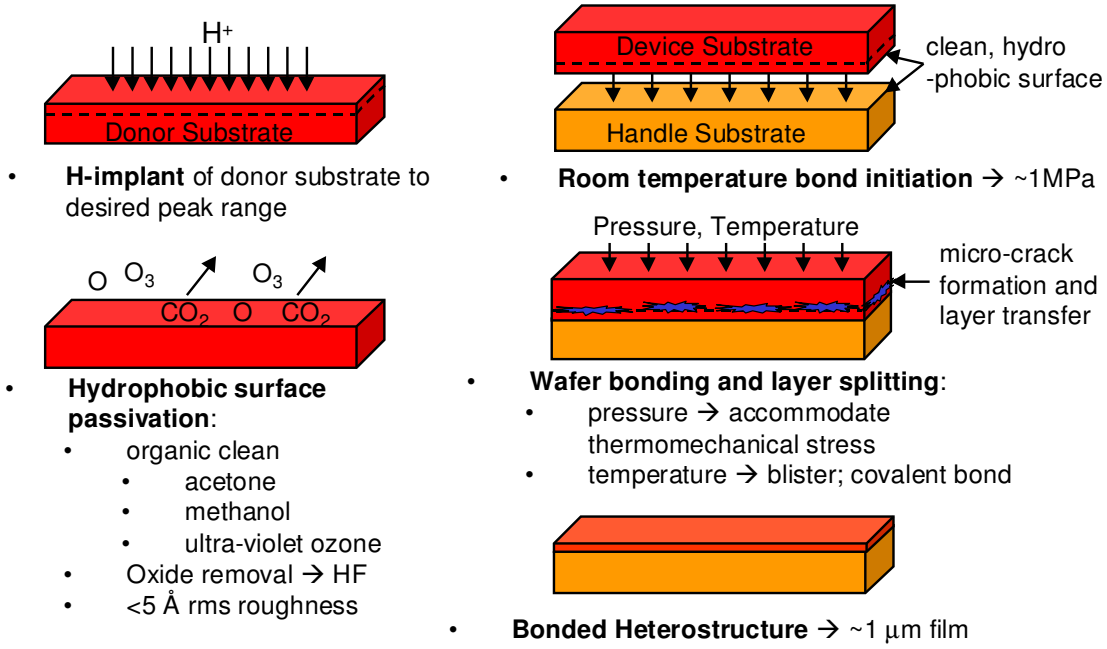


Figure 2 Bandgap versus lattice constant for the common compound semiconductor materials. Red lines indicate the ideal bandgaps for a four junction series interconnected solar cell under the AM0 spectrum at 25ºC. Dotted lines indicate the bandgap combinations being investigated in this work.



- **H-implant** of donor substrate to desired peak range
- **Room temperature bond initiation** → ~1MPa
- **Hydrophobic surface passivation**:
  - organic clean
    - acetone
    - methanol
    - ultra-violet ozone
  - Oxide removal → HF
  - <5 Å rms roughness
- **Wafer bonding and layer splitting**:
  - pressure → accommodate thermomechanical stress
  - temperature → blister; covalent bond
- **Bonded Heterostructure** → ~1 μm film

Figure 3 A process for producing InP-on-silicon engineered substrates based on the Smart-cut technology.

Much of the work at Cal Tech has focused on perfecting the Smart-cut process for InP/Si and developing an engineered substrate that is epi-ready. This requires a surface which is both free of dislocations that might propagate into the epitaxial film, and has a characteristic surface roughness similar to that of epi-ready polished InP.

Double heterostructures grown on as-transferred InP/Si engineered substrates have produced much lower photoluminescence intensity as compared to control samples grown on thick InP substrates. One potential cause of the presumed lower material quality on InP/Si is due to the presence of a region of highly defective InP at the surface of the engineered substrate, presumably caused by the ion implantation and layer transfer process. Figure 4 shows cross-sectional TEM images of the InP/Si pair, clearly showing an area of defective material at the exposed surface. More importantly, InP near the bonded interface appears to be less defective than the surface region. Polishing processes such as plasma etching, chemo-mechanical polishing, and wet chemical polishing etches are being investigated as means for removing the surface damage, thereby creating a surface more conducive to high quality epitaxial growth.

High resolution TEM images have revealed the presence of an oxide at the InP/Si interface. This interface layer is formed during the anneal in a nitrogen ambient, presumably resulting from residual water at the clean interfaces just prior to bonding. Despite the presence of this interfacial oxide layer, through-the-film current voltage measurements indicate an ohmic, low resistance behavior. The specific resistivity of the interface is less than 0.1 Ω-cm^2.

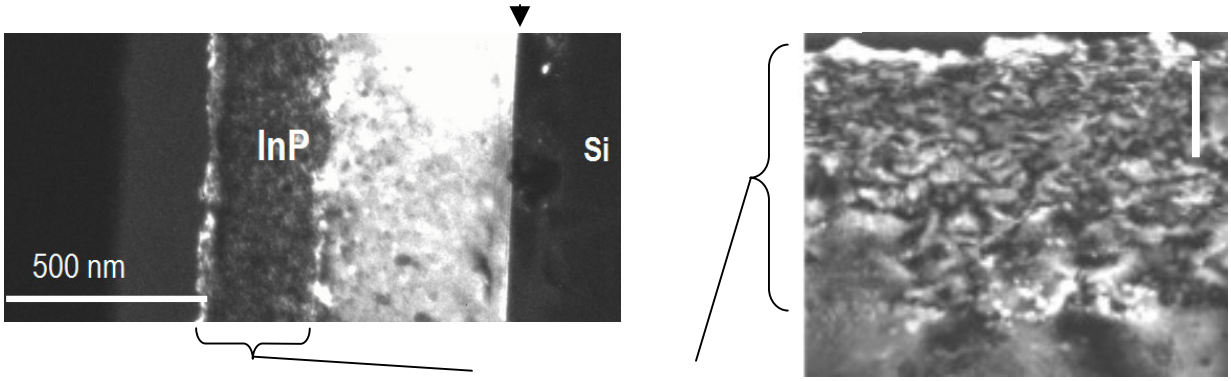
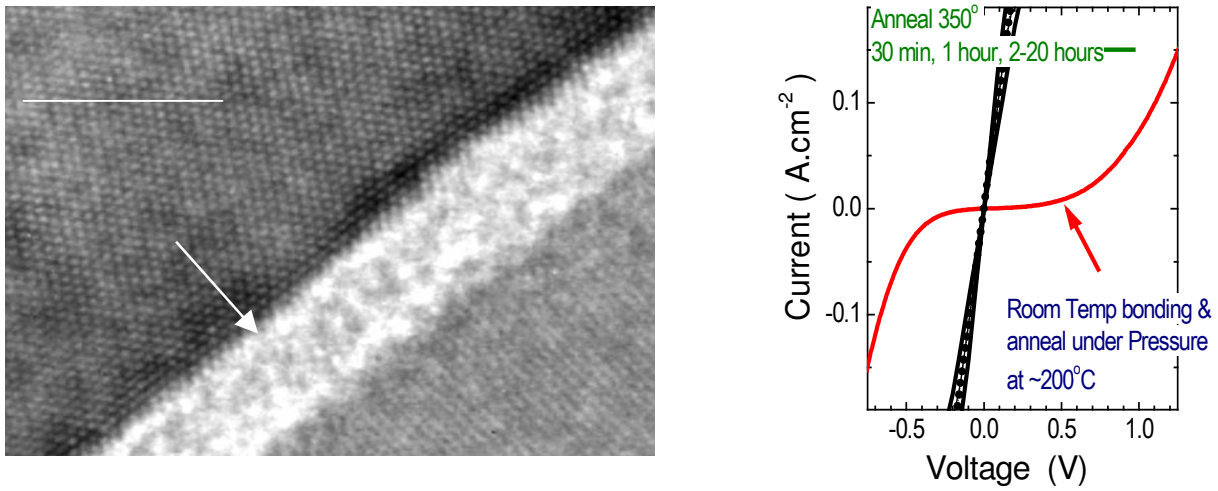


Figure 4 Cross-sectional TEM micrographs of an InP/Si engineered substrate. The images suggest a region of damaged, highly defective material near the implanted region of the InP.

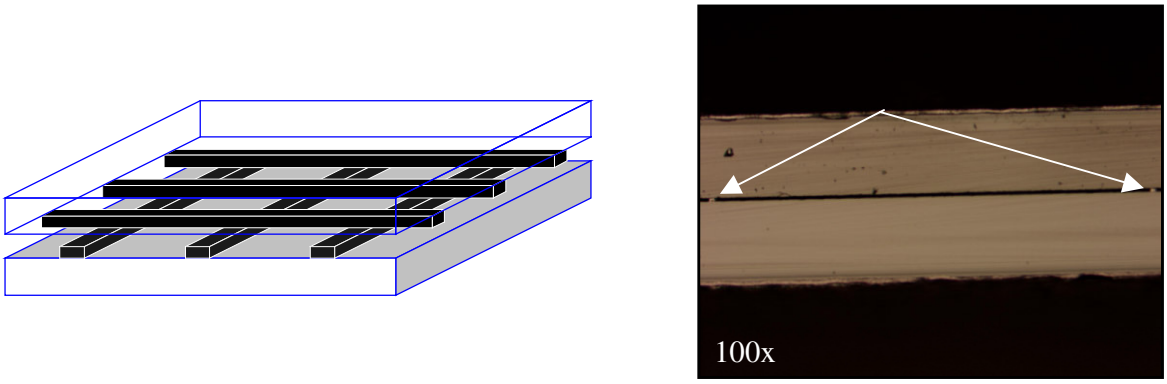


(a) (b)

Figure 5 (a) A high resolution TEM image indicating the presence of an interfacial oxide. (b) Through-the-film current-voltage characteristics of an InP/Si pair, suggesting less than 0.1 ohm-cm^2 specific resistivity.

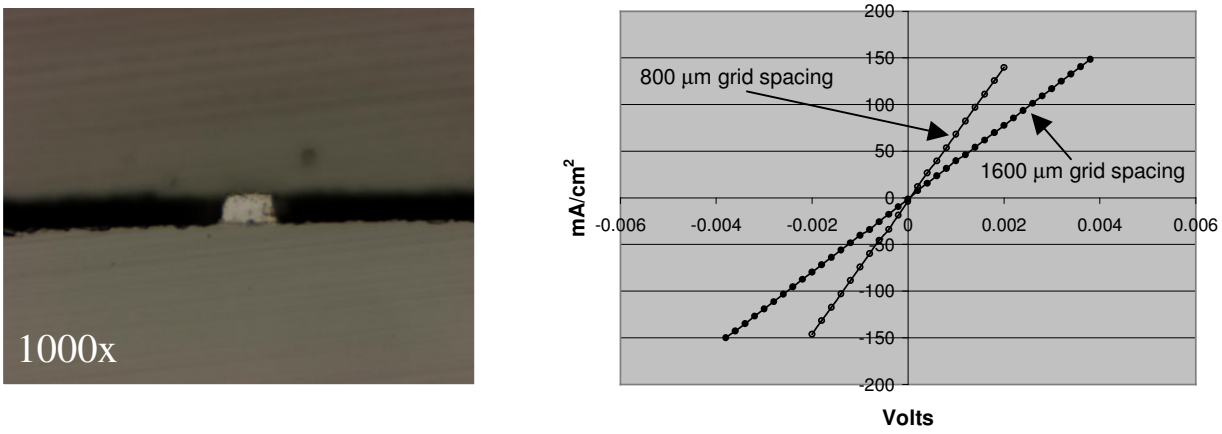
TANDEM INTERCONNECTION

One of the tandem interconnect approaches being evaluated is a eutectic metal bond at the interface between two perpendicularly oriented metallic grids, as depicted in Figure 6(a). Advantages of this approach include the absence of a fixturing jig to hold the two cells optically in series, the absence of a peripherally formed interconnect which otherwise complicates the fabrication procedure, and the elimination of the need for pattern alignment in joining the two grids. Gold-germanium melts at a eutectic temperature of 356ºC. Grid fingers coated with a gold-germanium alloy can therefore be bonded together at low temperatures using moderate pressure. The eutectic metal bond approach is being experimentally evaluated using test structures such as that shown in Figure 6(b). Gridded germanium wafers have been bonded together to test the mechanical stability and electrical conductivity of the resulting interconnect. Figure 7(a) suggests intimate contact between the grid finger and germanium substrate. The resulting test structures are mechanically robust and produce an interconnect with very low specific resistivities of 0.024 Ω-cm^2 and 0.014 Ω-cm^2 for 1600 µm and 800 µm grid spacings, respectively. This type of interconnect scheme results in a modest 2-4% transmission loss due to grid shading.



(a) (b)

Figure 6 (a) A conceptual schematic of the gridded interconnect scheme being evaluated. (b) A cross-sectional optical micrograph (100x) showing a metallic grid successfully bonded to two germanium wafers.



(a) (b)

Figure 7 (a) A cross-sectional optical micrograph (1000x) showing metallic grid successfully bonded to two germanium wafers. (b) Through-the-film current voltage characteristics of germanium wafers with a gridded, bonded interface.

BOTTOM TANDEM DEVELOPMENT

Prototype lattice matched bottom tandems consisting of 1eV InGaAsP, a low bandgap tunnel diode, and 0.74 eV InGaAs are being grown and processed on InP. The performance of these devices serves as a benchmark for devices to be grown on the InP/Si engineered substrates. The bottom tandem is projected to contribute 9-10% absolute to the overall device efficiency at ~10 suns AM0. Devices grown and processed at NREL have reached 6.1% efficiency without AR coating at 1 sun AM0, as shown in Figure 8. These 0.108 cm^2 devices were measured under a simulated AM0 spectrum filtered by a low resistivity GaAs wafer coated on both sides with an AR coating.

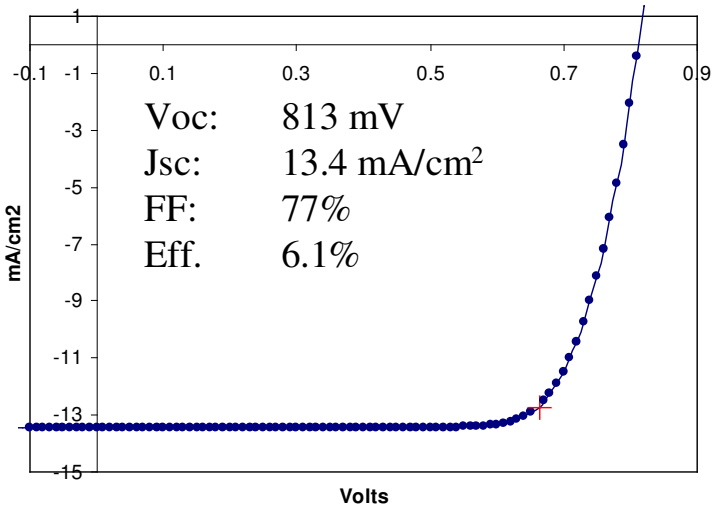


Figure 8 Current density-voltage characteristics of a 1.0 eV InGaAsP, 0.74 eV InGaAs prototype tandem on InP, measured under a fintered AM0 spectrum at 25ºC.

ANTI-REFLECTION COATING DEVELOPMENT

The 4-junction, nominally current matched solar cell being developed here can achieve an unprecedented AM0 efficiency of 40%, which is near the theoretical limits of a 4-junction device. This is made possible by the highly efficient utilization of photons over an extremely broad spectral range (300–1700 nm). Achieving a performance near the theoretical limits requires near-unity quantum efficiency for all subcells in the solar cell structure. This places requirements on AR coating performance that have previously not been necessary. The AR coating transmission band of the top tandem must be much broader that is currently necessary for production triple junction solar cells.

With the realization that the standard AR coating used for production triple junction solar cells would result in substantial loss in a 4-junction cell, we have designed an improved AR coating using methods presented in earlier work [6]. Anti-reflection coating design is accomplished here with optical modeling software which both optically and electrically models device performance as a function of the AR coating structure. A new AR coating design as presented in Figure 9 results in a modeled 1% absolute efficiency gain over the standard dual layer AR coating. Table I summarizes the relevant modeled device parameters.

SUMMARY

An affinity for high performance solar cells in the space market, as well as the development of new engineered substrate technology, has warranted a re-consideration of mechanically stacked solar cell technologies. Mechanically stacked approaches result in a wider materials and interconnectivity design space compared to monolithic approaches. We are investigating the Smart-cut technology to produce InP/Si engineered substrates. Successful transfer of InP films to a silicon substrate has been demonstrated, and the resulting structure is

mechanically stable after MOCVD growth. The electrical resistivity of the bonded interface is low, despite the presence of a very thin interfacial oxide. Work continues in regard to producing an epi-ready surface for the subsequent growth of high quality MOCVD layers. Tandem cell interconnectivity approaches are being investigated which can result in minimal parasitic loss and are also simple to process. Bottom tandem prototype cells have been fabricated on InP, with encouraging results. New AR coatings have also been designed to improve the optical coupling to these extremely wide-band solar cells.

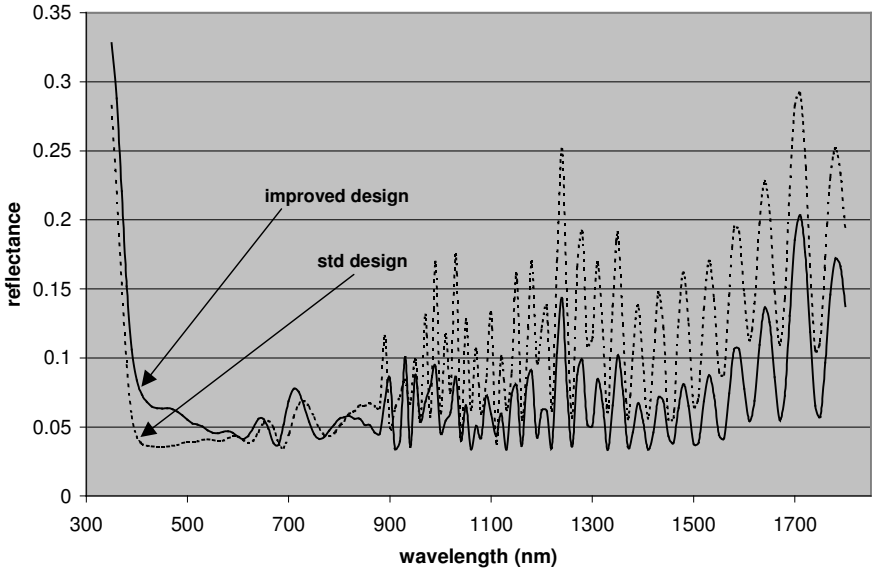


Figure 9 Modeled reflectance of a top tandem solar cell. A new AR coating design is compared to Emcore's standard AR coating structure.

Table I Predicted performance metrics for a 4-junction cell, nominally current matched, using the reflectance design modeled in Figure 9.

	std. design	new design
modeled efficiency (%)	34.23	35.67
maximum Jsc (mA/cm^2)	17.86	17.86
achieved Jsc (mA/cm^2)	15.54	16.65
weighted transmission (%)	87.03	93.21

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