0.1 μm InP HEMT DEVICES AND MMICs FOR CRYOGENIC LOW NOISE AMPLIFIERS FROM X-BAND TO W-BAND

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Abstract

We present the TRW 0.1 μm InP HEMT MMIC production technology that has been developed and used for state-of-the-art cryogenic LNA applications. The 0.1 μm InP HEMT devices typically show cutoff frequency above 200 GHz and transconductance above 1000 mS/mm. Aspects of device design and fabrication are presented which impact important parameters including the InP HEMT device gain, gate leakage current, and parasitic capacitance. One example of state-of-the-art cryogenic MMIC performance is a W-band cryogenic MMIC LNA operated at 20 degrees Kelvin that shows above 23 dB gain and a noise temperature of 30 to 40 K (0.45 to 0.6 dB noise figure) over the band of 80-105 GHz.

I. Introduction

Extremely sensitive receivers with minimum noise performance, high gain, and a high degree of gain stability are required for radiometer applications. Indium phosphide high electron mobility transistors (InP HEMTs) and MMICs are ideal candidates because of their proven low noise and high gain performance [1]. Indeed, InP HEMT-based low noise amplifiers (LNAs) operating at cryogenic temperatures are being developed for the radiometer applications, and provide minimum noise temperature performance with extremely high gain and bandwidth at cryogenic operation from X-band to W-band [2-6].

We present the TRW 0.1 μm InP HEMT MMIC production technology that has been developed and used for state-of-the-art cryogenic LNA applications. Aspects of device design and fabrication are presented which provide the InP HEMT device with high gain, low gate leakage current, and reduced parasitic capacitance, thereby leading to improved performance. Examples of cryogenic LNA performance at X- and W-band are shown.

II. HEMT Fabrication and Performance

The InP HEMT epitaxial layer structures were grown by molecular beam epitaxy (MBE) at TRW on 3-inch semi-insulating InP substrates. Figure 1 shows a schematic of the InP HEMT device, which is single-side delta-doped, and includes a 65% indium channel that typically provides ~10% higher gain than our baseline 60% indium channel device. Room temperature Hall measurements typically show mobility of 11000 cm^2/Vs and channel electron carrier density of $3.5x10^{12}$ cm^{-2}, and at 77 Kelvin the mobility was 42000 cm^2/Vs and channel electron carrier density of $3.3x10^{12}$ cm^{-2}

The wafers were processed using the baseline TRW InP HEMT MMIC production process [1] which typically shows RF circuit yields of 75% to 80%. The frontside InP HEMT MMIC process provides 75 nm silicon nitride passivated 0.1 μm T-gate HEMT devices, 100 Ω/sq thin film resistors, 300 pF/mm^2 metal-insulator-metal capacitors, and two levels of metal interconnects. The backside InP HEMT MMIC process provides a 75 μm thick wafer with dry-etched through-substrate vias which connect the backside metal ground plane to the frontside device and circuit elements [7].

A key component in the HEMT fabrication is the control and repeatability of the gate process, which includes gate lithography, recess, and metallization. The 0.1 μm gate is defined by electron beam lithography in a bilayer of PMMA/P(MMA-MAA). Figure 2 shows that the gate length is typically 0.09 μm with 0.01 μm sigma for 100 wafers. The gate recess is performed using a wet etchant. The etchant, combined with excellent adhesion of PMMA to the wafer, provides minimal lateral etching, and therefore device gain and current are maximized since channel electron density is not depleted in the regions extrinsic to the gate. Furthermore, the impact of surface-related effects (traps) are minimized by limiting the lateral gate recess dimension. The inset in Figure 2 shows a cross section of a recessed 0.1 μm T-gate with negligible lateral etching outside of the gate area.

The 0.1 μm gate HEMTs typically show peak transconductance (Gmp) above 1000 mS/mm and cutoff frequency (f_T) above 200 GHz. Figure 3 shows Gmp as a function of Vgp (the gate voltage at which the transconductance peaks). The target Vgp for optimal performance is from 0.2 to 0.3 V. This target provides maximum Gmp and gain while preventing appreciable forward Schottky gate leakage current. The inset of Figure 3 shows the gate current as a function of gate voltage, Vg. The gate current is measured under 3-terminal operation with drain bias of 1 V.

The processing and device design have been tailored to maximize gain and minimize gate current, which are two important factors in optimizing devices for cryogenic noise performance. Low gate current operation is most crucial for the lower frequency LNA applications

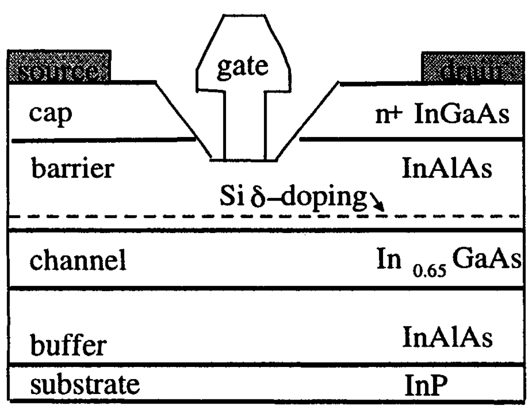

Figure 1. Schematic of the InP HEMT heterostructure with 65% indium channel.

(X-band) since gate current is a component contributing to shot noise. Decreased gate leakage current improves the overall cryogenic noise performance of the LNAs, especially at lower frequencies. At high frequencies (V-, W-band) where the device is stable, gain is proportional to the square of Gm. For gain limited cryogenic devices, the output noise dominates. Increased gain reduces the output noise contribution, as well as contribution from subsequent stages in the LNA, as long as the output noise is not increased. The gate current has less of an impact at

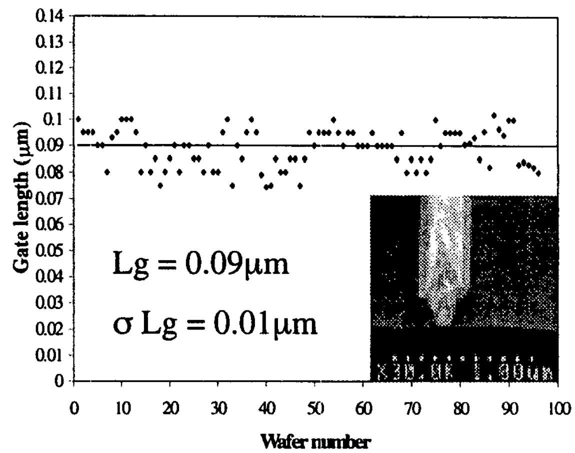

Figure 2. Gate length statistical parameter chart (SPC) for 0.1 μm T-gate. The inset shows a cross-section of the recessed T-gate.

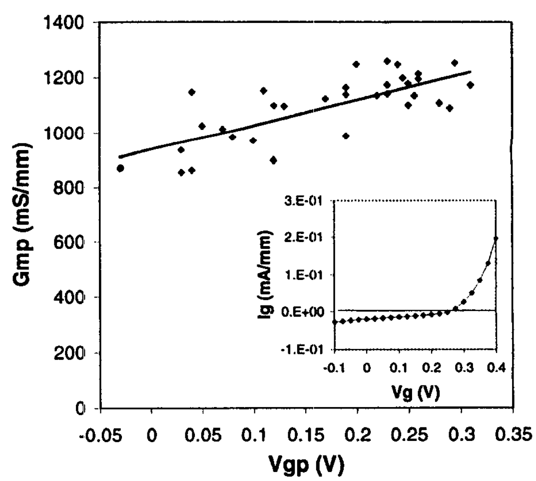

Figure 3. Peak transconductance (Gmp) versus the gate voltage, Vgp; where Vgp is defined as the gate voltage at which Gmp occurs. The inset shows the gate current as a function of gate voltage (Vg).

higher frequencies because the shot noise, shorted by capacitance, decreases linearly with increasing frequency.

III. Cryogenic Performance

The InP HEMT devices were characterized at cryogenic temperatures at JPL using a cryogenic coplanar wave guide probe station [3]. Figure 4 shows the device transconductance and gate current as a function of gate voltage with a drain bias of 0.7 V, measured at 12 K. The gate current is 1 to 2 orders of magnitude lower, and the transconductance is ~10% higher than at room temperature. In Figure 5, there are two curves each of Gm and Ig which lie almost on top of each other, and one of the measurements was made in the dark, and one with light. There is negligible effect of light on the characteristics, indicative of low trap density in the material.

Cryogenic MMICs and MICs have been designed and operated from X-band to W-band at temperatures in the range of 10 to 20 Kelvin. An example of a coplanar-design, wide bandwidth, 4-stage InP HEMT MMIC for W-band cryogenic applications is shown in Figure 5. A 40 μm periphery InP HEMT is used in each stage of the MMIC. Figure 6 shows the measured cryogenic noise performance of the MMIC at 20 Kelvin. The MMIC shows a noise temperature of 30 to 40 K (0.45 to 0.6 dB noise figure) over the band of 80-105 GHz, with over 23 dB gain. The bias conditions were at a drain voltage of 0.58 V and a total current of 6.9 mA, equivalent to only 4 mW of power. The devices can be biased as low as 0.4 V (drain bias) and the MMIC shows only ~1dB lower gain and negligible noise temperature increase, demonstrating the excellent gain at low bias that the InP HEMT devices provide.

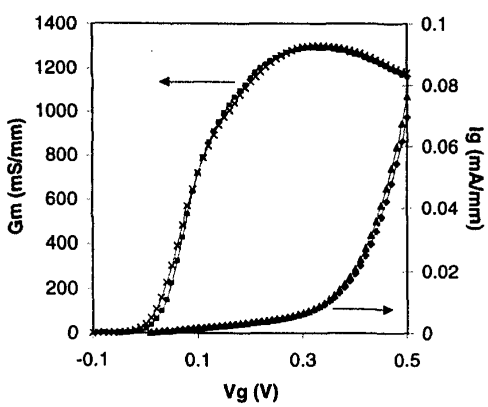

Figure 4. Transconductance (Gm) and gate current (Ig) as a function of gate voltage (Vg), measured at a drain bias of 0.7 V and 12 degrees Kelvin. Two curves almost conciding: one measured in dark and one with light.

The cryogenic noise performance of the W-band LNA showed a dependency on the layout of the 40 μm HEMT devices. The best cryogenic noise performance was achieved with circuits utilizing 2-finger devices in each of the 4 stages, compared to 4-finger devices. The LNA with 2-finger devices showed about 15 K lower noise temperature and improved gain compared to that of the LNA with 4-finger devices, as well as improved input return loss and gain flatness. The improvements are partially attributed to the lower parasitic fringing capacitance (Cdg ~20% less, and Cgs ~9% less) associated with the gate/mesa crossover of the 2 finger devices compared to the 4-finger devices.

A photo of a 3-stage X-band MIC LNA is shown in Figure 7, and Figure 8 shows the measured and modeled performance of the 3-stage MIC LNA operating from 6 to 12 GHz at 12 Kelvin. It shows a minimum noise temperature of 3.5 K at 8.4 GHz with 36 dB gain. The MIC LNA employs InP HEMT coplanar discrete devices with periphery of 200 μm. Each of the devices is biased at a drain voltage of 0.65 V and drain current of 3.5 mA.

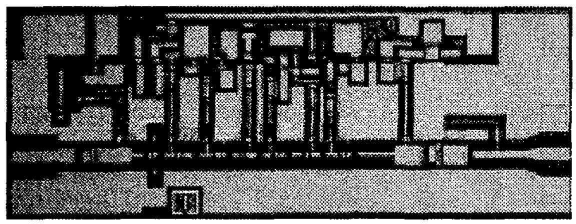

Figure 5. Photo of a 4-stage coplanar-design InP HEMT MMIC LNA whose dimensions are 0.8 x 2.1 mm.

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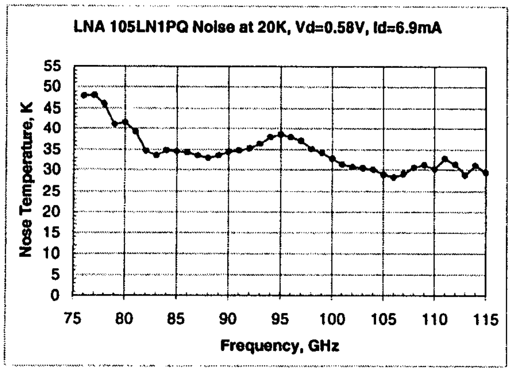

Figure 6. Measured noise temperature performance of the W-band, 4-stage, coplanar-design InP HEMT MMIC LNA measured at 20 K at a drain bias of 0.58 V and total current of 6.9 mA.

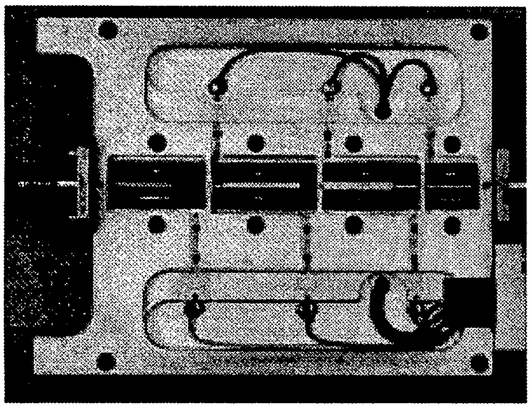

Figure 7. Photo of the 3-stage X-band MIC LNA.

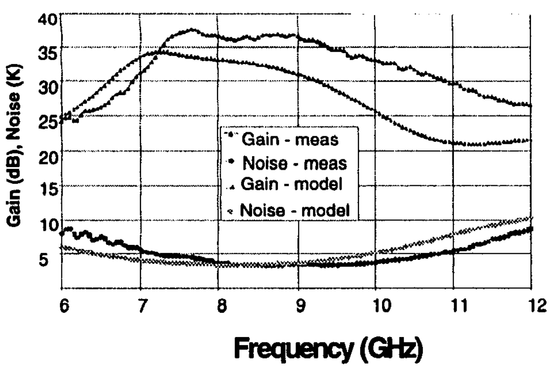

Figure 8. Measured and modeled noise temperature and gain of the X-band, 3-stage MIC LNA measured at 12 K.

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