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SPIE.

Event: SPIE Astronomical Telescopes + Instrumentation, 2018, Austin, Texas, United States

A near-infrared pyramid wavefront sensor for Keck adaptive optics: real-time controller

Sylvain Cetre^a, Olivier Guyon^b, Charlotte Bond^c, Mark Chun^c, Dimitri Mawet^d, Peter Wizinowich^a, Charles Lockhart^c, Sean Goebel^c and Ed Wetherell^a

^aW.M.Keck Observatory, 65-1120 Mamalahoa Highway, Kamuela, HI 96743, USA

^bSubaru Telescope, National Astronomical Observatory of Japan, 650 North A'ohoku Place, Hilo, HI 96720, U.S.A

^cInstitute For Astronomy, 640 North Aohk Place, Hilo, HI 96720-2700 USA

^dCalifornia Institute for Technology, MC 249-17, 1200 East California Blvd, Pasadena CA 91125, USA

ABSTRACT

A new real-time control system will be implemented within the Keck II adaptive optics system to support the new near-infrared pyramid wavefront sensor. The new real-time computer has to interface with an existing, very productive adaptive optics system. We discuss our solution to install it in an operational environment without impacting science. This solution is based on an independent SCEXAO-based pyramid wavefront sensor real-time processor solution using the hardware interfaces provided by the existing Keck II real-time controller. We introduce the new pyramid real-time controller system design, its expected performance, and the modification of the operational real-time controller to support the pyramid system including interfacing with the existing deformable and tip-tilt mirrors. We describe the integration of the Saphira detector-based camera and the Boston Micromachines kilo-DM in this new architecture. We explain the software architecture and philosophy, the shared memory concept and how the real-time computer uses the power of GPUs for adaptive optics control. We discuss the strengths and weaknesses of this architecture and how it can benefit other projects. The motion control of the devices deployed on the Keck II adaptive optics bench to support the alignment of the light on the sensors is also described. The interfaces, developed to deal with the rest of the Keck telescope systems in the observatory distributed system, are reviewed. Based on this experience, we present which design ideas could have helped us integrate the new system with the previous one and the resultant performance gains.

Keywords: Real-Time Control, Pyramid Wavefront Sensor, Adaptive Optics

1. INTRODUCTION

The current Keck II¹ and Keck I NGS AO systems were commissioned in 1999 and 2001, respectively. The Keck II,^{2,3} and Keck I⁴ LGS AO system, upgrades to the existing NGS AO systems, began science operations in 2004 and 2012, respectively. Through April 2017 a total of 794 refereed science papers were published based on data from the Keck AO systems, including 300 based on LGS AO data.

A near-infrared pyramid wavefront sensor (PWS)⁵ is being developed for the Keck II adaptive optics (AO) system with National Science Foundation funding to carry out a pilot L-band imaging coronagraph survey of 150 M dwarfs to identify exoplanet candidates. The abundance of M-type stars, their low close binary fraction, and the ubiquitous presence of massive proto-planetary disks at young ages imply that they are common sites of planet formation. Unfortunately the faintness of these stars at optical wavelengths has made them difficult to observe at the required contrast and spatial resolution to detect exoplanets with current AO systems. These stars are however sufficiently bright in the near-infrared to be used as AO guide stars. The planet to star contrast ratio is particularly favorable in L-band and a suitable L-band vortex coronagraph is implemented in the NIRC2 science camera that is fed by the Keck II AO system. The choice to develop a near-infrared PWS

Further author information: (Send correspondence to W.M.K.O.)

W.M.K.O.: E-mail: sctre@keck.hawaii.edu, Telephone: +1 (808) 881 3888

Adaptive Optics Systems VI, edited by Laird M. Close, Laura Schreiber,
Dirk Schmidt, Proc. of SPIE Vol. 10703, 1070339 · © 2018 SPIE
CCC code: 0277-786X/18/\$18 · doi: 10.1117/12.2311781

was driven by the high performance of visible PWS, the recent availability of near-infrared e-APD arrays, and measured performance improvements using a near-infrared tip-tilt sensor with the Keck I laser guide star (LGS) AO system.⁶ The near-infrared PWS will be a key component of the Keck Planet Imager and Characterizer (KPIC) project.⁷ The characterizer part of KPIC includes a fiber injection unit⁸ (FIU) that will feed exoplanet light to the NIRSPEC spectrograph. The PWS is closely integrated with the FIU to provide the wavefront sensing.⁹ The opto-mechanical design will also support the use of off-axis guide stars using a field steering mirror (FSM) assembly. This is not required for science with the NIRC2 vortex coronagraph or FIU. However, the use of off-axis guide stars will facilitate more general NGS AO science with NIRC2 (e.g. observations of the dust obscured galactic center) and provides a platform for the future use of the near-infrared system for low order sensing as part of the LGS AO system.

This paper will focus mainly on the AO system and its RTC. Each Keck AO system includes a visible Shack-Hartmann wavefront sensor and a quad cell avalanche photodiode based, tip-tilt sensor (known as STRAP) developed by Microgate and ESO. Both AO systems are controlled by a wavefront controller (known as MGAOS) developed by Microgate. This control system was deployed in 2006¹⁰ and has been in operation since. It offers powerful and reliable performances, thanks to its FPGA/DSP architecture, but it is challenging to add new hardware and/or to modify the software. The PWS will allow the Keck AO system to perform correction in the infrared wavelength. In order to optimize the development time, we decided to adapt the SCEXAO¹¹ architecture to this project. The main challenge with this configuration is that the new RTC had to live in parallel with the operational RTC without impacting it.

2. SYSTEM OVERVIEW

The existing Keck II AO bench was modified to insert the PWS sensor plate and the FIU for NIRSPEC. A choice of a dichroic beamsplitter or mirror is inserted in front of the NIRC2 science camera to send light to the FIU and PWS. This motorized device is used to switch between normal operation and operation with the PWS and FIU. The 349 actuators Xinetics deformable mirror and the down tip-tilt mirror are used in both cases (with the existing Shack-Hartmann or with the pyramid).

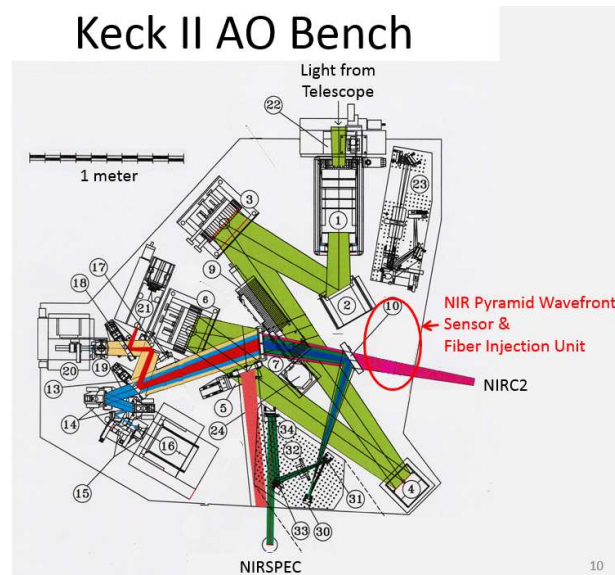


Figure 1: Keck II AO bench light path to NIRC2. A dichroic beamsplitter or mirror can be inserted in front of NIRC2 to send the light to the PWS and FIU located in the red circled area.

The concept¹² is shown in Figure 2. When NIRC2 is the science instrument a dichroic beamsplitter is inserted in the beam to NIRC2 to reflect light to the PWS. When using the FIU to feed NIRSPEC a mirror is inserted in

the beam to NIRC2. In both cases the existing Keck AO system opto-mechanics are used including the existing deformable and tip-tilt mirrors.

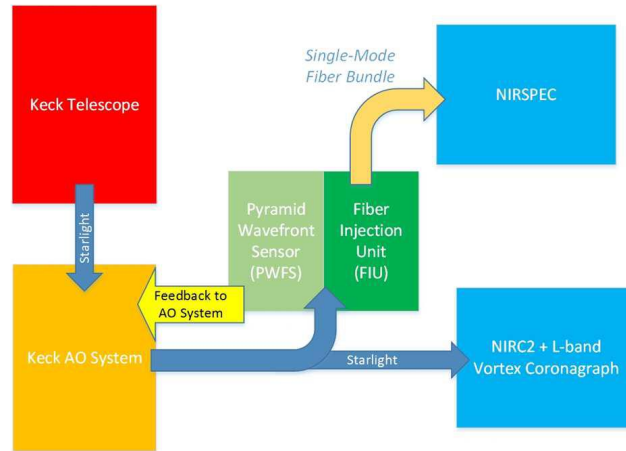


Figure 2: Overview Block Diagram.

A subsystem of this project is the new real-time controller (RTC). The new RTC interfaces with the operational RTC to control the existing deformable and tip-tilt mirrors. The new RTC runs on a standard x86 architecture computer deployed in the Keck summit network, running a 64-bits version of Linux.

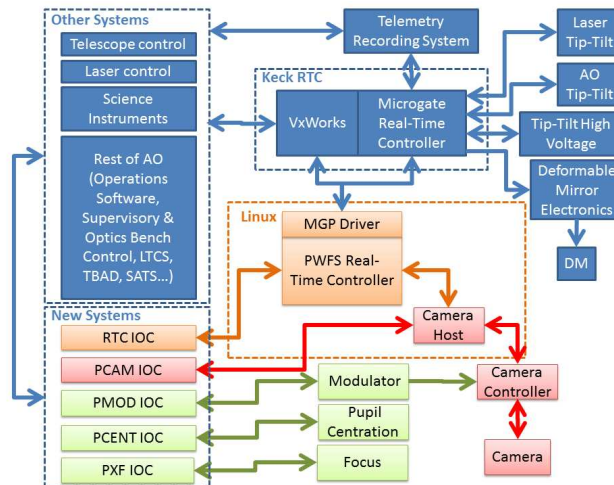


Figure 3: Overview of the Pyramid AO RTC: The new Linux-based RTC (orange) interfaces with the existing Keck RTC (blue) in order to control the existing deformable and tip-tilt mirrors. The new RTC is physically connected to the PWS camera host to control the PWS camera. The new PWS devices include a modulator which synchs the camera frames, a pupil centration stage to register the pupil to the camera pixels, and a focus stage to maintain the pyramid tip conjugate to the science detector.

New motion control devices have been added to the system to ensure stability, alignment and performance. An additional MEMS deformable mirror with about 1000 actuators will be deployed as part of the FIU in the NIRSPEC branch and will be also controlled by the RTC. The new RTC communicates over the network using the Keck Task Library¹³ (KTL) and the Experimental Physics and Industrial Control System¹⁴ (EPICS). It is part of the distributed environment and it can communicate with any subsystem (telescope, science instruments, etc.).

3. DESIGN

3.1 Camera System¹⁵

The PWS camera, provided by the University of Hawaii Institute for Astronomy (IfA), contains a near-infrared SAPHIRA detector.

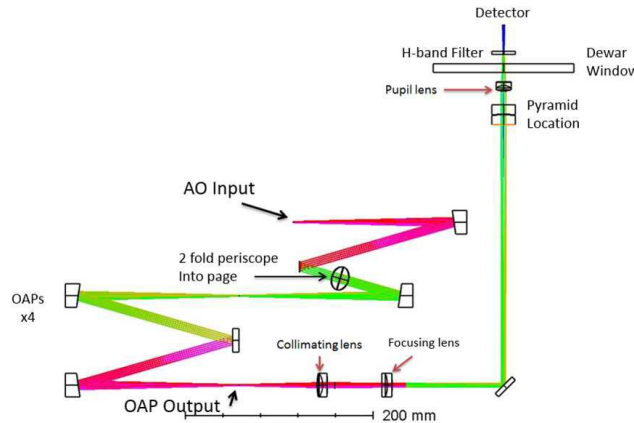


Figure 4: Optical path from the AO input to the PWS detector.

The light reflected to the PWS (the AO Input in Figure 4) reflects off multiple off-axis parabolas (OAPs) until it reaches the collimating lens. A collimating lens, mounted on a focus stage, and focusing lens are used to reimage the AO input focus onto the tip of the pyramid. After going through the pyramid optics, the light goes through a Pupil lens which is mounted on a pupil centration stage.

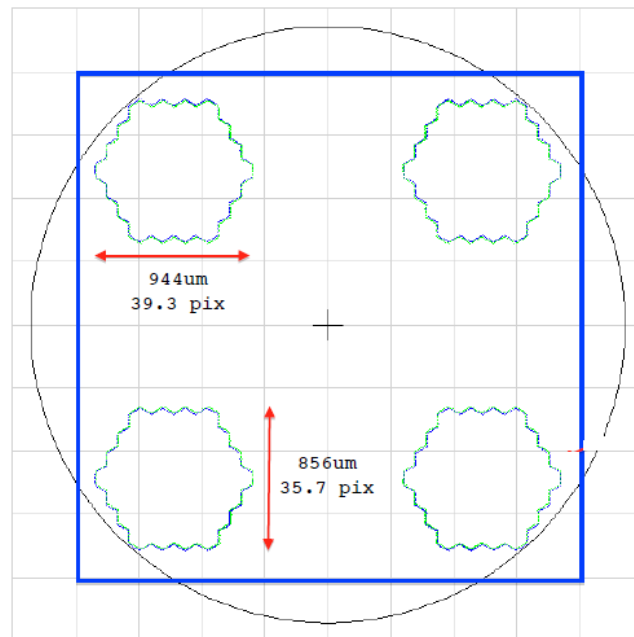


Figure 5: Representation of the four pupils on the 128x128 pixels area of the detector. Each pupil has a diameter of about 40 pixels.

The optics bench is designed to create four pupils each 40 pixels across. The camera reads 32 pixels at a time per row and then it reads to the next 32 pixels on the same line and so on. The number of columns of the final

region of interest will be a factor of 32. Each line is read individually. Each pupil will require reading 64x64 pixels in order to accommodate the 40 pixel pupil diameter. The four pupils will be read in a 128x128 region of interest.

The Saphira camera is installed in a dewar, looking down on the AO bench. It is cooled down with glycol lines connected to the Keck facility glycol system. Its electronics send the pixels information over an USB 3.0 connection to the RTC.

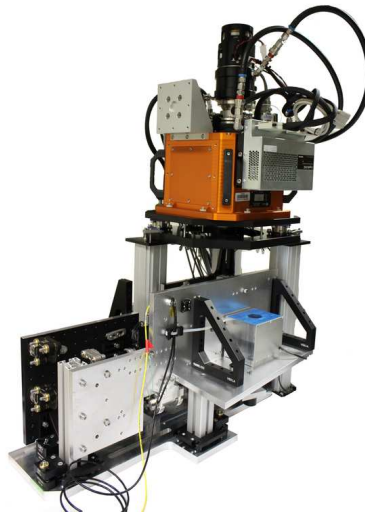


Figure 6: Saphira camera mounted on top of the PWS and FIU optical plates.

A software package developed by the IfA runs on the RTC and provides control of the camera. The code extracting the pixels is specific to our AO solution. This code writes directly in a shared memory of the RTC. This software allows connection to the camera electronics to configure gain, fixed exposure time, external trigger readout, etc.

3.2 Real-time Control System

The new PWS RTC interfaces with the existing Keck MGAOS RTC. The MGAOS RTC has been in operation since 2006 and has been a very productive system ever since. The new system is designed to reduce impact on operations by minimizing cables handling, software re-configuration, etc. The new RTC is based on an open source solution, CACAO.¹⁶

3.2.1 CACAO Solution

The Compute And Control for Adaptive Optics (CACAO)¹⁷ is an open source software package written in C, optimized for performance using multi-core CPUs and GPUs for high computing throughput. The main functionalities of this solution are:

- The Shared Memory: all the data (images, dark, slopes, DM commands, etc.) go to shared memory. The CACAO solution provides a C structure organizing the data in the shared memory. Individual data are identified as a unique name and can be read or written from C or python processes. The code is also based on IPC semaphores. They are used to synchronize the different processes and how the latter access the data in the shared memory.
- The computational processes: originally developed in C for performance purpose, we re-used a python layer on top of the shared memory to easily and quickly test algorithms. Currently, there are two ways to close

the pyramid AO loop: one using the SCExAO based algorithm in C and the other using a slope-based algorithm in python. The code can run on both CPU and GPU for AO loop computation.

- The input processes: the RTC is fed with pixels by a dedicated process. It reads the information coming from the USB 3.0 connection and it writes the image in the shared memory. This software is written in C to provide fast processing.
- The output processes: once the RTC has computed new commands to apply on the deformable mirror and the tip-tilt mirror, it writes the results in another shared memory. A dedicated process is waiting for any new command to arrive in the shared memory. Then it sends the command to the device using the appropriate drivers.
- The satellites processes: They are all the processes not used for real time control. It can be an archiver, graphical user interface, the Keck interface, etc.

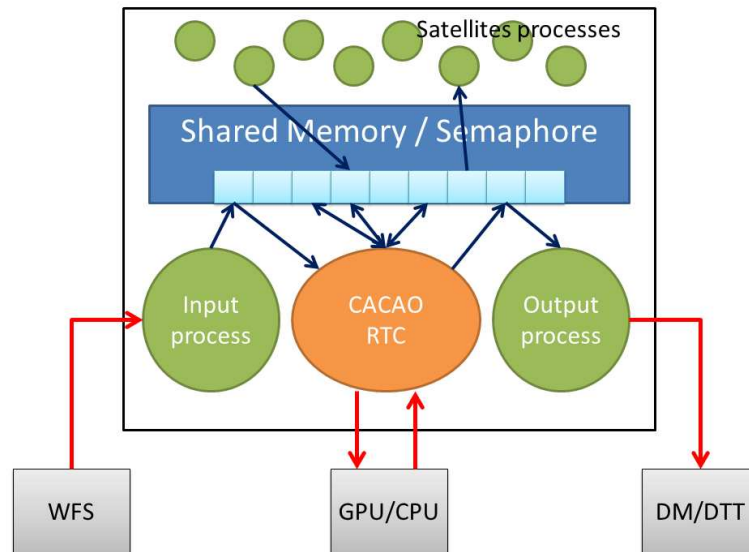


Figure 7: RTC processes organization.

CACAO is using CUDA, CuBLAS and MAGMA for GPU acceleration. It re-uses standard libraries (gsl, fitsio, libtool) which allow it to run on almost any Linux distribution. CACAO is easily scalable and computation is easily optimized. For example, we are implementing 2 separate loops in our PWS system: one controlling the Xinetics DM 349 and one controlling the Boston kilo-DM. These loops will not run in parallel since they use the same PWS. The two mirrors will live in parallel in the CACAO environment. The creation of the DM entity is very simple: it consists of writing a configuration file describing the DM architecture.

3.2.2 Hardware

The RTC is based on a x86 architecture linux server. It is easily scalable. The RTC is using Dual Processors with multiple cores Intel(R) Xeon(R) Gold 6126 CPU @ 2.60GHz, with 48 cores total. Resources are reserved for specific tasks, like input, output and computational processes.

One Geforce GTX 1080 ti Graphical Processing Unit, used for AO computation is installed in the RTC. In order to have a dedicated computing unit to run the predictive control algorithm, a second GPU will be installed in future to have a dedicated computing unit to run a predictive control algorithm. It provides a powerful computational unit to deal with the AO matrix products.

The AO system reuses the Xinetics deformable mirror currently in operation. This mirror and the tip-tilt mirror are physically connected to the operational Microgate RTC. In order to communicate with these mirrors,

the new RTC uses a modified version of the Microgate protocol drivers, allowing the re-use of some of the functionality of the Microgate RTC. These functionalities were provided originally to be used with a VxWorks interface. Additionally, a modified version of the embedded firmware provided by Microgate helps to reduce the latency and jitter when driving the mirrors with this drivers.

A additional Boston Micromachine deformable mirror (kilo-DM) will be connected to the RTC as part of a funded upgrade to the FIU. A new DM process will be deployed on the RTC using the Boston Micromachine drivers.

3.3 Motion Control System

For alignment and optimization, several actuated devices are needed on the AO bench.

- A new dichroic has been installed to send the beam to the new pyramid optical plate where the new sensor is installed. This dichroic is controlled by the existing observatory Delta Tau PMAC based controlled system. To reduce the impact on the existing system we used an existing channel: we only need to connect the stage without modifying the controller hardware. The controller software has been updated to match the stage.
- A focus stage for the PWS is connected on a Turbo PMAC VME crate. This stage will be used to ensure the sensor is conjugate to the NIRC2 focal plane or the fiber feeding NIRSPEC, depending on the science mode.
- A modulator is installed in front of the pyramid optics. The modulator is connected to a Burleigh amplifier. This amplifier is connected to a Teensy controller which controls the amplitude and phase of two sine waves (one for each axis) in order to drive the image in a circle around the tip of the prism. The modulator also provides a trigger signal to start the readout of the detector. It allows us to control the exposure time of the camera and to synchronize the modulation.
- A two-axis stage moves the pupil reimaging optics after the pyramid to register the camera pixels to the DM actuators.

3.4 Observatory Interface

A light python server runs on the real time computer providing an interface to the CACAO software. It uses a specialized python module which provides access to the computer shared memory. It allows to perform all the required operations needed by the observer (open/close the loops, change loops gain, load new reconstructor, etc.). This server has almost no impact on the multi-core computer. Several EPICS IOCs provide the entry point to the RTC, camera and motion control for the rest of the Keck subsystems (telescope, operational software, etc.). A Keywords layer is provided for operation. EPICS interfaces are available to control the RTC, the camera, the modulator, the pupil stabilization, the focus stage and the dichroic.

4. PERFORMANCE

The PWS is planned to be installed at the telescope in September 2018. The following numbers have been measured using benchmarks and simulations. The camera was tested in its integration lab, and the spare hardware of the Keck AO system was used to measure the drivers response. These numbers give a good approximation of what will be the latency of the system. The reconstruction measurements were performed on the final computer using the GPU that will be used on sky. These performances are evaluated for the system using the Xinetics 349 actuators. Once the Boston kilo-DM will be available, we should see a major improvement in the latency thanks to the much faster connection to the DM electronics. The benchmark shows that, thanks to the number of cores in the recent GPU, no major performance reduction will be shown in the matrix computation.

4.1 Latency

The latency is computed by adding up different times measured during the computational process. The configuration of the camera, the GPU computational power and the device drivers implementation are the source of the latency. The following measurements were done for 4 pupils (40x40 pixels) on the PWS and the Xinetics DM 349 actuators.

The maximum speed at which the camera can run depends on the pixel rate. This parameter is programmable to up to 2 Mhz. We are planning to use the 1 Mhz pixel rate which is very stable and robust to start with. Based on this pixel rate, the actual maximum frame rate used is 1.41 kHz. The readout of the camera is triggered by the modulator controller allowing us to synchronize the modulation and the image acquisition. This camera speed gives an integration time of 709 μ s. The transfer time, using USB, of the 128x128 16 bits image take 171 μ s, based on an ADC+USB3.0 speed of 192 MBps. The transfer of the image to the GPU on the PCIe bus takes about 1.76 μ s. The duration of the matrix computation inside the GPU is about 24.74 μ s. The transfer of the resulting DM command on the PCIe bus takes 0.94 μ s. The total time spent in the transfer to the GPU plus in the GPU is about 27.44 μ s. Once in the shared memory, it triggers the mgpDriver which needs 124 μ s to transfer the DM command to the DM electronics. These measurements were performed in the laboratory system using the spare MGAOS hardware. The response time of the DM actuators is specified at 250 μ s. If we consider the following definition of the latency:

$$Latency = \frac{1}{2}exposure + readout + transfer + processing + DMdrivers + DMelectronics + DMphys$$

$$Latency = 1.636 \text{ ms}$$

For a camera pixel rate of 1 MHz, we compute a latency of 1.636 ms.

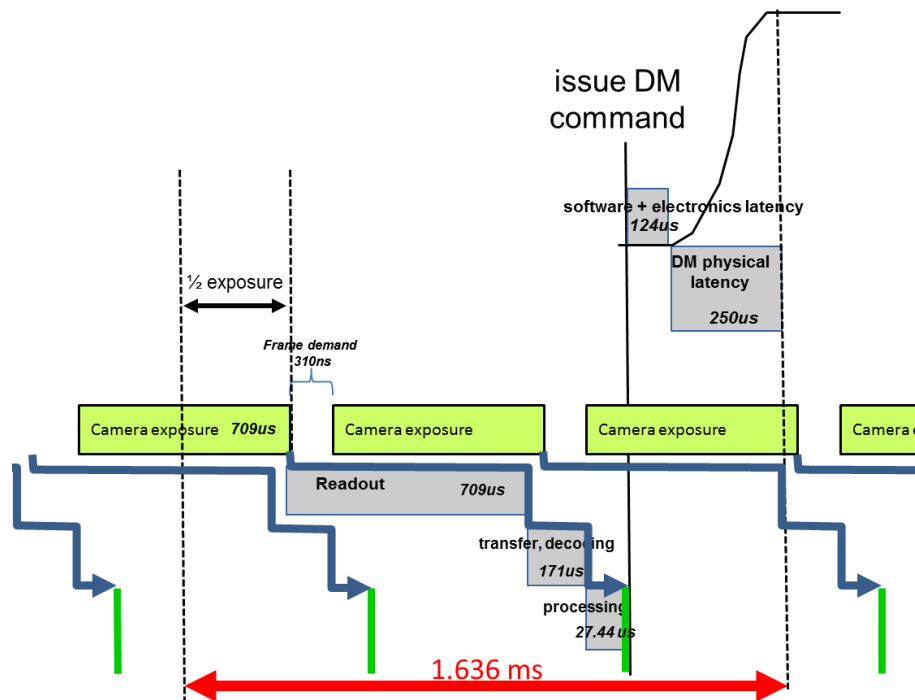


Figure 8: System latency (the time scale is not respected)

We could not measure the actual response of the Kilo-DM drivers and physical move but we could see the impact of the increased size of the DM on the GPU timing. Using the MEMS will add about 10 μ s of latency. This time increase will be more that compensated by the better timing of the drivers and mirror response.

Table 1: Comparison of GPU performances for the Xinetics 349 and the Boston Kilo-DM

	DM349	Kilo-DM
Host to Device	1.76	1.75
Computation	24.74	34.37
Device to Host	0.94	1.05
Time (μs)	27.44	37.17

4.2 Jitter

The latency and expected performance were determined mainly using statistics and do not take into account the jitter. Simulations running on the RTC impact the final performance. We present in this section the jitter measured at the GPU level. A final measurement of the total jitter will be performed once all the devices are installed and aligned. Thanks to the Nvidia profiler tool, we were able to have a better estimation of the jitter introduced by the GPU. All these tests will be redone once the system is fully installed on the Keck II AO bench.

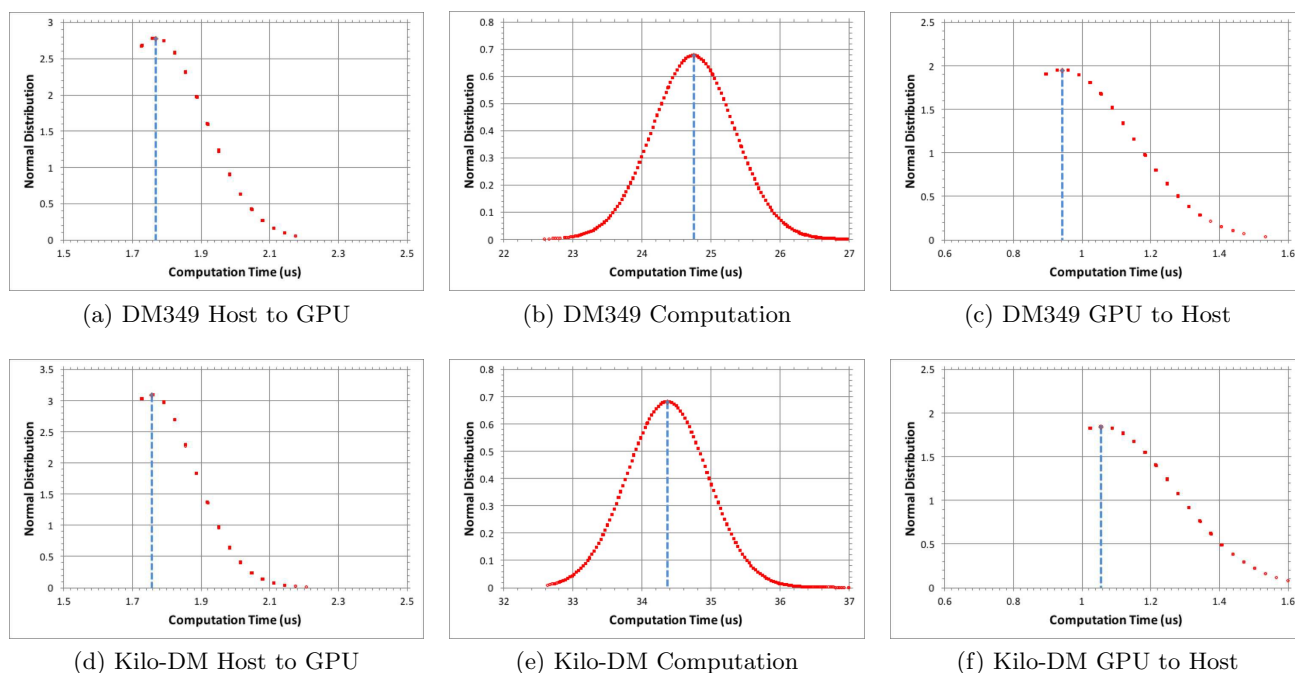


Figure 9: GPU timing for Xinetics DM349 and Boston Kilo-DM for a sample of 10000 computations.

The previous graphics represents the time spent in the 3 main step of the GPU computation sequence for DM349 and kilo-DM respectively. (a) and (d) graph represents the time to transfer the data from the host to the GPU, (b) and (e) graphs are the time used by the GPU to compute the Matrix Vector product and (c) and (f) graphs are the time spent to transfer back the DM commands from the GPU to the host. We measure the jitter by computing the standard deviation of the time spent in the GPU for a sample of 10000 computations.

Table 2: Comparison of GPU jitter for the Xinetics 349 and the Boston Kilo-DM

	DM349	Kilo-DM
Host 2 Device	143	128
Computation	590	585
Device 2 Host	204	216
Total Jitter (ns)	937	929

The expected jitter is **937 ns** for the Xinetics DM349 and **929 ns** for the Boston Kilo-DM. These results

show that the jitter is not really impacted by the matrix size and should not impact the final performance.

4.3 Improvements

A better characterization of the performance will be performed once the system is fully assembled. The physical location of the different devices and the intensive use of the old system make it challenging to perform such measurements.

A way to improve the performance would be to directly connect the DM and the DTT to the RTC. It would allow to reduce the 124 μ s spent in the mgpDriver. The funded Keck II RTC upgrade will do this.

There is a double write of the image in the shared memory which can be replaced by a direct memory access of the GPU; instead of writing the image in the shared memory and having an external process extracting it and sending it to the GPU, it will be possible to directly write to the GPU memory from the readout process. It will save about 20 μ s.

Another improvement that will come in the near future is the increase of the camera pixel rate. It will allow the system to run faster. A pixel rate of 2 MHz is under implementation and will allow the system to run almost twice as fast. A rough estimate, using a camera frame rate of 2.82 kHz, gives a latency of 1.103 ms.

Table 3: Comparison of the expected performance for a pixel rate of the camera of 1 MHz and 2 MHz

	1 MHz pixel rate	2 MHz pixel rate
1/2 exposure	354	177
exposure	709	354.5
transfer	171	171
processing	27.44	27.44
DM drivers + electronics	124	124
DM physical move	250	250
Latency (us)	1636	1103

In general, a simple improvement such as an upgrade of the system with newer and more powerful CPUs is sufficient. It will allow better data transfer (to/from shared memory) and less jitter in the CPU operations.

A dedicated project to use predictive control is being planned. It will require a dedicated computational unit.¹⁸

5. CONCLUSION

The main challenge was to integrate the system in parallel with the existing operational one. The solution is convenient because it protects the existing hardware preventing the disconnection of the deformable mirror and the tip tilt mirror. However it comes at a cost in latency. Even with the loss of performance, we decided to preserve the operational system. A powerful interface allowing control of the existing system devices is an advantage for prototyping new solutions and will save development time in the future upgrades. A project to make a facility class instrument of the PWS is planned.

CACAO provides a very interesting solution to quickly implement an AO system using a pyramid wavefront sensor independent of the hardware with little loss in performance. It is a very scalable solution which can be deployed in a few days. It allows the system development team to focus on their hardware interface. The required development is writing of the independent processes into the shared memory and the processes reading from the shared memory. The performance will increase with time by upgrading the system with newer computational units (CPUs and GPUs) and probably without the need of any software changes. The open source Linux x86 architecture will allow this quick upgrade.

ACKNOWLEDGMENTS

The near-infrared PWS is supported by the National Science Foundation under Grant No. AST-1611623. The fiber injection unit is supported by the Heising-Simons Foundation. The PWS camera was provided by Don Hall as part of his National Science Foundation funding under Grant No. ASF-1106391. We would like to acknowledge the technical contributions of Kevin Tsubota, Sam Ragland, Jason Chin, Jon Chock at WMKO, Eric Warmbier at IfA, Nemamja Jovanovic, Jacques-Robert Delorme at Caltech, the SCEXAO team at Subaru and Frantz Martinache at Observatoire de la Cote d'Azur. Finally, we would like to thank Accelerate Diagnostics for providing the first GPU used in the RTC. The W. M. Keck Observatory is operated as a scientific partnership among the California Institute of Technology, the University of California, and the National Aeronautics and Space Administration. The Observatory was made possible by the generous financial support of the W. M. Keck Foundation. The authors wish to recognize and acknowledge the very significant cultural role and reverence that the summit of Mauna Kea has always had within the indigenous Hawaiian community. We are most fortunate to have the opportunity to conduct observations from this mountain.

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