A FULL WAVEGUIDE BAND MMIC TRIPLER FOR 75-110 GHZ

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Abstract — **Design and test data for a full waveguide band MMIC tripler using anti-parallel Schottky diodes are reported in this paper. The circuit outputs between –3.7 dBm and +2.0 dBm from 75 to 110 GHz. When tuned for power flatness, the output is between –4.6 dBm and –1.3 dBm across the band. The conversion efficiency is about 1.5% in both cases. To the authors' knowledge, this is the first reported MMIC frequency tripler to cover the entire W-Band.**

I. INTRODUCTION

Signal sources in W-Band are of interest for various applications including atmospheric remote sensing, automotive radar systems, and test instrumentation. A popular approach to generating these signals is to cascade a low-frequency source with one or more multipliers. This takes advantage of the superior oscillator technology at lower frequencies.

Many types of multipliers can be used. Both doublers [3]-[4] and triplers [5]-[10] have been reported. Some designers favor transistor multipliers [9]-[10], citing improved conversion loss. However, diode multipliers are more common in the millimeter-wave range, owing to improved frequency response and stability. Unfortunately, most of the reported circuits do not cover the full waveguide bandwidth. Two notable exceptions are the commercially available components produced by Millitech [5] and Pacific Millimeter Products [6]. These waveguide circuits deliver on the order of 1 mW across W-Band with 2% conversion efficiency. However, Monolithic Millimeter-Wave Integrated Circuits (MMICs) are often preferable to waveguide circuits due to their compactness, repeatable performance, and low-cost fabrication in large quantities. This paper describes the design and evaluation of a wideband MMIC tripler using planar Schottky diode technology.

II. DESIGN

The tripler was designed around an anti-parallel diode pair. This configuration is useful for producing the third harmonic of the drive frequency while suppressing the even harmonics [7]. Suppression of the 4th harmonic is of particular importance in this design because at some frequencies it will fall within the designed output band. For example, an input signal at 26 GHz will lead to the desired output at 78 GHz, as well as an undesired tone at 104 GHz. This spurious component cannot be rejected by filtering because that would also attenuate the desired signal for inputs at the high end of the band.

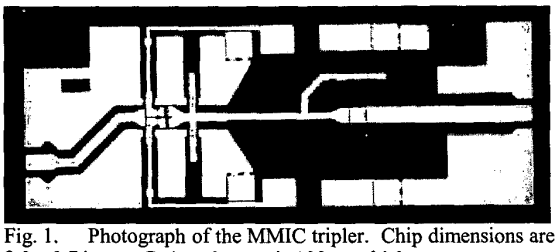

Fig. 1. Photograph of the MMIC tripler. Chip dimensions are 2.0 x 0.74 mm. GaAs substrate is 100 μm thick.

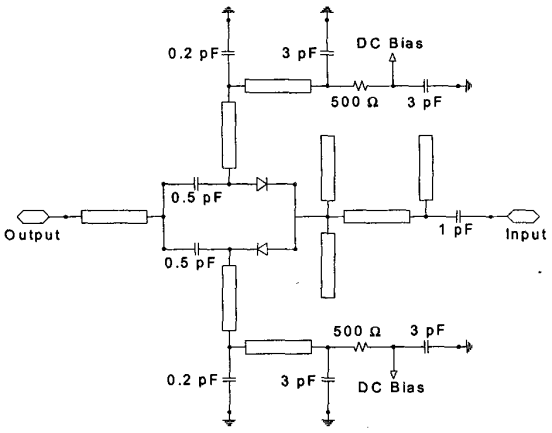

Fig. 2. Schematic of the tripler, showing MIM capacitors, thin-film-resistors, and transmission line sections.

A photograph of the chip appears in Figure 1, and a schematic is shown in Figure 2. The microstrip network on the input port is designed to provide a conjugate match from 25-37 GHz. The tuning-stub incorporates a series of air-bridges along its length. This was done in order to

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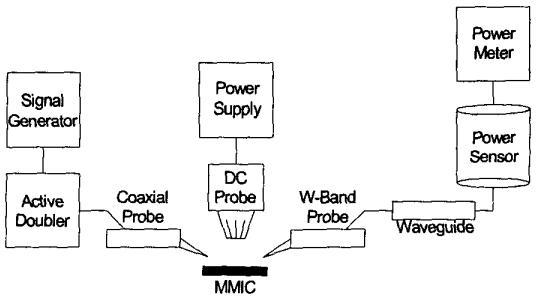

Fig. 3. Block diagram of the test setup.

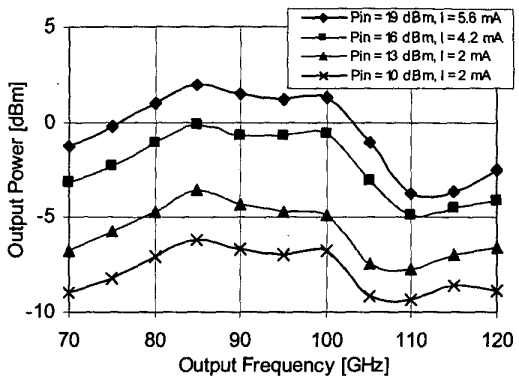

Fig. 4. Output power vs. frequency. The chip was biased with the indicated constant current values. Little change was noted with constant voltage bias.

allow minor adjustments to be made after fabrication. By selectively breaking one of these air-bridges with a needle probe, the length of the stub can be shortened. After the matching network is a pair of open-circuited stubs designed to present an approximate short-circuit at the diodes from 75-110 GHz. This provides frequency isolation as well as a ground-return for the output.

The bias line for both diodes is on the output side. Bypass capacitors are located at the appropriate positions on this line to match the diodes to the output port in W-Band, while providing a ground-return for the input frequency. Thin-Film resistors were included in the bias path to protect the sensitive diodes from static damage. The output transmission line network consists entirely of grounded coplanar waveguide. Via holes were placed at quarter-wavelength intervals in the topside ground-planes to suppress parallel plate modes.

The circuit design described above was entered into HP's Advanced Design System (ADS). Using the optimization routines provided with this software, the passive network parameters, such as transmission line

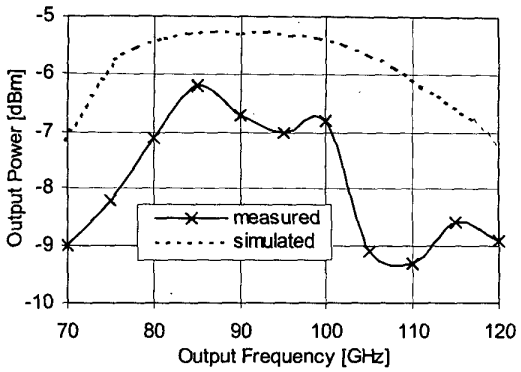

Fig. 5. Measured and simulated output power vs. frequency. Input power was 10 dBm, and bias current was held constant at 2 mA.

lengths and impedances, were allowed to vary within a 10% range of their original values. A gradient search algorithm was used to explore this parameter space and design a tripler with output power variation of ±1 dB over the frequency range from 75-110 GHz.

The chips were fabricated by United Monolithic Semiconductor (UMS) using their BES Schottky Diode MMIC process. Anode dimensions of 1x3 μm were selected for high frequency performance. This diode exhibits low junction capacitance of approximately 6 fF and series resistance of 7 Ω, resulting in a calculated cutoff frequency over 3 THz. The GaAs substrate thickness is 100 μm and the chip dimensions are 2.0 x 0.74 mm.

III. Measurements

Scalar measurements were performed on several chips. A block diagram of the test setup is shown in Figure 3. The input signal was provided by an active frequency doubler (DBS Microwave model DB99-0356) driven by an HP 83620B Signal Generator. The input signal was coupled into the chip through a GGB Industries coplanar wafer probe. Output power was measured with an HP W-Band Power Sensor. The losses in the waveguides and probe-transitions, typically about 1-1.5 dB, were calibrated out, so the data represents the performance of the chip alone. Bias current was supplied to the chip through needle probes.

Output power versus frequency for various bias conditions and drive levels are shown in Figure 4. Between –4 dBm and +2 dBm was measured across the band for high drive level. Figure 5 shows the simulated performance along with measurement under the same drive

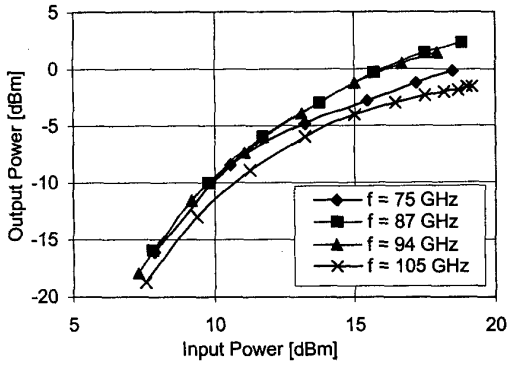

Fig. 6. Output power vs. input power. Input power was swept up to the limits of the test setup. The chip was biased with a constant current of 4.2 mA.

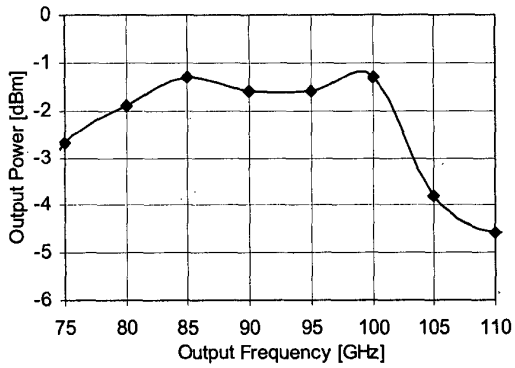

Fig. 7. Output power vs. frequency after trimming the input tuning stub and optimizing bias for power flatness. Input power was +16 dBm, and the chip was biased with a constant 3.7 V.

conditions. In general, the chip delivered 1-3 dB less power than predicted. Output power versus input power for several frequency points is plotted in Figure 6, showing that the tripler was not saturated during these measurements. This suggests that higher output power is achievable.

An attempt was made to improve the power flatness by trimming the input tuning stub. The middle air-bridge on this stub was broken with a needle probe and micro-manipulator. Also, the bias voltage was adjusted to optimize the conversion loss at the worst frequency point, anticipating a sacrifice in output power at other frequencies. The result of this adjustment is plotted in Figure 7. For input power of 16 dBm, the chip delivered between –4.6 dBm and –1.3 dBm from 75-110 GHz.

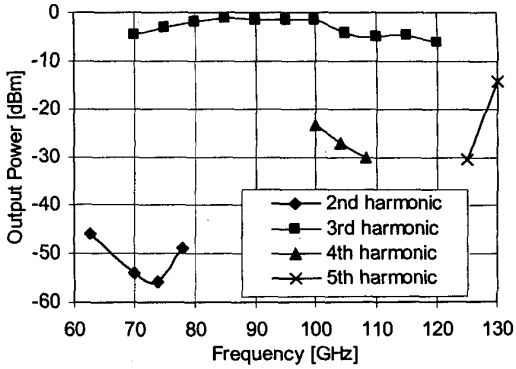

Fig. 8. Output power versus frequency for the 2nd through 5th harmonics. Input power was +16 dBm, and the chip was biased with a constant current of 4.2 mA.

Additional tests were performed to characterize the output power spectrum of the triplér. This data is shown in Figure 8. Of critical importance is the 4th harmonic from 100-110 GHz, the range over which both the 3rd and 4th harmonics fall within the designed output band. As the plot shows, the 4th harmonic is more then 20 dB below the desired output. The 5th harmonic is not so well suppressed by the MMIC, measured as high as –14 dBm, but at 130 GHz this tone is far enough out of band to be filtered easily.

IV. Conclusion

A full W-Band MMIC frequency tripler has been presented. The design uses a pair of 1x3 μm planar Schottky diodes on GaAs in the anti-parallel configuration. It delivers up to 0.74 mW of power with no more than 3.3 dB variation from 75-110 GHz. This is believed to be the first MMIC tripler reported to provide relatively flat output power across the entire W-Band. Plans are already being made to integrate this chip with a full W-Band power amplifier MMIC [12] to create a 50 mW power source in a compact multi-chip module.

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REFERENCES

[1] P. Penfield and R. Rafuse, *Varactor Applications*, Cambridge, MA: MIT Press. 1962.

[2] S. Maas, *Nonlinear Microwave Circuits*, New York, NY: IEEE Press, 1997.

[3] S. Chen, T. Ho, F. Phelleps, J. Singer, K. Pande, P. Rice, J. Adair, and M. Ghahremani, "A high-performance 94-GHz MMIC doubler," *IEEE Microwave Guided Wave Lett.*, vol. 3, pp. 167-169, June 1993.

[4] J. Papapolymerou, F. Bauchler, J. East, and L. Katehi, "W-Band Finite Ground Coplanar monolithic multipliers," *IEEE Trans. Microwave Theory and Tech.*, vol. MTT-47, pp. 614-619, May 1999.

[5] "Fullband Frequency Triplers," Product data sheet, REV00 C 051199, Millitech Corporation, Technology and Manufacturing Center, South Deerfield, MA.

[6] "Frequency Multipliers," Product data sheet, Pacific Millimeter Products, Golden, CO.

[7] M. Cohn, R. Freitag, H. Henry, J. Degenford, and D. Blackwell, "A 94 GHz MMIC tripler using anti-parallel diode arrays for idler separation," *IEEE MTT-S Intl. Microwave Symp. Digest*, pp. 763-766, San Diego, CA, 1994.

[8] A. Rahal, R. Bososio, C. Rogers, J. Ovey, M. Sawan, and M. Missous, "A W-Band medium power multi-stack quantum barrier varactor tripler," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 368-370, November 1995.

[9] Y. Campos-Roca, L. Verweyen, M. Fernandez-Barciela, E. Sanchez, M.C. Curras-Francos, W. Bronner, A. Hulsmann, and M. Schlechtweg, "An optimized 25.5-76.5 GHz PHEMT-based coplanar frequency tripler," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 242-244, June 2000.

[10] H. Fudem, and E. Niehenke, "Novel millimeter-wave active MMIC triplers," *IEEE MTT-S Intl. Microwave Symp. Digest*, pp. 387-390, Baltimore, MD, 1998.

[11] A. Raisanen, "Frequency multipliers for millimeter and submillimeter wavelengths," *Proc. IEEE*, vol. 80, pp. 1842-1852, November 1992.

[12] L. Samoska and Y. C. Leong, "65-145 GHz InP MMIC HEMT medium power amplifiers," *submitted to IEEE RFIC Symposium, 2001.*