Progress on a Fixed Tuned Waveguide Receiver Using a Series–Parallel Array of SIS Junctions

Nils W. Halverson[1], John E. Carlstrom[1], David P. Woody[1], Henry G. Leduc[2], and Jeffrey A. Stern[2]

I. Introduction

We are developing a 200 – 300 GHz receiver that incorporates multiple SIS junctions in a "series-parallel" configuration to achieve broadband impedance matching. At RF frequencies the junctions appear in series through capacitors, and at DC and IF frequencies they appear in parallel through inductors, so that the junctions are impedance matched to both the waveguide and the IF amplifier. Using a single fixed backshort and a full height waveguide, the receiver is designed to have a bandwidth of 100 GHz in the 230 GHz band. A similar design has been tested at frequencies around 100 GHz with excellent results by Shitov et al. (1991) and Vystavkin et al. (1993). Although our initial receiver is designed operate in the 200 – 300 GHz band, the design may be readily scaled to higher frequencies. In this paper we discuss computer and scale modeling of the device, fabrication, and preliminary test results.

II. The Design

By matching impedances at both the RF and IF ports, the sensitivity of the receiver is optimized through efficient coupling of the RF power into the junctions, and efficient coupling of the IF power into the IF amplifier. In a single SIS junction the RF input impedance is lower than the IF output impedance. At the same time the RF signal impedance in a waveguide is a few hundred ohms, while the standard IF amplifier input impedance is 50 ohms. This makes it difficult to match a single junction at both the RF and IF ports. In addition the junction has some parasitic capacitance which must be tuned out at the frequencies of interest. We have used electrically short ($<< \lambda/2$) integrated capacitors and inductors to connect an array of four SIS junctions in a series at the RF, and in parallel at the IF and DC, eliminating the mismatch problem (see Figure 1).

The series–parallel configuration also provides several other advantages. The inductors which connect the junctions in parallel are also used to tune out the junctions' parasitic capacitance. Junction uniformity is not critical since the junctions are DC biased in parallel through the inductors. Also, the match is broadband with a bandwidth of $\sim$ 100 GHz using a fixed backshort. This feature is particularly useful for the sideband separation receiver being developed at Caltech by Akeson et al. (1993), in focal plane arrays, and in multiple antenna arrays such as the forty dish Submillimeter Array proposed by NRAO. Lastly, a full height waveguide may be used, making the receiver easier to fabricate at higher frequencies.

[1] California Institute of Technology, Pasadena, CA
[2] Jet Propulsion Laboratory, Pasadena, CA

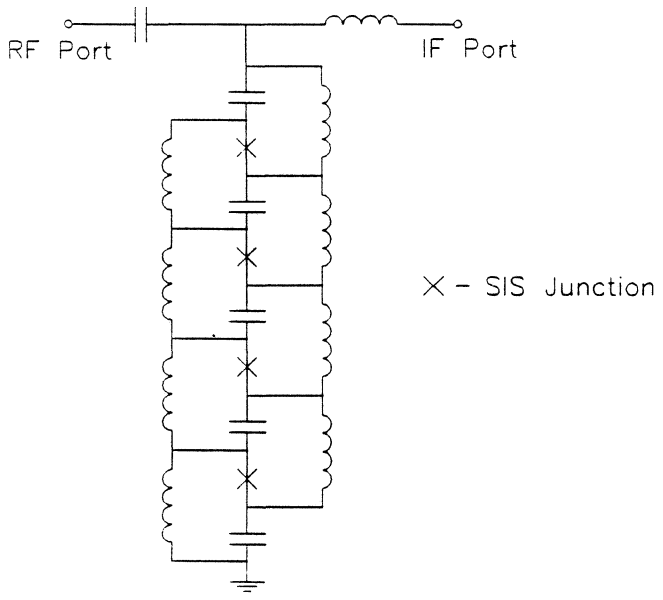


FIGURE 1. Schematic diagram for the series–parallel array of SIS junctions. The junctions, including parasitic capacitance, are represented by X's. The junctions are connected in parallel at the IF through inductors and in series at the RF through capacitors.

III. Computer and Scale Modeling

The device was computer modeled and optimized using EEsof's Touchstone[1] microwave circuit simulation program. The inductors and capacitors were modeled as lumped circuit elements, and the SIS junctions were simulated with parallel resistors and capacitors. Two basic designs were modeled, one in which the tuning elements were designed to couple RF power uniformly into each junction, and one which was stagger tuned for broader bandwidth (see Figure 2). In the stagger tuned design, the simple computer model did not take into account the variations in impedances between junctions due to unevenly coupled LO power. Testing of these devices in the near future will shed light on their feasiblity. Computer modeling predicted 40 GHz and 100 GHz bandwidth respectively for the two designs.

The tuning structures were scale modeled at 1 – 2 GHz, a scale factor of 175, in L-band full height waveguide. Terminated coplanar transmission line formulas were used to calculate inductor lengths. The circuit was etched on single sided PC board using chip capacitors and resistors to simulate the series capacitors and junctions. Delrin plastic with a dielectric constant $\epsilon_r \sim 3.8$ was used to simulate the quartz substrate. Initially, the resonance band of the scale model was significantly lower than computer model predictions, most likely due to mutual inductance between the coplanar inductors. This was

[1] EEsof Incorporated, Westlake Village, CA 91362

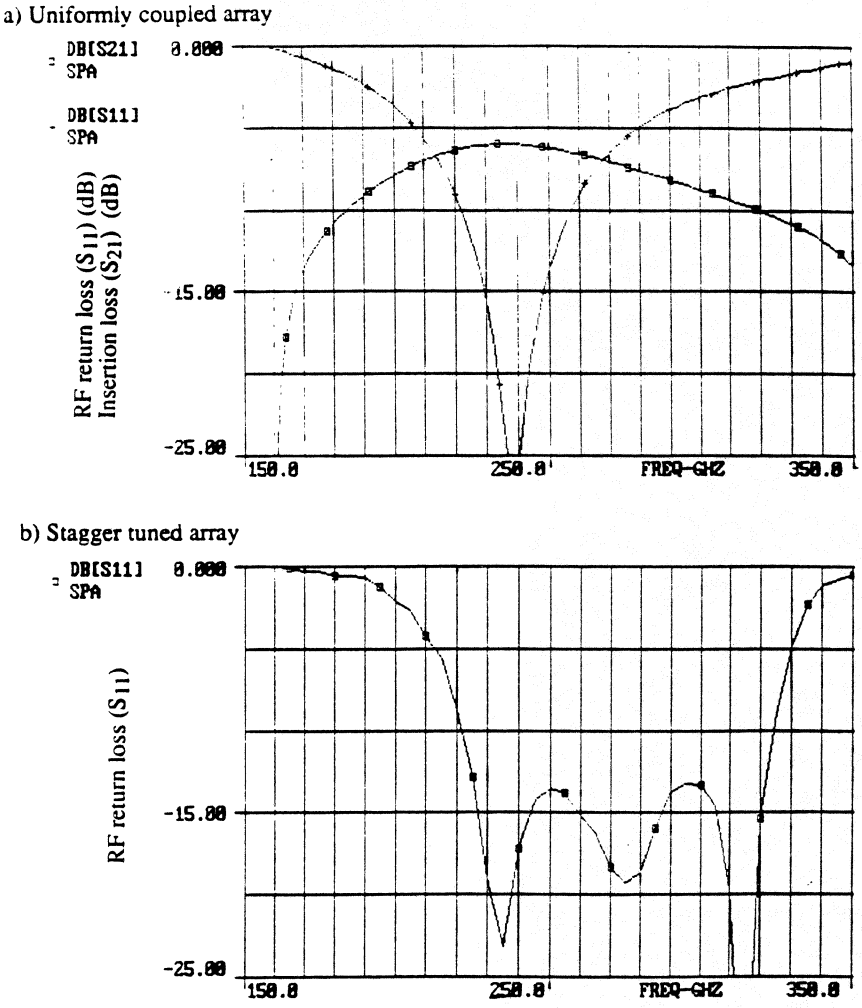
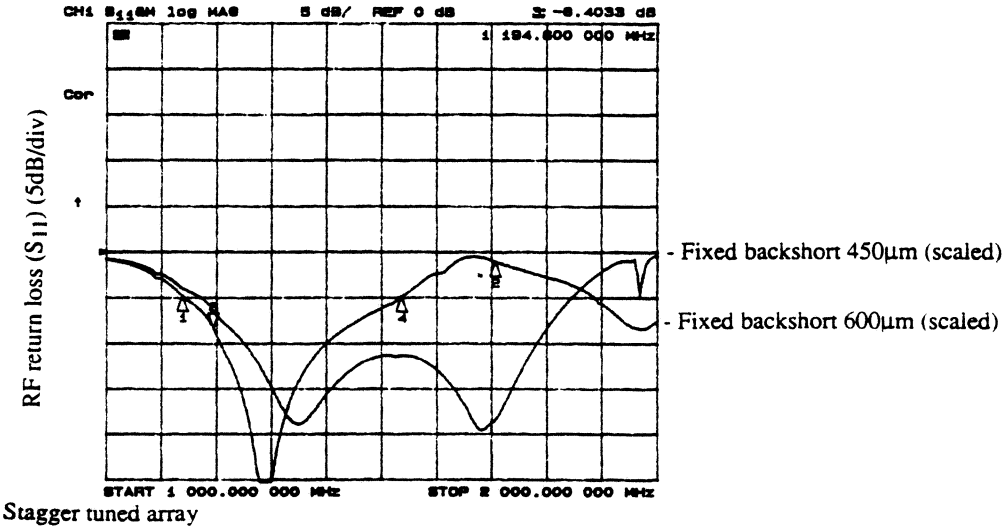


FIGURE 2. Series–Parallel array computer model predictions using lumped element circuit analysis and parallel resistors and capacitors to model the junctions. a) RF return loss and single junction insertion loss for a uniformly coupled array of 4 junctions. Each junction absorbs -6 dB of the input power at the design frequency, with 40 GHz bandwidth. The backshort is postioned 450μm from the array. b) RF return loss for a stagger tuned design, with 100 GHz bandwidth. The backshort is positioned 420μm from the array.

corrected empirically in the computer model. Figure 3 shows scale model results for uniformly coupled and stagger tuned arrays, with scaled bandwidths of 90 GHz and 50 GHz respectively, using a fixed backshort. Additional tuning flexibility is gained if the backshort is allowed to be adjusted. Structural complexities not modeled in the lumped circuit computer analysis caused the scale model resonances to differ somewhat from those predicted by Touchstone. In particular, the unexpectedly large bandwidth of the uniformly coupled array was surprising but encouraging. Despite these discrepencies the relatively simple computer models were a useful tool for predicting scale model performance. In the future we plan to simulate the device more accurately with a high frequency structure simulator.

a) Uniformly coupled array



b) Stagger tuned array

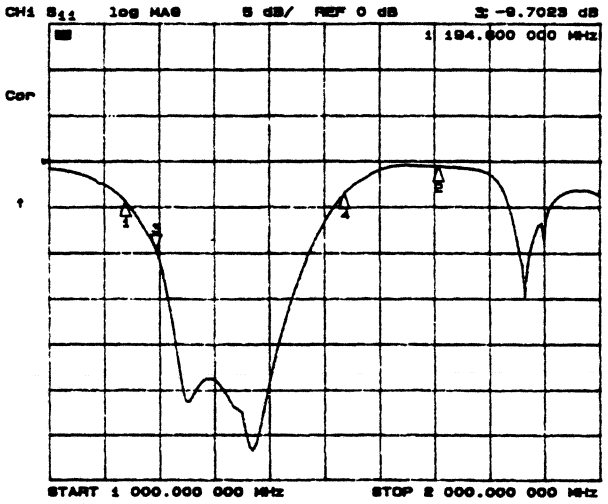


FIGURE 3. Series–Parallel array scale model measurements of RF return loss vs. frequency. Markers 1 and 2 represent scale frequencies of 200 and 300 GHz, respectively. a) Uniformly coupled array, with measurements for two backshort positions, $450\mu m$ and $600\mu m$ scaled. With backshort postion optimized the bandwidth is ~90 GHz. b) Stagger tuned array with backshort at $560\mu m$ scaled, and a bandwidth of ~50 GHz.

IV. Fabrication and Preliminary Test Results

The mixers were fabricated at the JPL Micodevices Laboratory using $Nb/AlO_x/Nb$ trilayer with critical current density $J_c \sim 10$ kA/cm^2. E-beam lithography was used to etch the $0.6\mu m \times 0.6\mu m$ junctions. The measured R_n is 16Ω for the array, near the designed value, with an ωRC product of 2.5. A photomicrograph of the uniformly coupled junction design is shown in Figure 4, with the SIS junction positions darkened for contrast.

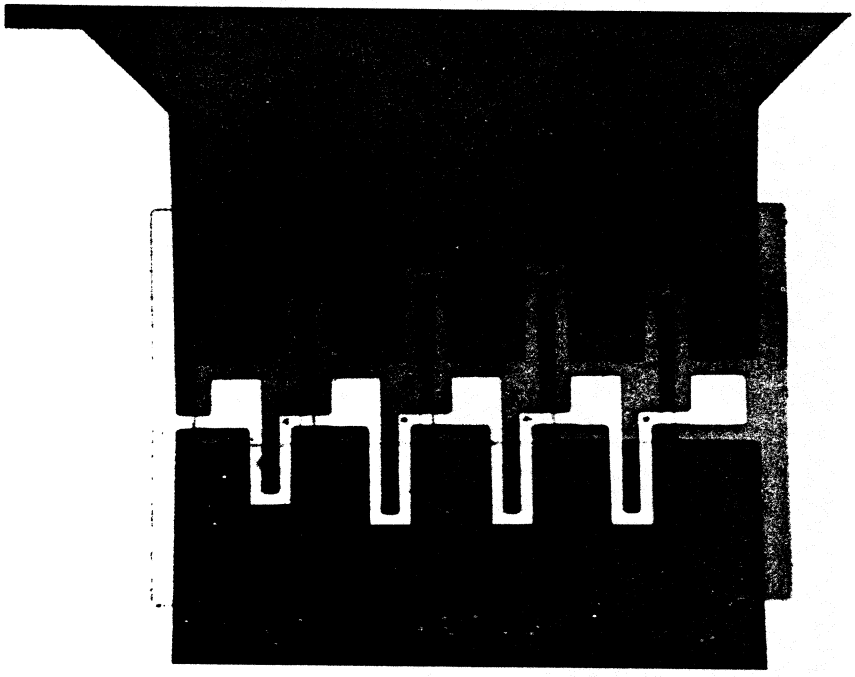


FIGURE 4. Photomicrograph of one of the uniformly coupled arrays. SIS junction locations are darkened for contrast. End inductors are shorter in order to couple RF power uniformly between junctions.

The outer inductors are shorter in order to couple RF power uniformly between the four junctions.

Before this conference there was only time to test one array from the first fabrication run. A full height waveguide for which the mixer was optimized was not available, and a reduced height waveguide was used instead. In initial tests of the uniformly coupled array a receiver noise temperature of 65 K was obtained at 210 GHz with a conversion loss of 4 dB calculated using the shot noise technique of Woody et al. (1985). As shown in the sample I-V curve in Figure 5, the junctions are well behaved thoughout the region of interest, with clearly defined LO steps and no apparent instabilities due to the Josephson effect.

In the test mixer block, a limited range of movement prevented the backshort from being placed at the optimal position 450μm from the array, as predicted by the scale model. Noise temperatures ranging from 65 to 140 K were obtained by tuning the backshort around the $3\lambda/4$ range at each frequency. With the backshort in a fixed position at $\sim 600\mu$m, we obtained receiver noise temperatures of 120 to 240 K throughout the range of the local oscillator, as seen in Figure 6.

These preliminary results are very encouraging, yielding respectable noise temperatures and demonstrating the broad bandwidth of the device. We are presently working on testing variations of the uniformly coupled and stagger tuned arrays in a full height waveguide mixer block. We expect that in proper testing conditions the noise temperatures demonstrated with the first array will be significantly reduced. We look forward to

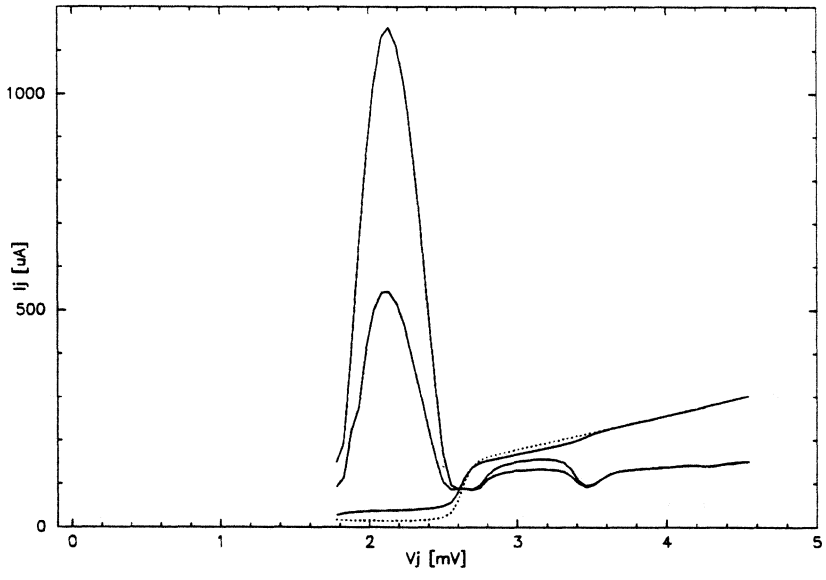


FIGURE 5. A sample I-V curve with LO off and with LO applied, and IF power with hot and cold loads. The junctions are well behaved thoughout the region of interest.

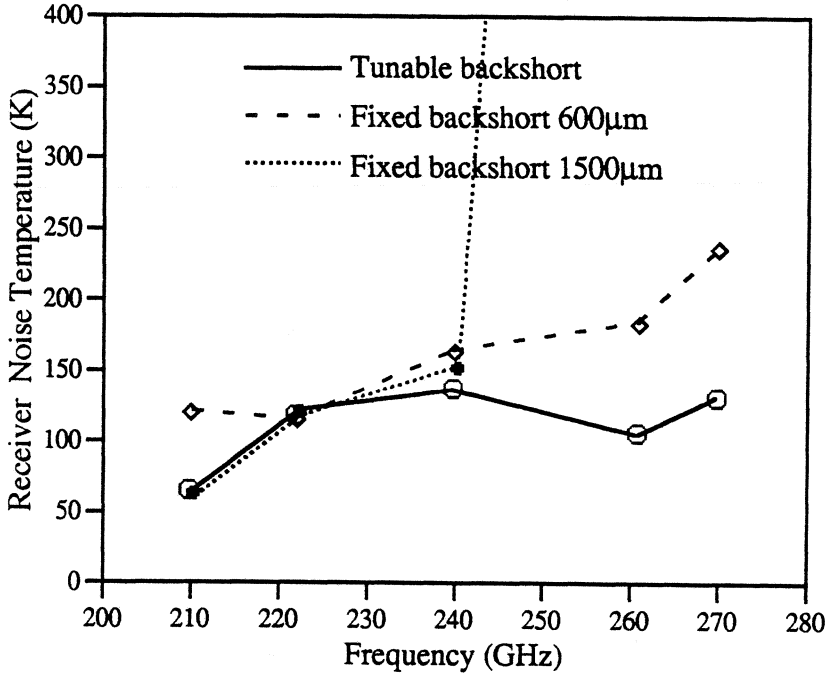


FIGURE 6. Preliminary measurements of receiver noise temperatures for the series–parallel array. The three lines represent noise temperatures using a tunable backshort, a fixed backshort at $\sim 600\mu$m and at $\sim 1500\mu$m. Tests were conducted using a reduced height waveguide mixer block. The array was optimized for a full height waveguide, but one was not available at the time the measurements were taken.

continued testing of the devices, and submillimeter devices in future iterations. We plan to implement successful devices at the Owens Valley Millimeter Array.

References

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