Circuit Design of the Loaded-Line Phase Shifter

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Abstract — **Circuit design procedures for the loaded-line phase shifter are presented, utilizing a phasor diagram representation of the line to identify its loading modes. The effects of losses in the loading elements on the circuit parameters are determined and design factors affecting bandwidth are discussed.**

I. Introduction

A PHASE-SHIFTING circuit is used in communications and antenna beam-directing circuits to introduce a change of phase in the transmitted signal. In the phase shifter types considered here, a discrete phase shift is produced by a change of the bias on semiconductor control devices in line-loading elements. Ideally, the insertion loss of the phase shifter should be small and equal in both of its phase states. The loaded-line phase shifter (Fig. 1) has advantages of simplicity and low insertion loss for phase shifts of less than 90°. The circuit consists of two equal two-state switchable admittances $Y_i = G_i + jB_i$ connected in shunt with a line section of characteristic impedance Z_c and electrical length θ, where $i = 1,2$ refers to the two bias states of the switching devices. The transition between the two admittance states produces a change $\Delta\phi$ in the phase of the transmission scattering coefficient S_{21}.

The circuit design problem of the loaded-line phase shifter consists of the selection of values for the six unknown parameters θ, Z_c, G_i, and B_i ($i = 1,2$). The conductance G_i results from ohmic losses in the loading elements Y_i and is typically small when low-loss switching devices are used. With low-loss loads, a good approximate solution is obtained by assuming that G_i is equal to zero. If the loaded electrical length θ is considered to be a free parameter, a large number of possible circuit designs exist [7], [10]. With the assumption of arbitrary θ, a frequent design approach has been to utilize computer-aided circuit analysis to generate a large array of circuit designs having input match and phase shift $\Delta\phi$, from which may be selected a suitable design showing wide bandwidth and low insertion loss [3]–[10]. In the present work, it is shown that the choice of loaded length θ is not arbitrary, but that its value depends upon the loading mode chosen, that is, the relative values of load admittances Y_1 and Y_2. A phasor representation of the phase shifter is utilized to demonstrate these relationships, and it is shown how the form of the conventional circuit design relations can be used to guide the selection of specific load-admittance configurations. The effect of losses in the loading elements upon the accuracy of the loss-free circuit design relations is also examined. The objective of the present work is, therefore, to furnish insight into the operation and design requirements of the loaded-line phase shifter and to point out some available options in the loading configurations used.

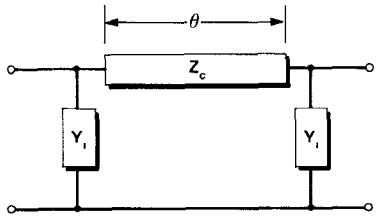

Fig. 1. Loaded-line phase shifter.

A derivation of the transmission characteristics of the input-matched phase shifter with lossless loading elements is given in Section II to establish the analytical approach being employed. The relations for the circuit parameters Z_c and B_i with θ specified are derived. The design based on the assumed losslessness of the phase shifter yields accurate computed values of the circuit parameters when high-Q devices such as silicon p-i-n diodes are used for switching. In cases where these devices are not available, as, for example, in GaAs integrated circuits where FET's in the passive switching mode may be used for switching, the loading losses may become significant, and it is important to confirm the extent to which the accuracy of the design relations is affected by nonnegligible values of normalized load conductance G_i/Y_0. In Section III, the effects of loading losses on the transmission factor S_{21} and the circuit-parameter relations is determined.

It is shown in Section II how the phasor diagram for the lossless phase shifter can be interpreted in terms of previously defined loading modes of the susceptances B_i. It is assumed that the concept of the defined loading modes can be carried over to a phase shifter having low to moderate losses, and options for the selection of load configurations are demonstrated.

II. The Lossless Loaded Section

The loaded-line phase shifter has conventionally been analyzed in terms of the model of its equivalent section of a uniform transmission line [2]–[4]. When losses are present, the equivalent line may have a complex characteristic

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impedance and propagation factor. To avoid the introduction of the extraneous concept and notation, the loaded-line phase shifter is here analyzed in terms of the elements of its 2×2 scattering matrix S_{ij}. The scattering matrix characterizes the input match, insertion loss, and phase shift of the two-port.

The scattering matrix is most readily obtained by transformation from the *ABCD* matrix of general circuit parameters. The *ABCD* matrix has been derived by several authors [2], [4], [5]. Its elements are

$$A_m = D_m = (\cos\theta - B_l Z_c \sin\theta) + jG_l Z_c \sin\theta \quad (1a)$$

$$B_m = jZ_c \sin\theta \quad (1b)$$

$$C_m = 2G_l(\cos\theta - B_l Z_c \sin\theta) + jZ_c\left[2B_l Y_c \cos\theta + \left(Y_c^2 + G_l^2 - B_l^2\right)\sin\theta\right] \quad (1c)$$

where subscripts m are used on the matrix elements. The transformation to the scattering matrix for a reciprocal, symmetrical two-port is given by

$$S_{11} = S_{22} = \frac{B_m Y_0 - C_m Z_0}{2A_m + B_m Y_0 + C_m Z_0} \quad (2)$$

$$S_{21} = S_{12} = \frac{2}{2A_m + B_m Y_0 + C_m Z_0} \quad (3)$$

where $Z_0 = 1/Y_0$ is the characteristic impedance of the circuit into which the phase shifter is connected.

The required phase shift $\Delta\phi$ corresponds to the change in the argument ϕ_i of $S_{21}(Y_i)$ when the load elements make the transition from Y_1 to Y_2, or, in the loss-free case, from jB_1 to jB_2. The specification of phase shift $\Delta\phi$ is not sufficient to determine the circuit parameters, and additional constraints are required. A constraint conventionally introduced is the requirement of input match. The elimination of reflected waves from the input to the phase shifter by input matching reduces the return loss and removes the occurrence of phase errors, which can be caused by interaction of the reflected waves with adjoining stages when phase bits are cascaded [2], [4]. Under the assumption of losslessness, the scattering matrix of the two-port is unitary, having the property $|S_{11}|^2 + |S_{12}|^2 = 1$. Thus, with the vanishing input reflection coefficient S_{11}, the transmission factor S_{21} of the phase shifter approaches unity.

The condition of the input match is specified by requiring $S_{11} = 0$ in (2). This leads to

$$B_m Y_0 = C_m Z_0. \quad (4)$$

When (4) is used in (3), the transmission matrix element S_{21} becomes

$$S_{21} = \frac{1}{A_m + B_m Y_0}. \quad (5)$$

With the assumption of losslessness, G_i is set equal to zero in (1a), which with, (5), becomes

$$S_{21} = \frac{1}{(\cos\theta - B_l Z_c \sin\theta) + jZ_c Y_0 \sin\theta}. \quad (6)$$

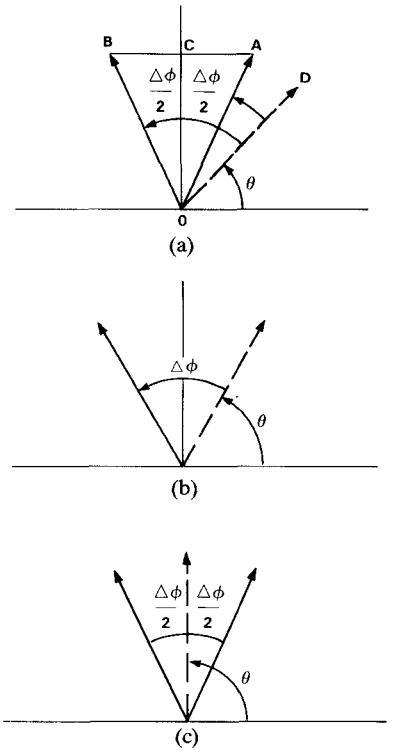

Fig. 2. Phasor diagrams for loaded-line phase shifters of electrical length θ. (a) Class I. (b) Class II (L/U). (c) Class III (CC).

In the input-matched loss-free case, the magnitude of S_{21} is unity. Therefore, in (6)

$$\cos\phi = \cos\theta - B_l Z_c \sin\theta \quad (7)$$

$$\sin\phi = -Z_c Y_0 \sin\theta \quad (8)$$

where ϕ is the phase angle of S_{21}. From (8), $\sin\phi$ remains constant during load switching, while $\cos\phi$, in (7), assumes two values with the two loading admittance states. The unit phasor S_{21}, which satisfies these conditions, is as shown in Fig. 2(a), in which OC is equal to $\sin\phi$ and CB and CA correspond to the two values of $\cos\phi$. The phase lag due to the geometrical length of the line is indicated in this figure by the dashed line OD at angle θ. Application of loading B_1 or B_2 rotates the phasor to OA or OB, respectively. The phase is thus switched symmetrically about 90° by increments of $\pm\Delta\phi/2$ by the line loading. Using $\phi = (90 \pm \Delta\phi/2)$ in (7) and (8) yields

$$Z_c = Z_0 \frac{\cos(\Delta\phi/2)}{\sin\theta} \quad (9)$$

$$\frac{B_i}{Y_0} = \frac{\cos\theta}{\cos(\Delta\phi/2)} \pm \tan(\Delta\phi/2) \qquad (i = 1,2). \quad (10)$$

Equations (9) and (10) are design relations for the lossless loaded-line phase shifter for phase shift $\Delta\phi$, with θ undetermined. These relations coincide with corresponding expressions derived from the equivalent transmission-line model [6], [8]. Under the present assumptions, the insertion loss is zero for all electrical lengths θ. From (7), we can infer that $d\phi/\text{dB}$ is positive for $\theta < 90°$. Therefore, the addition of capacitive susceptance loading increases the

phase angle ϕ, corresponding to counterclockwise rotation in Fig. 2.

A set of loading modes for the loaded-line phase shifter was defined by Opp and Hoffman [3]. Their condition for Class I loading corresponds to Fig. 2(a), in which the two values of B_i and the corresponding phase displacements are nonzero and unequal. Class II is the case in which one value of B_i is zero. When $B_1 = 0$, the phase of S_{21} is $\phi = \theta$, as in Fig. 2(b). Applying load B_2 then shifts the phase by $\Delta\phi$. This mode may be called load–unload (L/U) loading since the line load is conceptually applied to and removed from the line. With real semiconductor switching devices, line loading cannot be entirely removed, due to device capacitance in the switch OFF state. Compensation for device capacitance may be introduced, however, as shown in Section IV. Opp and Hoffman's Class III loading is that in which $B_1 = -B_2$. In the general case, the loading is switched between complex-conjugate (CC) values. With this condition in (10), the line length is necessarily $\theta = 90°$, and the loading switches the phase by $\pm\Delta\phi/2$ about this value, as in Fig. 2(c). In this complex-conjugate loading mode, a uniform output amplitude is maintained with phase shift when losses are present (cf. Fig. 3).

III. Effect of Losses in Line Loading

In the present work, all loaded-line phase shifter loss is assumed to be due to semiconductor loss in the loading admittances Y_i, appearing as a nonzero conductance component G_i. Transmission-line loss in the loaded section of length θ is neglected. With $G_i \neq 0$, the real and imaginary parts of (4) are

$$G_i(\cos\theta - B_i Z_c \sin\theta) = 0 \tag{11}$$

$$Y_0^2 \sin\theta = 2B_i Y_c \cos\theta + \left(Y_c^2 + G_i^2 - B_i^2\right)\sin\theta. \tag{12}$$

In the loss-free case ($G_i = 0$), (11) is automatically satisfied, but with $G_i \neq 0$, (11) can be satisfied for a single value of B_i only. As a result, input match is not maintained during phase switching with losses present. In the limit of small losses, the loss-free case is approached if (12) is satisfied. This is possible for two values of loading susceptance since (12) is quadratic in B_i. Therefore, (12) is assumed to hold, yielding the "quasi-input-matched" condition. With (12) in (3), the transmission factor (5) becomes

$$S_{21} = \frac{1}{(1+G_i Z_0)\left[(\cos\theta - B_i Z_c \sin\theta) + jZ_c Y_0 \sin\theta\right]}. \tag{13}$$

Equation (13) is similar to (6) except for the factor $(1+G_iZ_0)$ in the denominator. Again using (12), (13) may be rewritten

$$S_{21} = \frac{\cos\phi + j\sin\phi}{(1+G_i Z_0)\sqrt{1+G_i^2 Z_c^2 \sin^2\theta}} \tag{14}$$

where

$$\cos\phi = \frac{\cos\theta - B_i Z_c \sin\theta}{\sqrt{1+G_i^2 Z_c^2 \sin^2\theta}} \tag{15}$$

$$\sin\phi = -\frac{Z_c Y_0 \sin\theta}{\sqrt{1+G_i^2 Z_c^2 \sin^2\theta}}. \tag{16}$$

If it is assumed that the phasor S_{21} is caused to switch by equal increments $\Delta\phi/2$ about 90° by the load switching, as in the loss-free case, then (14)–(16) lead to

$$Z_c = Z_0 \frac{\cos\frac{\Delta\phi}{2}}{\sin\theta}\left(1 - G_i^2 Z_0^2 \cos^2\frac{\Delta\phi}{2}\right)^{-1/2} \tag{17}$$

$$\frac{B_i}{Y_0} = \frac{\cos\theta}{\cos\frac{\Delta\phi}{2}}\left(1 - G_i^2 Z_0^2 \cos^2\frac{\Delta\phi}{2}\right)^{1/2} \pm \tan\frac{\Delta\phi}{2}. \tag{18}$$

The squared terms in the normalized conductance G_iZ_0 in (17) and (18) represent the corrections to the loss-free parameter expressions (9) and (10) when losses are present. For small normalized conductance ($G_iZ_0 \leqslant 1$), these corrections may be negligibly small, as shown below. Equation (18) preserves a useful property of the corresponding loss-free expression (10). Calculation of the change in normalized load susceptance with either expression yields

$$(B_1 - B_2)/Y_0 = 2\tan(\Delta\phi/2).$$

For a sufficiently small phase shift, i.e., when $\tan(\Delta\phi/2) \simeq \Delta\phi/2$, ($\Delta\phi$ radians), the phase shift in radians is approximately equal to the change in normalized susceptance with load switching [2]. The form of (17) and (18) shows that these approximate expressions are valid only within the loss limit: $G_iZ_0\cos\Delta\phi/2 \leqslant 1$.

The form of (17) and (18) is not convenient for calculation in the general case since G_i/Y_0 is not independent of B_i/Y_0. The conductance normally increases with increasing B_i/Y_0. If a loading Q is defined

$$Q_L \equiv \frac{|B_i|}{G_i} \tag{19}$$

then (18) may be converted to the form

$$\frac{B_i}{Y_0} = \frac{\cos\theta}{\cos\frac{\Delta\phi}{2}}\left[\frac{1}{m} + \frac{\sin^2\frac{\Delta\phi}{2}}{\cos^2\theta}\left(\frac{1}{m^2} - \frac{1}{m}\right)\right]^{1/2} \pm \frac{1}{m}\tan\frac{\Delta\phi}{2} \tag{20}$$

where $m \equiv 1 + (\cos\theta/Q_L)^2$. With low to moderate losses, i.e., when Q_L is large, loading admittances calculated from the loss-free expression (10) differ negligibly from the result of (20). For example, with $Q_L = 10$, $\theta = 60°$, and $\Delta\phi = 45°$, (10) and (20) disagree by less than 0.3 percent.

Using the definition of loading Q_L ((19)) the insertion loss of the loaded-line phase shifter may be calculated from (14)

$$\mathrm{IL} = -20\left[\log(1 + B_i Z_0/Q_L) + \tfrac{1}{2}\log\left\{1 + (B_i Z_c \sin\theta/Q_L)^2\right\}\right]. \tag{22}$$

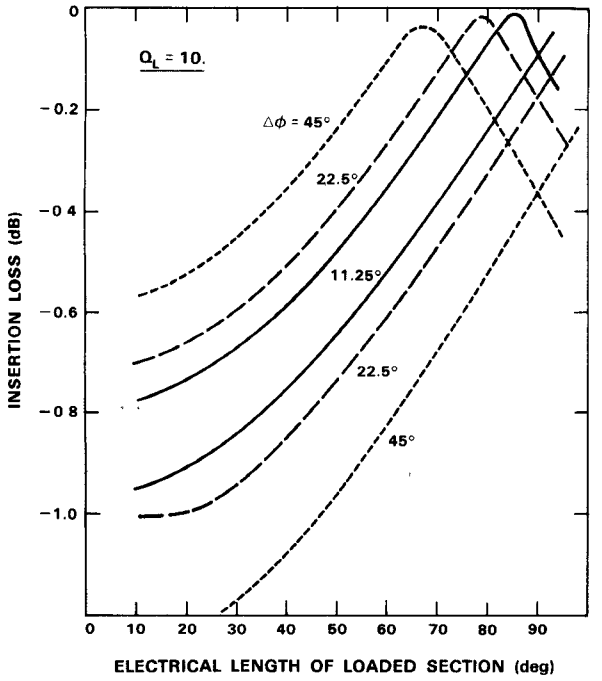

Fig. 3. Insertion loss versus loaded-line length of phase shifters with loading $Q_L = 10$, for phase shifts $\Delta\phi$ of 11.25°, 22.5°, and 45°.

Insertion loss as a function of loaded length θ is shown plotted in Fig. 3 for loading $Q_L = 10$, and typical phase shifts. A simpler calculation for insertion loss may be obtained by use of (9) and (10) instead of (17) and (18) in (22). The approximate result differs by less than 1 percent from the exact value when $Q_L > 10$.

Two insertion-loss curves appear in Fig. 3 for each value of phase shift $\Delta\phi$, corresponding to the fluctuation in insertion loss as the line-load state is switched. In this figure, the mean magnitude of insertion loss for each $\Delta\phi$ decreases monotonically with θ toward a minimum value at $\theta = 90°$. At $\theta = 90°$, the two insertion-loss curves for a given phase shift intersect, demonstrating that in the loaded-line phase shifter with losses, constancy of output amplitude with phase shift can be obtained only by use of an electrical length θ of 90 electrical degrees.

IV. Switched-Load Circuit Designs

The line-loading susceptances required for the phase shifter are specified by (18) or (10). The principles involved in load-element construction are sufficiently illustrated by the lossless-load case, for which (10) is applicable, rewritten below:

$$B_1 = Y_0\left(\frac{\cos\theta}{\cos(\Delta\phi/2)} - \tan(\Delta\phi/2)\right) \tag{23a}$$

$$B_2 = Y_0\left(\frac{\cos\theta}{\cos(\Delta\phi/2)} + \tan(\Delta\phi/2)\right). \tag{23b}$$

In the construction of the two-state load susceptances (23a,b) with the use of semiconductor switching devices, one of two types of circuit model may be adopted. In the first model, the semiconductor devices are considered to be nearly ideal switches, which are used to select load B_1 or B_2 alternately. In the second model, a lossless impedance transformer is used to convert the two bias-state terminal impedances of the semiconductor devices into the values required by (23a,b). These two models are illustrated schematically in Fig. 4. In Fig. 4(a), the diode switch connects the stub loads, as, for example, in Class II (L/U) loading. In Fig. 4(b), the transmission-line impedance-transformer converts the two-state terminal admittances of the diode to the required loading susceptances. The first model, with the diodes regarded as nearly ideal switches, is considered initially here.

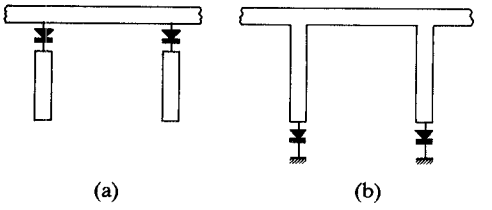

Fig. 4. Line-loading concepts. (a) Diode-switched stub loads. (b) Line-transformed diode impedances.

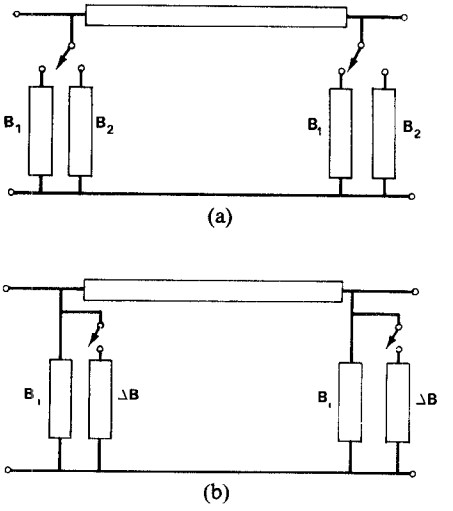

Fig. 5. Load switching schemes. (a) SPDT switching. (b) SPST switching.

In principle, the phase shift could be accomplished by use of a single-pole double-throw (SPDT) switch which selects alternately the separate load susceptances B_1 and B_2 of (23a,b), as in Fig. 5(a). We note, however, that these expressions may be reformulated as

$$B_1 = Y_0\left(\frac{\cos\theta}{\cos(\Delta\phi/2)} - \tan(\Delta\phi/2)\right) \tag{24}$$

$$\Delta B = 2Y_0\tan(\Delta\phi/2). \tag{25}$$

In this formulation, the line loading may be considered to be composed of a constant component B_1 (24), which is permanently connected to the line, and an incremental component ΔB, which is connected in shunt with B_1 by means of a single-pole single-throw (SPST) switch, as in Fig. 5(b). Alternatively, of course, B_2 may be taken as the fixed load, with a switched component $\Delta B = -2Y_0\tan(\Delta\phi/2)$ added in shunt to yield B_1. The SPST

TABLE I
LOAD SUSCEPTANCES OF THE LOADED-LINE PHASE SHIFTER, NORMALIZED TO SYSTEM CHARACTERISTIC ADMITTANCE Y_0.

$\Delta\phi$ =	5.63		11.25		22.5		45	
θ	B_1'	B_2'	B_1'	B_2'	B_1'	B_2'	B_1'	B_2'
30	.818	.916	.772	.969	.684	1.082	.523	1.352
35	.771	.869	.725	.922	.636	1.034	.472	1.301
40	.718	.816	.671	.868	.582	.980	.415	1.243
45	.659	.757	.612	.809	.522	.920	.351	1.180
50	.594	.693	.547	.744	.456	.854	.282	1.110
55	.525	.623	.478	.675	.386	.784	.207	1.035
60	.451	.550	.404	.601	.311	.709	.127	.955
65	.374	.472	.326	.523	.232	.630	.043	.872
67.5*	.334	.432	.286	.483	.191	.589	-.000	.828
70	.293	.392	.245	.442	.150	.548	-.044	.784
75	.210	.308	.162	.359	.065	.463	-.134	.694
78.75*	.146	.244	.098	.295	-.000	.398	-.203	.625
80	.125	.223	.076	.273	-.022	.376	-.226	.602
84.38*	.049	.147	-.000	.197	-.099	.299	-.308	.520
85	.038	.136	-.011	.186	-.110	.288	-.320	.509
87.19*	-.000	.098	-.049	.148	-.149	.249	-.361	.467
90**	-.049	-.049	-.098	.098	-.199	.199	-.414	.414
95	-.136	-.038	-.186	-.011	-.288	.110	-.509	.320
100	-.223	-.125	-.273	-.076	-.376	-.022	-.602	.226
105	-.308	-.210	-.359	-.162	-.463	-.065	-.694	.134
110	.392	.293	.442	.245	.548	.150	.784	.044

*CLASS II (L/U) PHASE SHIFTER FOR $\Delta\phi = 2(90-\theta)$

**CLASS III (C/C) PHASE SHIFTER

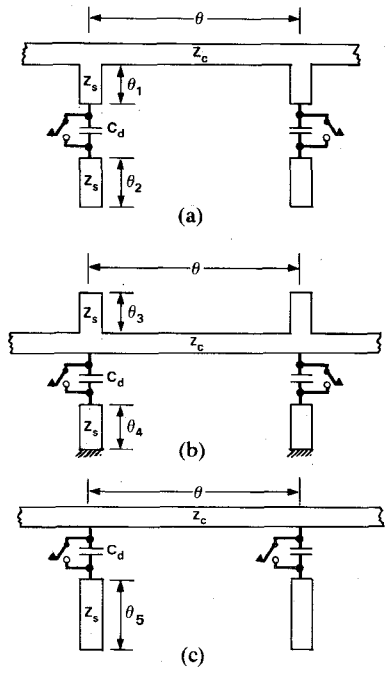

Fig. 6. Stub-loading circuits for lossless switches with capacitance C_d. (a) Tandem stubs. (b) Shunt stubs. (c) Load-unload (L/U) connection.

switch may be constructed with a single semiconductor device as compared with the two devices normally required for a SPDT switch, and since SPST switches require less circuit area in planar circuits, this circuit form may be preferable for economy of circuit area. The two switching schemes do not lead, in general, to electrically identical loads; however, if the sign of ΔB is different from that of the fixed load B_i, the frequency dependence of $B_i + \Delta B$ may lead to a different bandwidth from that with single-element loads B_1 and B_2, as shown in Section V below.

The load susceptances B_1 and B_2, or B_i and ΔB, may be supplied as lump capacitors or inductors if available. Distributed elements, composed of open- or short-circuit terminated stubs, may also be used. Stubs composed of the transmission-line medium are convenient to produce in an environment such as integrated microstrip circuitry, and will be treated in the following. A survey of the normalized loading susceptance requirements specified by (23a, b) for loaded-line phase shifters having selected values of length θ and phase shift $\Delta\phi$ is shown in Table I. The table shows how the sign and magnitude of the required loads depend upon the choice of loaded length θ for a given phase shift. As noted above, the sign of the switched component ΔB may be selected arbitrarily for given θ, depending on the choice of B_1 or B_2 as a fixed component of the load. The latter choice may be made on the basis of the bias supply for the switching devices, or upon frequency characteristics of the two cases. If ΔB is chosen negative and is provided by means of a shorted stub of less than 90° having a metallic-ground termination, as with a via hole in microstrip, a ground return path is thus provided for the SPST switch.

It may also be seen in Table I that, for the type of phase shifter being considered here (input-matched, with symmetrical phase switching about 90°), the smallest average absolute values of load susceptances B_1 and B_2 are required for load intervals θ in the neighborhood of 90°. For lengths less than 90° and small phase shifts $\Delta\phi$, both susceptance states B_1 and B_2 are positive (capacitive). For phase shifts of 45° and loaded lengths from 70° to 90°, the line loads must change sign upon phase shift. These characteristics determine the form of the load elements which must be designed for a given application. It is further seen in Table I that the choice of shorter length θ calls for larger load susceptances B_1 and B_2, requiring longer stubs when capacitive stub loads are used. If a minimum planar circuit area is required, a suitable compromise between loaded-line length and stub length must be reached. As has been shown, the length θ is arbitrary only with Class I loading. By combining the loading requirements for the wanted phase shift with the practical constraints of the circuit type being used, guidance is available in the choice of θ and the loading element design. Because of the potentially wide range of possible loading-circuit designs, a limited number of cases is presented here to illustrate typical procedures.

Fig. 6 shows representative stub-loading circuits which provide two loading states to the phase shifter using SPST switches. In this figure, the switching devices are represented as ideal switches shunted by capacitance C_d. In Fig. 6(a), with tandem stub lengths, both loading susceptance states are nonzero and positive, as is required by over 80 percent of the cases shown in Table I. In Fig. 6(a), the increment ΔB of (25) is positive.

If the switch capacitance is negligible ($C_d = 0$), the electrical lengths of the stub sections in the phase shifter with tandem stubs in Fig. 6(a) are

$$\theta_1 = \tan^{-1}(B_1/Y_s) \tag{26a}$$

$$\theta_2 = \tan^{-1}(B_2/Y_s) - \theta_1 \qquad (C_d = 0) \tag{26b}$$

where B_1 and B_2 are the required loading susceptances

given by (23a, b) and $Y_s = 1/Z_s$ is the characteristic admittance of the stub line. Neglect of the switch capacitance of typical semiconductor switching devices may lead to phase errors in the loaded-line phase shifter. Errors may be large for small phase shifts $\Delta\phi$ when loading-stub susceptances are comparable with the open-switch susceptance. For example, in the circuit of Fig. 6(a), the use of the uncorrected relations (26a, b) for the design of phase shifters at 10 GHz, with switches having capacitance $C_d = 0.03$ pf, leads to a phase-shift error of 11.4 percent in a $\Delta\phi = 45°$ phase shifter, and of 34.3 percent in a $\Delta\phi = 11.25°$ phase shifter. Capacitance-corrected stub lengths θ_1 and θ_2 for the phase shifter of Fig. 6(a) are given in Appendix I.

The shunt-stub circuit of Fig. 6(b) is of interest in that it may be operated in the Class I, Class II, or Class III loading mode by appropriate selection of circuit parameters. To show this, the following notation is defined:

$$K \equiv Y_0 \cos\theta / \cos(\Delta\phi/2) \tag{27}$$

$$T \equiv Y_0 \tan(\Delta\phi/2). \tag{28}$$

In Fig. 6(b) with switches closed, we have

$$B_1 = B_3 + B_4 = K - T. \tag{29}$$

With switches open, the loading is

$$B_2 = B_3 + \frac{B_4 B_c}{B_4 + B_c} = K + T \tag{30}$$

where B_3 and B_4 are the susceptances of the stubs of length θ_3 and θ_4, respectively, $B_c = C\omega$ is the susceptance of the open-switch capacitance, and B_1 and B_2 are as given by (23a, b). In Class I loading, where θ is specified, K is known. The stub lengths for Class I loading in Fig. 6(b) are then given by

Class I:

$$\theta_3 = \tan^{-1} Z_s\left(K + T\sqrt{1 - 2C_d\omega/T}\right) \tag{31}$$

$$\theta_4 = \cot^{-1}\left[Z_s T\left(1 + \sqrt{1 - 2C_d\omega/T}\right)\right] \tag{32}$$

where Z_s is the characteristic impedance of the stub line.

In Class II loading, the unloaded state may be obtained by parallel-resonating the stubs, in which case $\tan\theta_3 = \cot\theta_4$. This leads to

Class II:

$$\theta_3 = \tan^{-1} Z_s T\left(1 + \sqrt{1 - 2C_d\omega/T}\right) \tag{33}$$

$$\theta_4 = (90 - \theta_3)°. \tag{33a}$$

For the Class III loading case, $B_2 = -B_1 = T$, from which the stub lengths in Fig. 6(b) are

Class III:

$$\theta_3 = \tan^{-1}\left(Z_s T\sqrt{1 - 2C_d\omega/T}\right) \tag{34}$$

$$\theta_4 = \cot^{-1}\left[Z_s T\left(1 + \sqrt{1 - 2C_d\omega/T}\right)\right]. \tag{35}$$

If the switch capacitance C_d were zero in the single-stub loading circuit shown in Fig. 6(c), this would represent a Class II loading example. In Class II loading, two cases are possible, depending upon the sign of the loading susceptance. For positive loading, with open stubs as in Fig. 6(c)

$$\theta = (90 - (\Delta\phi/2))° \tag{36a}$$

$$\theta_5 = \tan^{-1} 2TZ_s \qquad (C_d = 0;\ \text{OC stubs}). \tag{36b}$$

With shorted-stub loading (negative ΔB), the stub load reduces the phase length of the loaded line; thus, we use

$$\theta = (90 + (\Delta\phi/2))° \tag{37a}$$

$$\theta_s = \cot^{-1} 2TZ_s \qquad (C_d = 0;\ \text{SC stubs}). \tag{37b}$$

With switching device capacitance C_d nonzero, however, the loading mode is Class I, and with open-ended stubs, as in Fig. 6(c), the circuit parameters are

$$\theta = \cos^{-1}\left[\sin(\Delta\phi/2)\sqrt{1 + 2(C_d\omega/Y_0)\cot(\Delta\phi/2)}\right] \tag{38a}$$

and the corresponding open-ended stub length θ_5 is given by

$$\tan\theta_5 = \frac{Y_0}{Y_s}\tan\frac{\Delta\phi}{2}\left[1 + \sqrt{1 + 2(C_d\omega/Y_0)\cot\frac{\Delta\phi}{2}}\right]. \tag{38b}$$

The characteristic impedance Z_c of the loaded section is then given by the use of (38a) and (9).

Class III — Complex-Conjugate (CC) Loading: In CC load switching, the two load admittance states are $G_1 + jB_1 = G_2 - jB_2$. In the low-loss case, $B_1 = -B_2 = \pm Y_0 \tan(\Delta\phi/2)$. In microstrip, if connections to the ground plane are available, the inductive susceptance can be obtained by a short-terminated stub. Numerous alternative circuits for complex-conjugate load pairs are possible. Fig. 7 summarizes stub circuits which may be used to produce complex-conjugate susceptance pairs. In this figure, ideal switches with zero capacitance are assumed. To illustrate the application of these circuits, consider Fig. 7(d). For the input susceptance with the switch open, we have

$$B_1 = Y_s \tan\theta_1 \tag{39a}$$

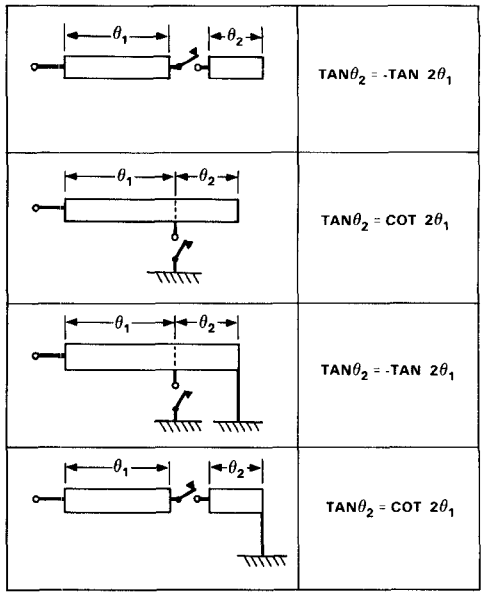

Fig. 7. Circuits for complex-conjugate susceptance switching.

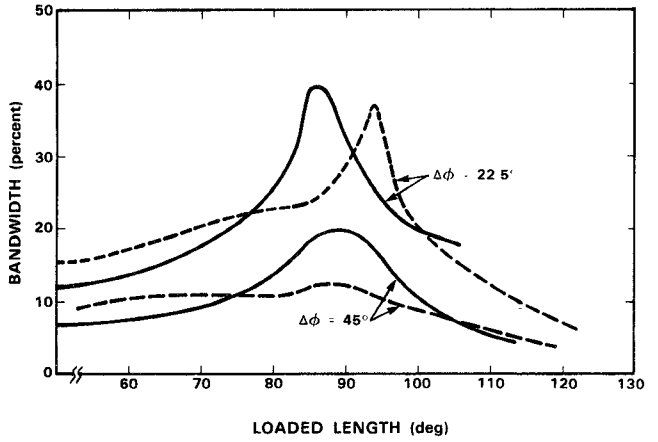

Fig. 8. Bandwidth of lumped-load Class I phase shifters. Solid-line: double-throw switching; broken line: single-throw switching.

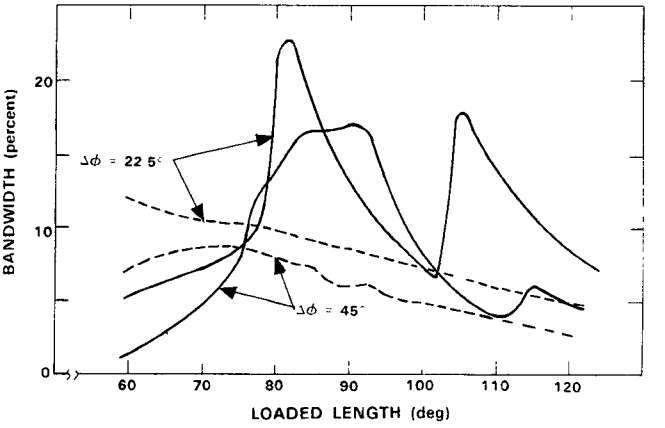

Fig. 9. Bandwidth of stub-loaded Class I phase shifters. Solid line: double-throw switching; broken line: single-throw switching.

where Y_s is the susceptance of the stub line. In the second bias state with the switch closed

$$B_2 = -Y_s \cot(\theta_1 + \theta_2). \tag{39b}$$

From (23a, b) with complex-conjugate loading, $\theta = 90°$. Therefore

$$B_1 = -B_2 = Y_0 \tan\frac{\Delta\phi}{2}. \tag{39c}$$

If a stub susceptance Y_s is assumed, (39) determines the remaining stub parameters θ_1 and θ_2. With the switching devices having nonzero capacitance, compensation for switch reactances may be introduced, as was done above for the Class I and Class II phase shifter [10].

When lossy switching devices are used, in order to attain constancy of insertion loss with phase shift in complex-conjugate load switching, the stub circuit must act as a two-state impedance transformer, which transforms the two bias-induced impedance states of the devices into a complex-conjugate pair, in which the susceptance has the magnitude given by (10) or (18) for the given phase shift. Such two-state impedance transformers can be devised, as shown in Appendix II.

V. Bandwidth and Applications

The loaded-line phase-shifter circuits discussed above are single-frequency designs valid over a limited range about the design frequency. A usual definition of bandwidth for this phase shifter corresponds to the frequency range over which the phase shift remains within $\pm 2°$ of the design value and the input VSWR is 1.2 or less in both phase states. The bandwidth depends upon the type of loading used (lumped or distributed), and the form of load switching (SPST or SPDT). Fig. 8 shows the bandwidths of Class I phase shifters with lumped inductor or capacitor loads as a function of loaded electrical length θ for phase shifts of 22.5° and 45°. These bandwidths peak generally for θ between 85° and 95° and decrease rapidly with increasing phase shift. At a 45° phase shift, peak bandwidths are larger with double-throw switching (Fig. 8, solid line) than with single-throw switching (broken line). When distributed (stub) loads are used, the maximum bandwidths of Class I phase shifters are greater when double-throw switching is used (Fig. 9). These differences are of course due to the differences in the dispersive character of B_1, B_2 loads ((23)) and B_i, $(B_i + \Delta B)$ loads, ((24)), and depend also upon the sign chosen for ΔB in the SPST case. In the stub-loading calculations shown in Fig. 9, ΔB was chosen negative. In this figure, all stub load susceptances were obtained with stub electrical lengths of less than 90°, i.e., shorted stubs for negative susceptances, and open stubs for positive susceptances. In these calculations, ideal switches with zero capacitance were assumed.

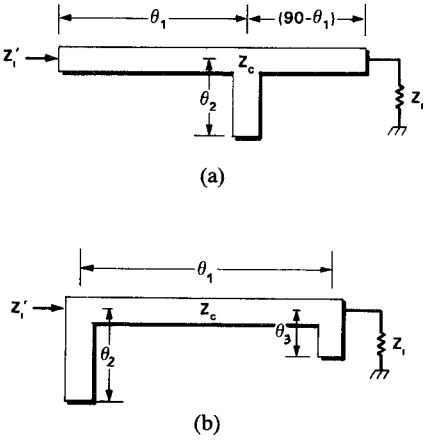

Fig. 10. Impedance transformers. (a) Single stub. (b) Double stub.

To test the circuit design techniques given above, SPST-switched 22.5° phase shifters were built in microstrip on a 0.125-in (3.18-mm) polyolefin substrate for 0.75 GHz using the circuit of Fig. 6(b), with Class I, II, and III loadings. Packaged p-i-n diodes with effective capacitances of 0.23 pf were used for switching. The circuit parameters calculated from (31)–(35), with stub characteristic impedances taken to be 93 Ω, were

Class	θ	Z_c	θ_3	θ_4
I	85°	49	28°	54°
II	78.8°	50	36°	54°
III	90°	49	20°	54°

In addition to the SPST-switched phase shifters above, a 22.5° Class I SPDT phase shifter was constructed on polyguide substrate for 0.75 GHz, with a loaded length θ of 82.5°. This phase shifter had for its loading elements an open stub of length 18.4° for load B_2, and a shorted stub of length 86.2° for load B_1. These were SPDT-switched with series-connected diode switches as in Fig. 5(a). The measured bandwidths of the SPST phase shifters were found to be 8, 10, and 10.5 percent for the Class I, II, and III phase shifters, respectively, compared with calculated bandwidths of 11.3, 12.3, and 13.3 percent, respectively. (These magnitudes are not in agreement with Fig. 9, since a switch capacitance of 0.23 pf was employed for these calculations, whereas Fig. 9 assumes zero switch capacitance.) The discrepancies in the measured bandwidth values are assumed to be due to parasitics at the transition to microstrip, and to diode-lead parasitics. The SPDT phase shifter had a measured bandwidth of 20 percent, in good agreement with a calculated bandwidth of 22 percent. This result confirms the broader bandwidth of SPDT-switched loads, which is implied by the curves of Fig. 9.

VII. Conclusion

In the design of the loaded-line phase shifter for phase shift $\Delta\phi$, the value employed for electrical length θ of the loaded section is subject to constraints depending on the two-state line-loading sequence adopted. When complex-conjugate loading is used ($B_1 = -B_2$), then $\theta = 90°$. With "load/unload" loading ($B_1 = 0 \neq B_2$), the line length is $\theta = (90 - \Delta\phi/2)°$. For the general loading case ($0 \neq |B_1| \neq |B_2| \neq 0$), the value of θ is not *a priori* restricted if it does not lead to an invalid requirement on the characteristic impedance Z_c of the loaded section. In all cases, the value of Z_c is chosen to provide input match in the loss-free model, or the closest approach to input match, when loading losses are present. In the latter case, the mean insertion loss of the phase shifter in its two phase states is least with $\theta = 90°$. With typical stub loadings, the phase-shift bandwidth is greatest with $\theta \cong 80°$.

Appendix I
Solution for Tandem-Connected Stub Lengths

In Fig. 6(a) with tandem stubs, the load susceptance of the stub circuit in the switch OFF state is

$$B_1 = \frac{C_d\omega(\tan\theta_1 + \tan\theta_2) + Y_s \tan\theta_1 \tan\theta_2}{C_d\omega(1 - \tan\theta_1 \tan\theta_2) + Y_s \tan\theta_2} Y_s \quad \text{(A1)}$$

where Y_s is the characteristic admittance of the transmission line used in the stubs. In the ON state of the lossless switch

$$B_2 = Y_s \tan(\theta_1 + \theta_2). \quad \text{(A2)}$$

The stub lengths θ_1 and θ_2 of the tandem-connected stubs in Fig. 6(a) are obtained by solution of (A1) and (A2), using B_1 and B_2 from (23) and (24), repeated below. By the use of trigonometric identities, (A1) and (A2) may be combined to yield the second-degree equation in $\tan\theta_1$

$$M\tan^2\theta_1 - 2N\tan\theta_1 = P$$

for which the solution is

$$\tan\theta_1 = \frac{N}{M}\left(1 + \sqrt{1 + MP/N^2}\right) \quad \text{(A3)}$$

where

$$M = 1 - C_d\omega(B_2 - B_1)/Y_s^2$$
$$N = (B_1 + B_2)/2Y_s$$
$$P = \left[(B_2 - B_1)C_d\omega - B_1B_2\right]/Y_s^2.$$

Then, from (A2)

$$\theta_2 = \tan^{-1}(B_2/Y_s) - \theta_1 \quad \text{(A4)}$$

where B_1 and B_2 are as given in (23) and (24)

$$B_1 = Y_0(\cos\theta/\cos(\Delta\phi/2) - \tan(\Delta\phi/2))$$
$$B_2 = Y_0(\cos\theta/\cos(\Delta\phi/2) + \tan(\Delta\phi/2)).$$

Appendix II
Two-State Impedance Transformers

If a two-terminal impedance having the two bias-switched impedance states Z_1 and Z_2 is transformed by a lossless two-port to transformed values Z_1' and Z_2', the initial and transformed impedances must satisfy the relation [11]

$$\hat{Q}^2 = \frac{(R_1 - R_2)^2 + (X_1 - X_2)^2}{R_1R_2} = \frac{(R_1' - R_2')^2 + (X_1' - X_2')^2}{R_1'R_2'} \quad \text{(A5)}$$

where $Z_i = R_i + jX_i$ and $Z_i' = R_i' + iX_i'$, $(i = 1,2)$. In (A5), $\hat{Q}$ is a characteristic constant of the impedance pair which is invariant to lossless transformation.

The impedance transformation by a two-port is given by

$$R' + jX' = \frac{A_m(R + jX) + B_m}{C_m(R + jX) + D_m} \quad \text{(A6)}$$

where A_m, B_m, C_m, and D_m are the elements of the $ABCD$ matrix of the two-port. For a lossless impedance transformer, this matrix has the form

$$M = \begin{pmatrix} a & jb \\ jc & d \end{pmatrix} \quad \text{(A7)}$$

where a, b, c, and d are real. For a reciprocal two-port, these elements satisfy

$$ad + bc = 1. \quad \text{(A8)}$$

Equation (A6) may then be written

$$R_j' + jX_i' = \frac{\alpha(R_i + jX_i) + j\beta}{j\gamma(R_i + jX_i) + 1} \quad (i = 1,2) \quad \text{(A9)}$$

where we have defined $\alpha = a/d$, $\beta = b/d$, $\gamma = c/d$. When

written for $i=1$ and $i=2$, (A9) may be solved to yield

$$\gamma = \frac{\left(R_1'R_2 - R_2'R_1\right)}{R_2\left(R_1'X_1 + X_1'R_1\right) - R_1\left(R_2'X_2 + X_2'R_2\right)} \quad \text{(A10)}$$

$$\alpha = \frac{R_1' - \gamma\left(R_1'X_1 + X_1'R_1\right)}{R_1} \quad \text{(A11)}$$

$$\beta = X_1' + \gamma\left(R_1R_1' - X_1X_1'\right) - \alpha X_1. \quad \text{(A12)}$$

Then, from (A8)

$$d = \frac{1}{\sqrt{\alpha + \beta\gamma}}. \quad \text{(A13)}$$

It must be observed that this transformation is valid only when (A5) is satisfied.

Finally, $a = d\alpha$, $b = d\beta$, and $c = d\gamma$.

With a, b, c, and d known, a lossless two-port must be constructed which embodies this transformation matrix. As a working rule, at least three free circuit parameters are required in the two-port, since there are essentially three characteristic constants in the transformation ((A9)). A useful transformer is one consisting of a quarter wavelength line with a shunt stub of variable magnitude and position (Fig. 10(a)). If both line and stub have the same characteristic impedance Z_c, the circuit parameters are

$$Z_c = \frac{1 \pm \sqrt{1 - bc}}{c} \quad \text{(A14)}$$

$$\sin\theta_1 = \sqrt{\frac{a}{a+d}} \quad \text{(A15)}$$

$$\tan\theta_2 = -(a+d). \quad \text{(A16)}$$

An alternative circuit which may be used as a two-state impedance transformer is the double-stub circuit (shown in Fig. 10(b)). A relatively simple calculation for its circuit parameters may be made by starting with suitable trial values of $Z_c \geq b$ in the relations

$$\sin\theta_1 = \frac{b}{Z_c} \quad \text{(A17)}$$

$$\tan\theta_2 = Z_c\frac{\cos\theta_1 - d}{b} \quad \text{(A18)}$$

$$\tan\theta_3 = Z_c\frac{\cos\theta_1 - a}{b}. \quad \text{(A19)}$$

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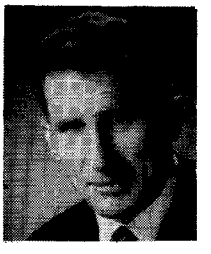

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