

# Dynamic Charge Restoration of Floating Gate Subthreshold MOS Translinear Circuits

Vincent F. Koosh  
California Institute of Technology  
Pasadena, CA 91125  
darkd@micro.caltech.edu  
<http://www.micro.caltech.edu>

Rodney Goodman  
California Institute of Technology  
Pasadena, CA 91125  
rogo@micro.caltech.edu  
<http://www.micro.caltech.edu>

## Abstract

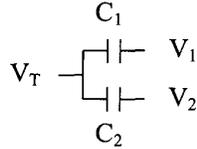
*We extend a class of analog CMOS circuits that can be used to perform many analog computational tasks. The circuits utilize MOSFET's in their subthreshold region as well as capacitors and switches to produce the computations. We show a few basic current-mode building blocks that perform squaring, square root, and multiplication/division which should be sufficient to gain understanding of how to implement other power law circuits. We then combine the circuit building blocks into a more complicated circuit that normalizes a current by the square root of the sum of the squares (vector sum) of the currents. Each of these circuits have switches at the inputs of their floating gates which are used to dynamically set and restore the charges at the floating gates to proceed with the computation.*

## 1. Introduction

A class of analog CMOS circuits has been presented which made use of MOS transistors operating in their subthreshold region[1][2]. These circuits use capacitively coupled inputs to the gate of the MOSFET in a capacitive voltage divider configuration. Since the gate has no DC path to ground it is floating and some means must be used to initially set the gate charge and, hence, voltage value. The gate voltage is initially set at the foundry by a process which puts different amounts of charge into the oxides. Thus, when one gets a chip back from the foundry, the gate voltages are somewhat random and must be equalized for proper circuit operation. One technique is to expose the circuit to ultraviolet light while grounding all of the pins. This has the effect of reducing the effective resistance of the oxide and allowing a conduction path. Although this technique ensures that all the gate charges are equalized, it does not always constrain the actual value of the gate voltage to a particular value. This technique works in certain cases[3], such as when the floating gate transistors are in a fully differential configuration, because the actual gate charge is not critical so long as the gate charges are equalized. If the floating gate circuits are operated over a sufficient length of time, stray charge may again begin to accumulate requiring another ultraviolet exposure. For the circuits presented here it is imperative that the initial voltage on the gate is set precisely and effectively to the circuit ground. Therefore, we utilize a dynamic restoration technique that makes it possible to operate the circuits indefinitely.

## 2. Floating gate translinear circuits

We begin by describing the math that governs the implementation of these circuits. A more thorough analysis for circuit synthesis is given elsewhere[1][2]. We will present a few simple circuit building blocks that should give the main idea of how to implement other designs.



**Figure 1. Capacitive voltage divider**

For the capacitive voltage divider shown in fig. 1, if all of the voltages are initially set to zero volts and then  $V_1$  and  $V_2$  are applied, the voltage at the node  $V_T$  becomes:

$$V_T = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2}$$

The current-voltage relation for a MOSFET transistor operating in subthreshold and in saturation ( $V_{ds} > 4U_t$ , where  $U_t = kT/q$ ) is given by[4]:

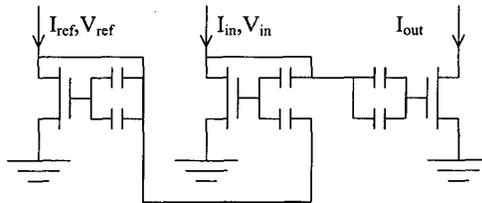
$$I_{ds} = I_o \exp(\kappa V_{gs}/U_t)$$

Using the above equation for a transistor operating in subthreshold, as well as a capacitive voltage divider, we produce the necessary equations of the computations desired.

In the following formulations, all of the transistors are assumed to be identical. Also, all of the capacitors are of the same size.

### 2.1. Squaring circuit

The formulation for the squaring circuit is given by the following.



**Figure 2. Squaring circuit**

$$\frac{U_t}{\kappa} \ln \left( \frac{I_{out}}{I_o} \right) = V_{in} \quad \frac{U_t}{\kappa} \ln \left( \frac{I_{ref}}{I_o} \right) = V_{ref}$$

$$\begin{aligned} \frac{U_t}{\kappa} \ln \left( \frac{I_{in}}{I_o} \right) &= \frac{V_{in}}{2} + \frac{V_{ref}}{2} \\ &= \frac{U_t}{\kappa} \ln \left( \frac{I_{out}}{I_o} \right)^{\frac{1}{2}} + \frac{U_t}{\kappa} \ln \left( \frac{I_{ref}}{I_o} \right)^{\frac{1}{2}} \\ I_{out} &= I_o \left( \frac{I_{in}/I_o}{(I_{ref}/I_o)^{\frac{1}{2}}} \right)^{\frac{1}{2}} = \frac{I_{in}^2}{I_{ref}} \end{aligned}$$

### 2.2. Square root circuit

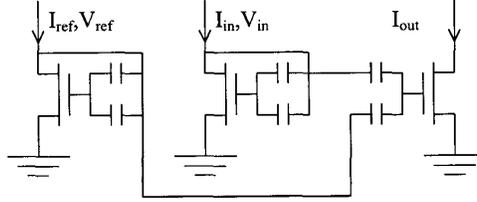


Figure 3. Square root circuit

The formulations for the square root circuit are done similarly and give:

$$I_{out} = \sqrt{I_{ref} I_{in}}$$

### 2.3. Multiplier/divider circuit

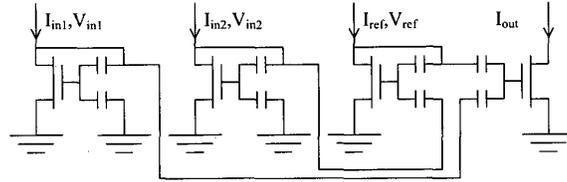


Figure 4. Multiplier/divider circuit

$$\frac{U_t}{\kappa} \ln \left( \frac{I_{in1}}{I_o} \right) = \frac{V_{in1}}{2} \quad \frac{U_t}{\kappa} \ln \left( \frac{I_{in2}}{I_o} \right) = \frac{V_{in2}}{2}$$

$$\begin{aligned} \frac{U_t}{\kappa} \ln \left( \frac{I_{ref}}{I_o} \right) &= \frac{V_{ref}}{2} + \frac{V_{in2}}{2} \\ \frac{V_{ref}}{2} &= \frac{U_t}{\kappa} \ln \left( \frac{I_{ref}}{I_o} \right) - \frac{U_t}{\kappa} \ln \left( \frac{I_{in2}}{I_o} \right) \\ \frac{U_t}{\kappa} \ln \left( \frac{I_{out}}{I_o} \right) &= \frac{V_{ref}}{2} + \frac{V_{in1}}{2} \end{aligned}$$

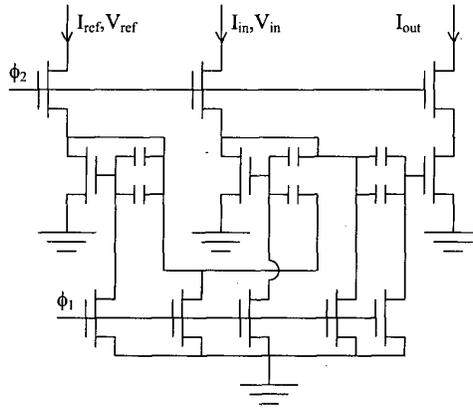
$$= \frac{U_t}{\kappa} \left( \ln \left( \frac{I_{ref}}{I_o} \right) - \ln \left( \frac{I_{in2}}{I_o} \right) + \ln \left( \frac{I_{in1}}{I_o} \right) \right)$$

$$I_{out} = I_{ref} \frac{I_{in1}}{I_{in2}}$$

Note that the divider circuit output is only valid when  $I_{ref}$  is larger than  $I_{in2}$ . This is because the gate of the transistor with current  $I_{ref}$  is limited to the voltage  $V_{fg_{ref}}$  at the gate by the current source driving  $I_{ref}$ . Since this gate is part of a capacitive voltage divider between  $V_{ref}$  and  $V_{in2}$ , when  $V_{in2} > V_{fg_{ref}}$ , the voltage at the node  $V_{ref}$  is zero and cannot go lower. Thus, no extra charge is coupled onto the output transistors. Thus, when  $I_{ref} > I_{in2}$ ,  $I_{out} \approx I_{in1}$ .

### 3. Dynamic gate charge restoration

All of the above circuits assume that some means is available to initially set the gate charge level so that when all currents are set to zero, the gate voltages are also zero. One method of doing so which lends itself well to actual circuit implementation is that of using switches to dynamically set the charge during one phase of operation, and then to allow the circuit to perform computations during a second phase of operation.



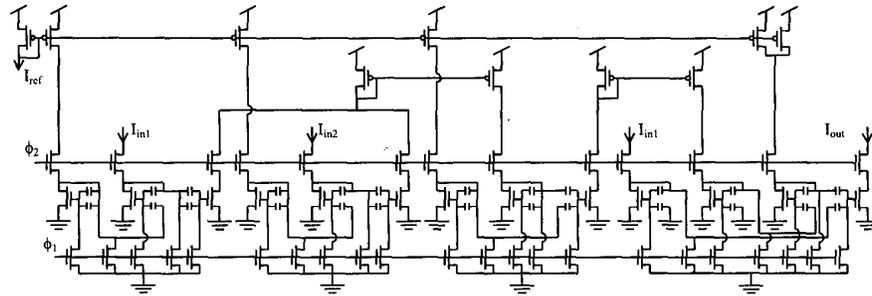
**Figure 5. Dynamically restored squaring circuit**

The squaring circuit in figure 5 is shown with switches now added to dynamically equalize the charge. A non-overlapping clock generator generates the two clock signals. During the first phase of operation,  $\phi_1$  is high and  $\phi_2$  is low. Thus, the input currents do not affect the circuit and all sides of the capacitors are discharged and the floating gates of the transistors are also grounded and discharged. This establishes an initial condition with no current through the transistors corresponding to zero gate voltage. Then, during the second phase of operation,  $\phi_1$  goes low and  $\phi_2$  goes high. This is the compute phase of

operation. The transistor gates are allowed to float, and the input currents are reapplied. The circuit now exactly resembles the aforementioned floating gate squaring circuit. Thus, it is able to perform the necessary computation.

The square root and multiplier/divider circuit are also constructed in the same manner by adding switches connected to  $\phi_2$  at the drains of each of the transistors and switches connected to  $\phi_1$  at each of the floating gate and capacitor terminals.

#### 4. Root mean square (vector sum) normalization circuit.



**Figure 6. Root mean square (vector sum) normalization circuit**

The above circuits can be used as building blocks and combined with current mirrors to perform a number of useful computations. For example, a normalization stage can be made which normalizes a current by the square root of the sum of the squares of other currents. Such a stage is useful in many signal processing tasks. This normalization stage is seen in figure 6. The reference current,  $I_{ref}$  is mirrored to all of the reference inputs of the individual stages. The reference current is doubled with the 1:2 current mirror into the divider stage. This is necessary because we need the reference current to be larger than the largest current we will divide by. Since the current we are dividing will be the square root of a sum of squares of two currents, when  $I_{in1} = I_{in2} = I_{max}$ , we need to make sure that the reference current for the divider section is greater than  $\sqrt{2}I_{max}$ . Using the 1:2 current mirror and setting  $I_{ref} = I_{max}$ , the reference current in the divider section will be  $2I_{max}$ , which is sufficient to enforce the condition.

The first two stages that read the input currents are the squaring circuit stages. The outputs of these stages are summed and then fed back into the square root stage with a current mirror. The output of the square root stage is then fed into the multiplier/divider stage as the divisor current. The reference current for the divider stage is twice the reference current for the other stages as discussed before. The other input to the divider stage will be a mirrored copy of one of the input currents. We can then feed the output back through another 2:1 current mirror (not shown) to remove the factor of 2. Thus, the overall transfer function computed would be:

$$I_{out} = I_{ref} \frac{I_{in1}}{\sqrt{I_{in1}^2 + I_{in2}^2}}$$

The addition of other divider stages can be used to normalize other input currents.

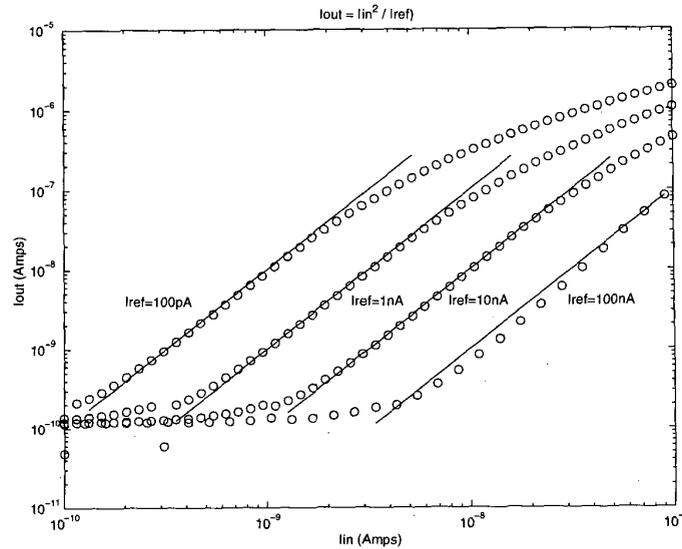


Figure 7. Squaring circuit results

This circuit easily extends to more variables by adding more input squaring stages and connecting them all to the input of the current mirror that outputs to the square root stage.

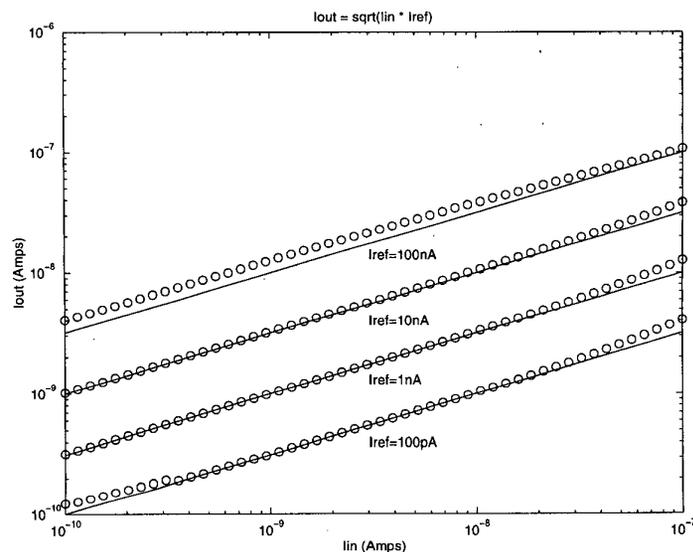
## 5. Experimental results

The above circuits were fabricated in a  $1.2\mu\text{m}$  double poly CMOS process. All of the pfet transistors used for the mirrors were  $W=16.8\mu$ ,  $L=6\mu$ . The nfet switches were all  $W=3.6\mu$ ,  $L=3.6\mu$ . The floating gate nfets were all  $W=30\mu$ ,  $L=30\mu$ . The capacitors were all  $2.475\text{ pF}$ .

The data gathered from the current squaring circuit, square root circuit and multiplier/divider circuit is shown in figures 7, 8, and 9, respectively. Figure 10 shows the data from the vector sum normalization circuit.

The solid line in the figures represents the ideal fit. The circle markers represent the actual data points.

The circuits show good performance over several orders of magnitude in current range. At the high end of current, the circuit deviates from the ideal when one or more transistors leaves the subthreshold region. The subthreshold region for these transistors is below approximately  $100\text{ nA}$ . For example, in figure 8, we see an offset from the theoretical fit for the  $I_{ref} = 100\text{ nA}$  case. Since the reference transistor is leaving the subthreshold region, more gate voltage is necessary per amount of current. This is because in above threshold, the current goes as the square of the voltage; whereas, in subthreshold it follows the exponential characteristic. Since the diode connected reference transistor sets up a



**Figure 8. Square root circuit results**

slightly higher gate voltage, more charge and, hence, more voltage is coupled onto the output transistor. This causes the output current to be slightly larger than expected.

Extra current range at the high end can be achieved by increasing the  $W/L$  of the transistors so that they remain subthreshold at higher current levels. The current  $W/L$  is 1, increasing  $W/L$  to 10 would change the subthreshold current range of these circuits to be below approximately  $1\mu\text{A}$  and hence increase the high end of the dynamic range appropriately. Leakage currents limit the low end of the dynamic range.

Some of the anomalous points, such as those seen in figures 7 and 9, are believed to be caused by autoranging errors in the instrumentation used to collect the data.

The divider circuit, as previously discussed, does not perform the division after  $I_{in2} > I_{ref}$ , and instead outputs  $I_{in1}$  as is seen in the figure.

The normalization circuit shows very good performance. This is because the reference current and the maximum input currents were chosen to keep the divider and all circuits within the proper subthreshold operating regions of the building block circuits.

The reference current for the normalization circuit,  $I_{ref}$ , at the input of the reference current mirror array was set to  $10\text{nA}$ . However, the ideal fit required a value of  $14\text{nA}$  to be used. This was not seen in the other circuits, thus it is assumed that this is due to the Early effect of the current mirrors. In fact, the SPICE simulations of the circuit also predict the value of  $14\text{nA}$ . Therefore, it is possible to use the SPICE simulations to change the mirror transistor ratios to obtain the desired output. Since this is merely a multiplicative effect, it is possible to simply scale the  $W/L$  of the final output mirror stage to correct it. Alternatively, it is possible to increase the length of the mirror transistors to reduce Early effect or to use a more complicated mirror structure such as a cascoded mirror.

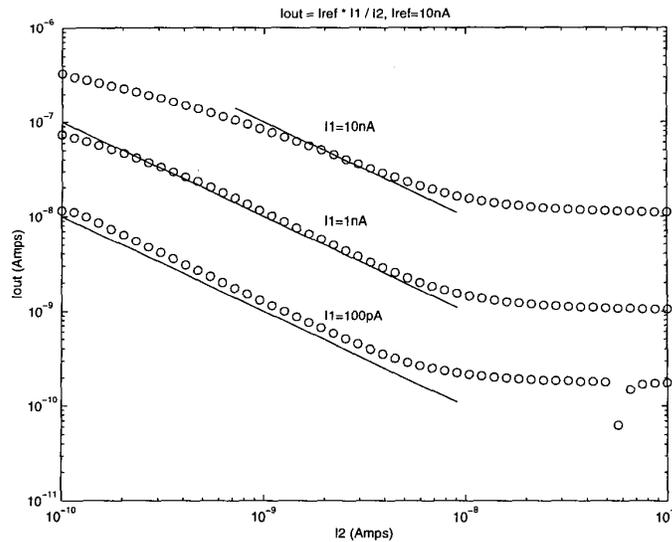


Figure 9. Multiplier/divider circuit results

## 6. Discussion

Unlike switched capacitor circuits that require a very high clock rate compared to the input frequencies, the clock rate for these circuits is determined solely by the leakage rate of the switch transistors. Thus, it is possible to make the clock as slow as 1 Hz or slower. The input can change faster than the clock rate and the output will be valid during most of the computation phase. The output does require a short settling period due to the presence of glitches in the output current from charge injection by the switches.

It may be possible to use a current mode filter or use two transistors in complementary phase at the output to compensate for the glitches[5].

One problem with these circuits is the presence of a large Early effect due to the overlap capacitance of the gate to the drain/source region of the transistor[1]. The method we chose to overcome this is to make the transistors long. This also required us to increase the width to keep the same subthreshold current levels. It may be possible to use some of the switches as cascode transistors to reduce the Early effect in the output transistors of the various stages. This would involve not setting  $\phi_2$  all the way to  $V_{dd}$  during the computation and instead setting it to some lower cascode voltage. This may allow a reduction in the size of the transistors. Furthermore, it is important to make the input capacitors large enough that any parasitic capacitances are very small compared to them.

Other techniques are also available which can improve matching characteristics and to reduce the size of the circuits. One such technique would involve using a single transistor with a multiphase clock that can be used as a replacement for all the input and output transistors in the building blocks[5].

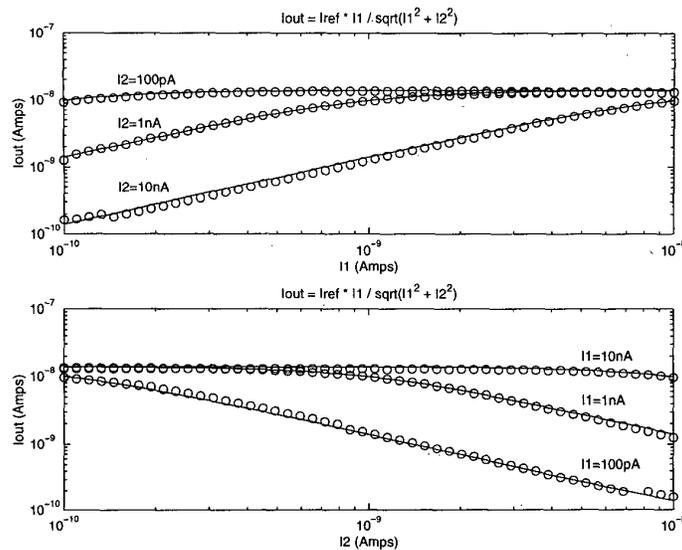


Figure 10. RMS normalization circuit results

## 7. Conclusion

We have presented a set of circuits for analog circuit design that may be useful for analog computation circuits and neural network circuits. We hope that it is clear from the derivations how to obtain other power law circuits that may be necessary and how to combine them to perform useful complex calculations. The dynamic charge restoration technique is shown to be a useful implementation of this class of analog circuits. Furthermore, the dynamic charge restoration technique may be applied to other floating gate computational circuits that may otherwise require initial ultraviolet illumination or other methods to set the initial conditions.

## References

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