Ultrafast WDM Logic

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***Abstract*— Ultrafast all-optical logic gates that accept optical inputs in which wavelength designates bit position within the overall byte are proposed and demonstrated. Four-wave mixing is shown to provide a conditional test function that can be used to construct any multi-input logic gate. Polarization provides the logic state for each bit. Implementations that use semiconductor optical amplifiers as the four-wave mixing medium can be monolithic and compact.**

***Index Terms*—Optical logic devices, optical mixing, optical signal processing, semiconductor optical amplifiers, ultafast optics, wavelength-division multiplexing.**

I. Introduction

THE DEPLOYMENT of wavelength-division-multiplexed (WDM) telecommunication systems is bringing ever greater resources to bear on new multiwavelength all-optical functions. To date, these functions assume serial, independent WDM data channels. Several authors, however, have investigated the possible advantages of byte-wide WDM (i.e., each bit of a word is assigned a distinct WDM wavelength so that byte parallel transmission is possible) [1]–[3]. Such systems could benefit from all-optical processing functions that are expressly designed to create wavelength logical operations. To date, optical processing functions such as all-optical logic gates [4] have been directed towards action on serial data streams (e.g., packet header recognition and routing [5]). The purpose of this paper is to show how ultrafast logic gates which operate on bits encoded in wavelength can be constructed. In addition, we demonstrate the idea by constructing an EXOR gate. These gates can be monolithic, and, like their electrical analogues, more sophisticated processing functions can be built up from parallel and/or cascaded combinations of individual gates.

The gates described here use four-wave mixing to provide an ultra-fast conditional test function that can be programmed to execute any desired truth table. Ultrafast four-wave mixing in semiconductor optical amplifiers (SOA's) and optical fibers has been considered recently as a technique for carrier wavelength translation in WDM systems [6]. We begin with a brief review of four-wave mixing in semiconductor optical amplifiers.

Fig. 1 illustrates the basic layout for this process. Two waves are introduced into an SOA, then write dynamic gain and index gratings in the SOA active layer. These gratings subsequently scatter energy out of the original waves creating the two new signal waves shown in the figure. An important aspect of this process is that it is polarization sensitive. In particular, if the semiconductor gain medium is isotropic then two orthogonally polarized input waves will not mix [7].[1] The mixing processes are well characterized and can generate waves of sufficient strength to shift 10-Gb/s modulated carriers by over 2 THz with low error-rate recovery of the data [8]. In addition, high bit rate cascading of these elements has recently been demonstrated [9], which is a necessary feature for application in logic gates.

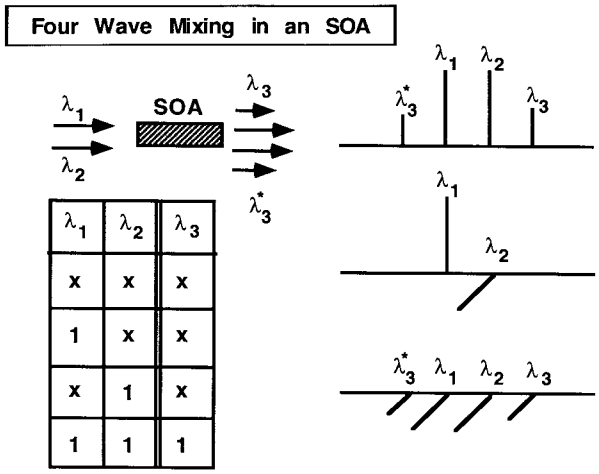

Fig. 1. Simplified diagram of four-wave mixing in a semiconductor optical amplifier. Two input signal waves are introduced into the amplifier and two new waves (making a total of four waves) are emitted from the device. The new waves provide a "conditional" test for coincidence of the two signal waves in time and polarization as illustrated in the right half of the figure for three different polarization configurations.

From the perspective of wavelength logic, four-wave mixing provides a simple but crucial function. It tests for a condition of coincidence of two wavelengths having the same polarization (the input waves in Fig. 1) and provides two new signals, either one of which can be used to confirm the coincidence. For linearly polarized input waves, we have the truth table presented in Fig. 1 for this process where the "1" condition signifies that power is present in the corresponding wavelength and the "X" condition signifies that power is not present in the corresponding wavelength. This conditional test function occurs on femtosecond time-scales and is therefore essentially instantaneous for nearly all data rates of interest.

II. Gate Operation and Programming

To create a logic function using this conditional test function, we must first define the meaning of logical "1" and logical

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[1] This is true in general in isotropic semiconductor gain media (e.g., bulk active layer SOA's) and, for most practical purposes, true for TE and TM directions in quantu-well SOA's.

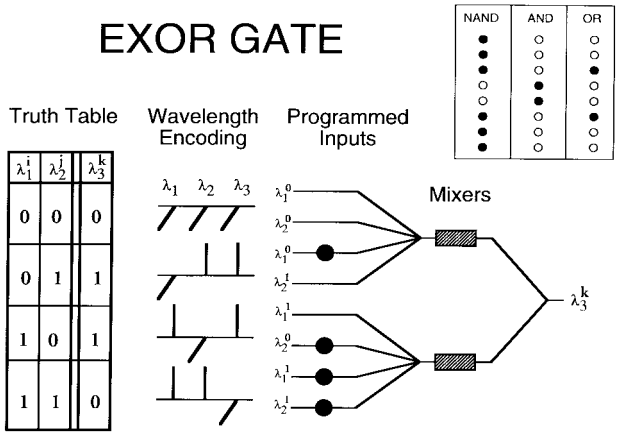

Fig. 2. Step 2 illustrated for the specific case of an EXOR gate. The inset shows the programming configurations for other logic gates.

"0" for each wavelength in the system. We define these states using the polarization state of the optical wave. That is, each wavelength will reside in one of two predetermined linearly polarized states that are designated as the logical "1" or the logical "0." This choice of logic states has the advantage that the logical inversion function can be implemented using a half-wave polarization element.

We now show that the half-wave element in conjunction with frequency selective taps and the four-wave mixing conditional test function can be used to construct any truth table. The first step in gate construction is to resolve the possible input bits of the two optical channels according to both wavelength and to polarization. This is easily accomplished through a series of wavelength and polarization selective wave guide splitters. The second step in gate construction amounts to "programming" the truth table. Fig. 2 illustrates the second step for a specific gate (in this case an exclusive OR, i.e., EXOR gate). Here, the logic states contributed from the first process are paired to form the four possible binary combinations. The truth table is then used to assign half-wave polarization rotation elements (i.e., invertors) to selected lines in the resulting network.

Suppose that we assign TM to logical "1" and TE to logical "0" and use a notation λ_C^Pwherein $P = 1, 0$ (TM, TE) indicates the polarization state associated with one of the two bits ($C = 1, 2$). Using this notation, the bottom two inputs in Fig. 2 correspond to logical "1" on each optical channel (i.e., both are TM polarized). The EXOR truth table requires that a logical "0" (TE polarized wave) be output for this input condition. If each input is inverted (i.e., half-wave elements are inserted on the bottom two guides), then four-wave mixing in the SOA will produce a new wave that is polarized TE when this condition occurs. (Note: a solid circle in the figure is the symbol for the half-wave rotation element). Proceeding up to the next two input states, logical "1" (TM) on the first input wavelength and logical "0" (TE) on the second input wavelength require a logical "1" (TM) output according to the EXOR truth table. This requires that a half-wave element be introduced on the second input as indicated, so that when the [1,0] input (equivalently [TM,TE]) occurs, four-wave mixing will create a third wave polarized TM or logical "1." Proceeding up the remaining inputs, the truth table locations are filled in as shown. There is a unique arrangement of half-wave elements for each truth table. The placement of these half-wave elements therefore amounts to programming the truth table into the gate.

The resulting output waves are then input to the two semiconductor optical amplifiers shown. These waves undergo four-wave mixing in the amplifier and generate two new output waves. The polarization of either of these new waves is logically related to the polarization of the input waves according to the truth table. Four-wave mixing has thus synthesized a single channel logical result from two distinct input channels. The desired gate operation (i.e., truth table) has been implemented at femtosecond speeds in the optical domain.

Note that two four-wave mixing elements (rather than one) are required to perform the conditional test functions. Two elements are necessary to separate the four input cases into two subgroups as illustrated in the figure. Otherwise, unintentional pairing of states would result in the mixing process creating spurious logical outcomes. It is important to note, however, that the separate mixing processes result in one and same output wavelength.

Proceeding as outlined above, it is possible to implement any two-input truth table by this simple programming procedure. The inset to Fig. 2 gives the gate programming configuration for three other common logic gates (AND, OR, NAND). Obviously, more sophisticated multi-input or multi-output gate functions are possible using this same idea. An example is shown in Fig. 3 in which an EXOR with Carry bit is implemented as might be required in an integer adder circuit.

It is important to note that all elements described here can be monolithically integrated. Thus, compact optical chip sets can be developed for any desired truth table. Furthermore, the architecture of the logic gates permits a convenient separation of the passive (linear) programmable elements from the conditional nonlinear test steps (four-wave mixing). Thus, the programmable elements could be monolithically integrated as a separate module and then later attached to the conditional test elements. This could be desirable for increased ease in fabrication or to make possible use of different fabrication technologies for the programmable and the conditional test elements. For example, a dynamically programmable set of gates could use electrical (or optical) control signals to reconfigure their function by reprogramming the configuration of invertors (see Fig. 4). This might require the use of a thin film fabrication technology that is incompatible with the four-wave mixing element technology, thus requiring the kind of separation described above.

III. Experimental Demonstration

In a preliminary experiment, we have tested the operation of the EXOR gate by implementing it in the simple way shown in Fig. 5. Notice that we did not use polarization maintaining wave guides in this experiment; as a result, we could not obtain the required polarization components at the input to each SOA by simply inputting to the gate TM (λ_1^1 and λ_2^1) and TE (λ_1^0 and

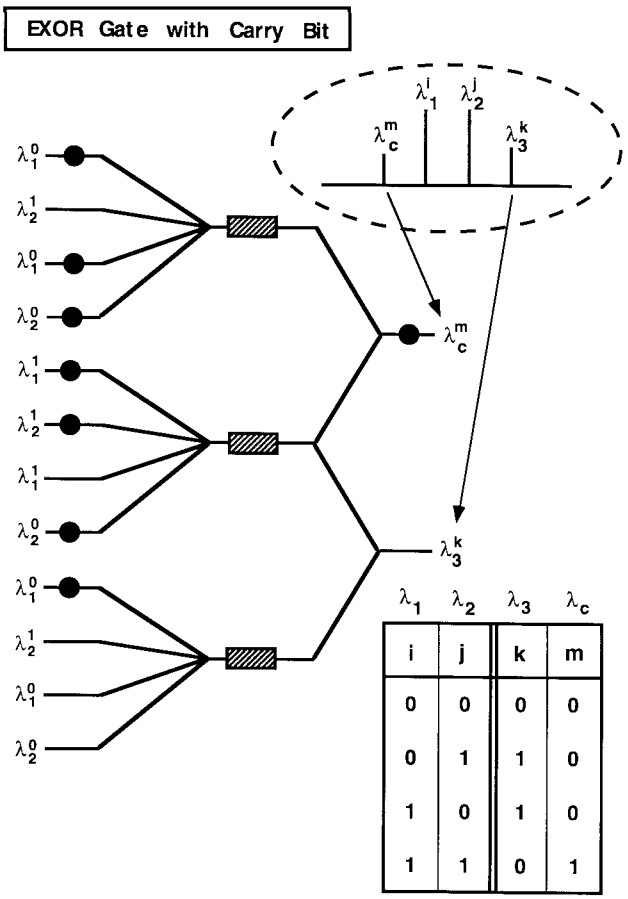

Fig. 3. EXOR with Carry bit gate function implemented using a single programming array.

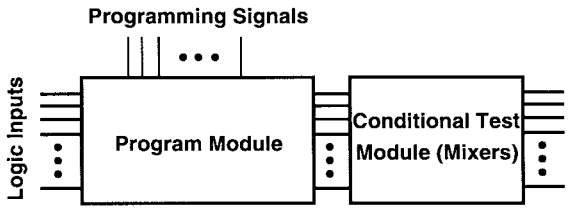

Fig. 4. The gate architecture described here provides a convenient separation of functions into those related to programming (polarization control) and those related to conditional test (nonlinear mixing). This could provide important fabrication simplifications that enable incompatible thin film technologies to be used for each function. This figure illustrates a dynamically reconfigurable multi-input processor that could use one technology for the Program Module to enable programmable gates and another for the Conditional Test Module to implement the ultrafast four-wave mixing.

λ_2^0) waves followed by polarization rotators. Instead, we used the polarization controllers shown in Fig. 5 (each of which is labeled by the polarization state that it is set to produce at the SOA input).

Furthermore, due to limited availability of components, only one of the input signals (X_1, of wavelength λ_1) was modulated with digital information. This signal was provided by an externally modulated distributed feedback laser. The modulator was a dual-output Mach–Zehnder interferometer, whose two output ports provide the modulating signal and its complement (i.e., in the language of Fig. 2, the waves λ_1^1 and

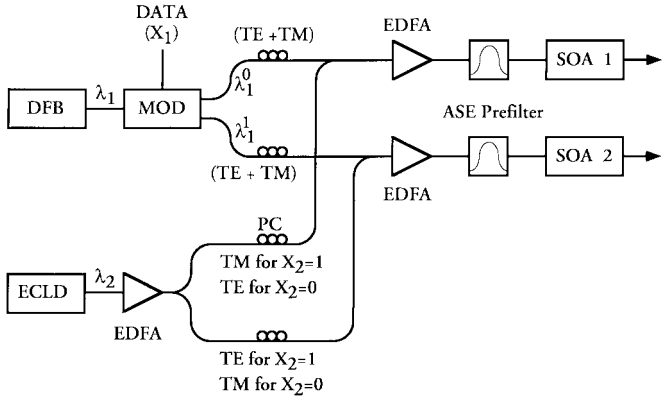

Fig. 5. Schematic diagram of the experimental setup used to implement the EXOR gate. The acronyms are DFB: distributed feedback laser; MOD: dual-output Mach-Zehnder modulator; ECLD: external cavity laser diode; PC: polarization controller; EDFA: erbium doped fiber amplifier; ASE Prefilter: 10 nm wide optical bandpass filter; SOA: semiconductor optical amplifier.

λ_1^0 respectively). It was driven by a Hewlett-Packard bit-error-rate (BER) tester with a preset bit pattern (at 2.5 Gb/s). On the other hand, the other input signal (X_2, of wavelength λ_2) was constant and set first to a logical one and then to a logical zero. In the former case, the EXOR truth table requires that the output signal Y be the complement of X_1; in the latter case that $Y = X_1$.

The results of this experiment are shown in Fig. 6. The upper trace is the preset bit pattern (10 011 100) encoded on the input signal X_1 (i.e., the optical intensity in wave λ_1^1), measured with a Hewlett-Packard microwave transition analyzer. The middle trace corresponds to the case $X_2 = 1$ and shows the four-wave mixing signal generated in SOA 1, which in this case is the TM component of the overall output wave of the EXOR gate (see Fig. 5). As such, this trace gives the output signal Y (given that TM is interpreted as a logical one). Consistent with the truth table, we indeed find it to be the complement of X_1. Similarly, the lower trace gives Y for $X_2 = 0$ (i.e., the four-wave mixing signal from SOA 2 in this case), which can be seen to be equal to X_1, again as required by the truth table. The SOA's used in the experiment have a small-signal gain of only 10 dB, which results in a low four-wave mixing conversion efficiency; this explains the additional noise on the lower two traces. We emphasize that this is only a preliminary demonstration.

IV. Conclusion

We have described logic gates that process information in wavelength. The processing occurs entirely in the optical domain and uses ultrafast wave mixing as a conditional test function. As a result, the clock cycle for the gates described here can reach exceedingly high values. The product of integer word length "N" and gate clock speed can exceed several terabits per second in the design proposed here and could ultimately be as high as the overall optical bandwidth of the system. The approach enables a modular design similar to that of conventional electronic digital chips. Specific gates (e.g., AND, OR, EXOR, NAND) are programmed into chips to encode the desired truth table. The conditions generated

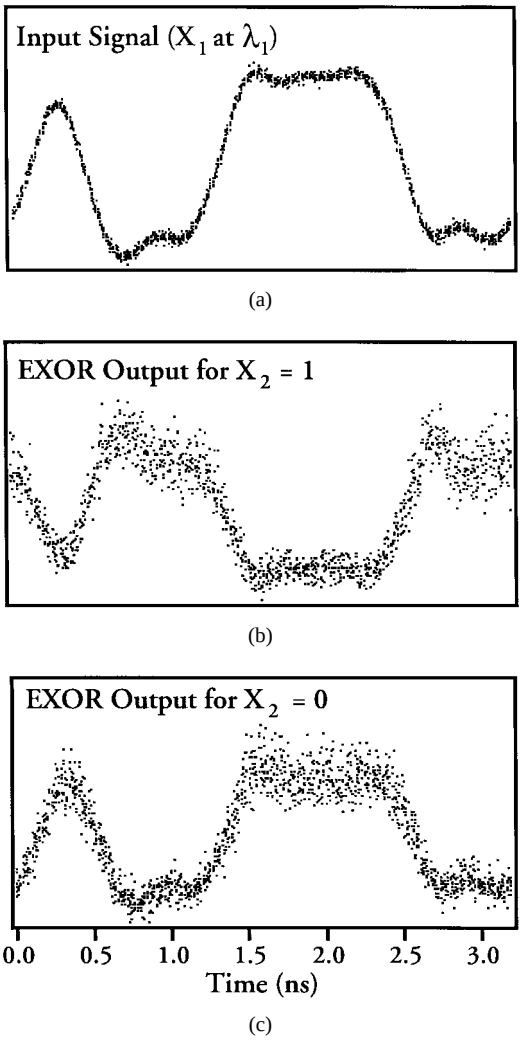

Fig. 6. Experimental results obtained with the setup of Fig. 5 for the EXOR gate. The upper trace is the input bit pattern X_1. The middle and lower traces represent the output signal of the gate given that other input X_2 is respectively, a logical one or a logical zero. The implementation of the EXOR truth table is clearly seen.

by this chip are tested by the four-wave mixing process, creating an output wavelength whose polarization is related to the polarization states of the input waves by way of the truth table. More complicated multi-input functions are possible using this approach and dynamically programmable functions could be envisioned in which either electrical or optical signals reconfigure a set of gates by reprogramming the invertor operations in the chips. Finally, we have provided a demonstration of the EXOR gate at gigabit rates.

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Kerry J. Vahala (S'82–M'84), for a biography, see this issue, p. 540.

Roberto Paiella (S'97), for photograph and biography, see this issue, p. 540.

Guido Hunziker, for photograph and biography, see this issue, p. 540.